EECS150 Components and Design Techniques for Digital Systems

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Outline

- Enrollment & Attendance
- Course Materials & Content
- Course Structure & Grading
- Cheating
- A Few Basic Principles of Digital Design

Enrollment

- If you are enrolled and plan to take the course you must attend your lab section next week, if not you will be dropped from the class roster. No exceptions!

- If you are on the wait list and would like to get into the class you must:
  1. Pick up and fill out an appeal form (available at the CS office) and turn it in to 390 Soda, by 5pm Friday, September 6.
  2. Attend lectures and do the homework, the first two weeks.
  3. In the second week of classes, go to the lab section in which you wish to enroll. Give the TA your name and student ID.
  4. Later, we will process the waitlist based on these requests, and lab section openings.
  5. Note: if you are not on the waitlist, you will not be considered for enrollment.

- No lab (or discussion) sections this week.

Cancelled Sections

Lab section 11 M 9-12

Discussion section 104 M 4-5

- If you are currently enrolled in one of these sections, see:

  Michael-David Sasson (msasson@cs, 379 Soda, 3-6002)

  after Wednesday for help in switching to a different section.

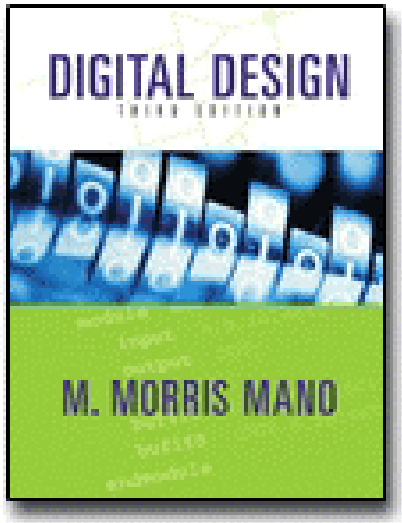
- You will get priority over waitlisted students into new sections.

Attendance

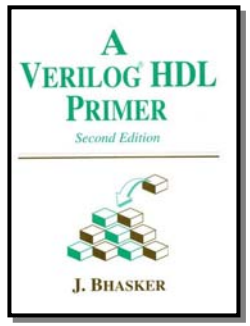
- Attend regular lectures and ask questions. If you cannot physically be here, you can watch the lecture on the web live or watch it later from the archive: *webcast.berkeley.edu*
- Attend weekly "lab lecture" (Friday 2-3). Lab lecture will probably not be webcast. Also, you we will have a short quiz at the beginning of each lab lecture.
  - Two quiz scores for each student will be dropped at the end of the semester, so you can miss two lab lectures (save this option for important dates – like job interview trips, etc.)
- Attend your lab section. You must stick with the same lab section all semester.
  - We will put together a lab section exchange in a few weeks to help you move to a different section.
- Attend any discussion section. You may attend any discussion section that you want regardless of which one you are enrolled in. Attendance is optional, but useful.
- The instructor and TAs hold regular office hours (see class webpage). Please take advantage of this opportunity!

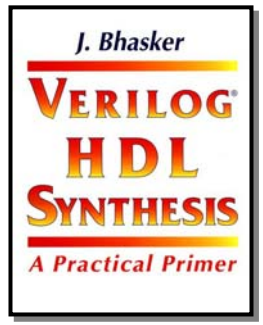
Course Materials

- Textbook: Digital Design, Third Edition, M. Morris Mano, Prentice Hall, 2002



Other useful books:





- Class notes, homework & lab assignments, solutions, and other documentation will be available on the class webpage:

  http://www-inst.eecs.berkeley.edu/~cs152/index.html

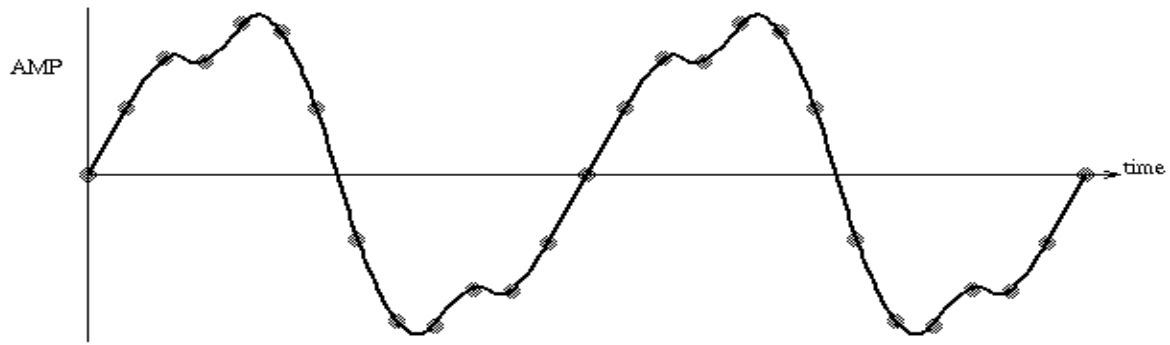
  – Check the class webpage and newsgroup often!
  – You are responsible for checking the class webpage at least once every 24 hours.

Course Content

Components and Design Techniques for **Digital Systems**

Synchronous Digital Hardware Systems

- Synchronous: "Clocked" - all changes in the system are controlled by a global clock (not asynchronous)
- Digital: All inputs/outputs and internal values (signals) take on discrete values (not analog).
  - Example: sound waveform



  - **A series of numbers is used to represent the waveform, rather than a voltage or current, as in analog systems.**

Course Content

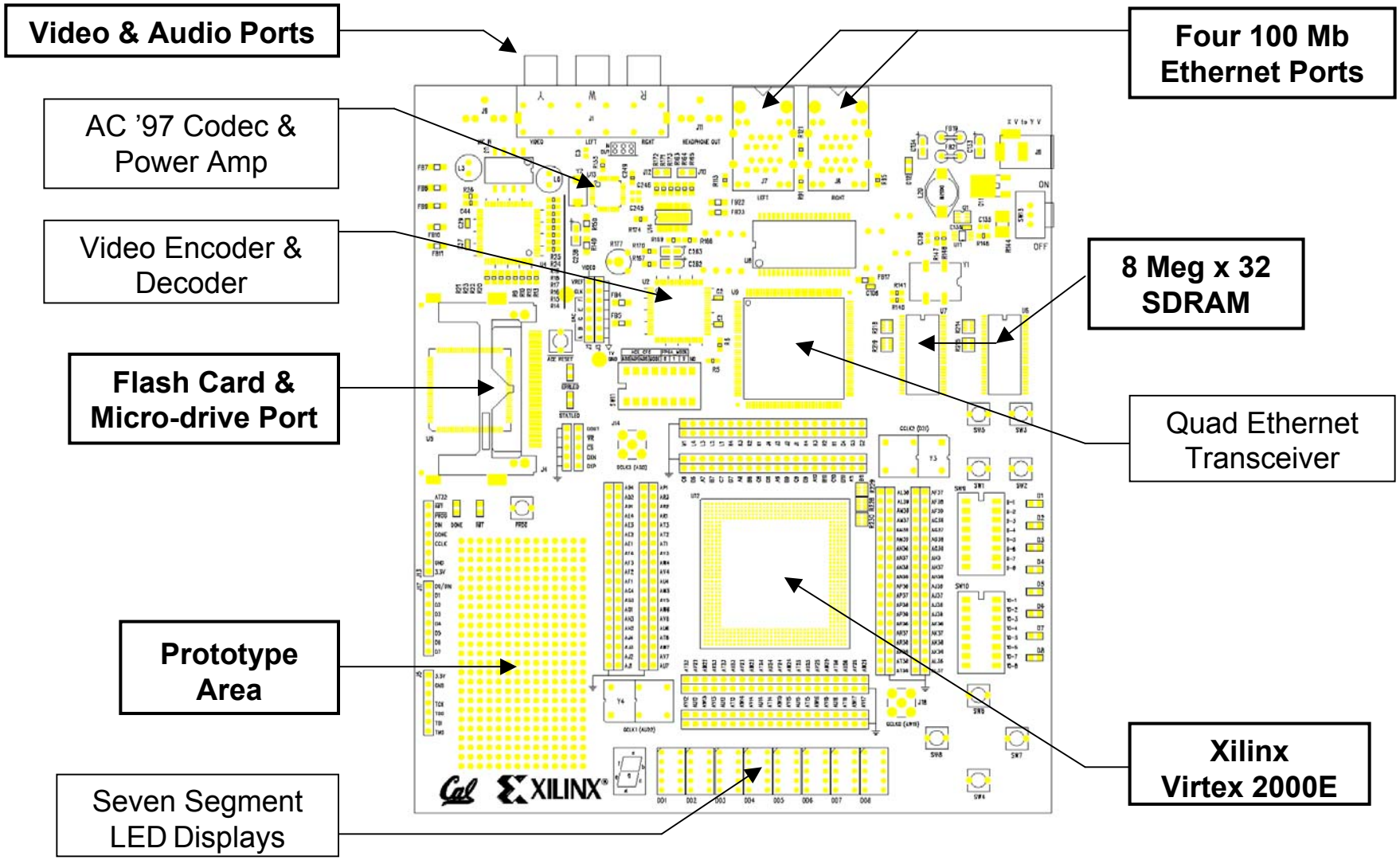
- Digital Architectures
- Arithmetic units, controllers
- Memory elements, logic gates, busses
- Transistor-level circuits
- Transistors, wires

- Not a course on transistor physics and transistor circuits. Although, we will look at these to better understand the primitive elements for digital circuits.
- Not a course on computer architecture or the architecture of other systems. Although we will look at these as examples.

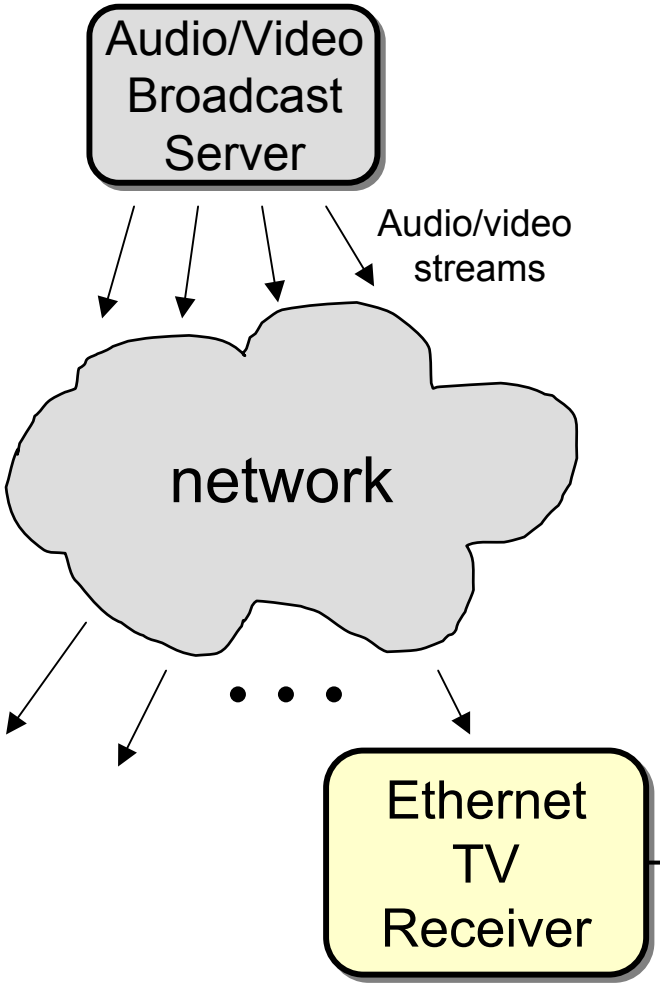
Significant Changes as of Spring 2002

- Verilog replaces schematics
- New laboratory facility, 125 Cory. Thanks to National Semiconductor!
- Mano book replaces Katz.
- Changes in order and emphasis in course content.
- Not Changed:
  - large project
  - lots of work
  - lots of fun!
- Significant change for this semester: new lab/project board.
  - Thanks to Xilinx, Inc.

New Class Lab/Project Board

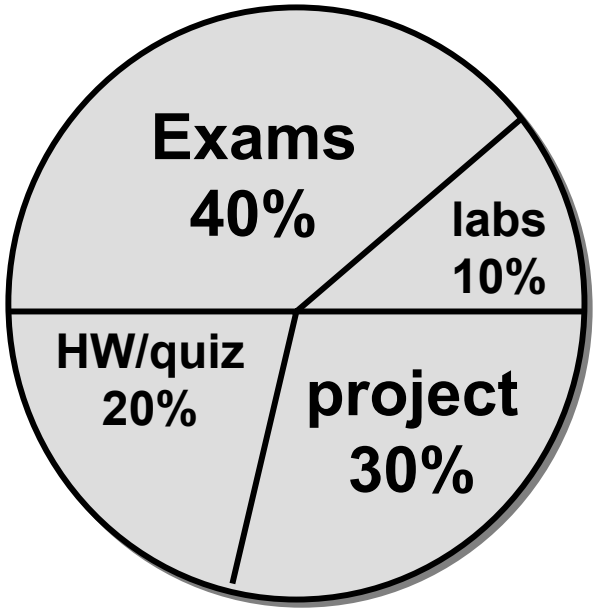


Final Project: eTV (ethernet TV)



- Multiple audio/video streams are broadcast over the 100Mbit switched ethernet in the lab.
- The receiver must selects a particular stream from the network and displays it on LCD display.
- Everyone (working in groups of 2) will design, implement, debug, and demo a receiver for Ethernet TV.

Course Grading



- Three exams of approximately equal weight - held in the evening.
- Weekly homework based on reading and lectures.
  - graded on effort only,
  - out at the end of each week, due before next week quiz.
- Weekly quiz closely related to one of the homework problems. Given at the beginning of the lab lecture.
  - Most of "HW/quiz" grade points based on quiz grades.
- Lab exercises for weeks 2-6, followed by project checkpoints and final checkoff.
- Labs and checkpoints due within the first 30 minutes of your next lab session.

Course Structure & Grading

A week in the life of a EECS150 student

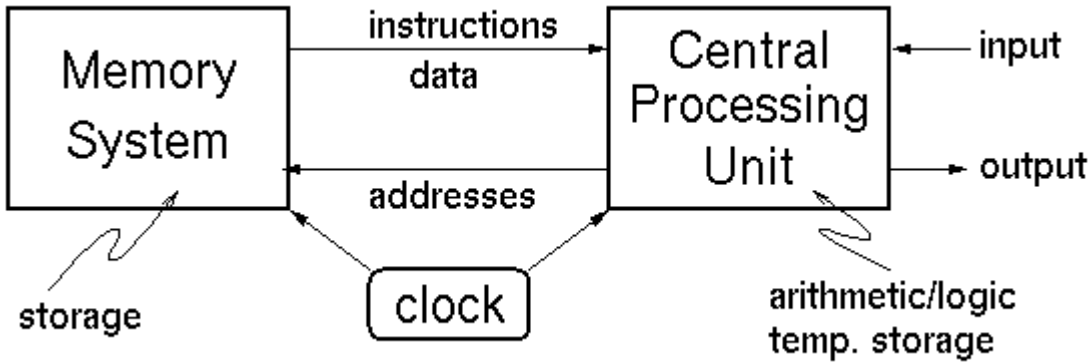
Monday (for example):	
Discussion section	1
Tuesday:	
Lecture 2-3:30	1.5
Wednesday (for example):	
Lab section	3
Thursday:	
Lecture 2-3:30	1.5
Friday:	
Lab Lecture	1
Reading book, reviewing notes	3
Homework	4
TOTAL	15 hours/week

Cheating

- Any act that gives you unfair advantage at the expense of another classmate.
- Examples:
  - copying on exams, homework,
  - copying design data,
  - modifying class CAD software,
  - modifying or intentionally damaging lab equipment.
- If you ever have a question about what will be considered cheating, please ask me.
- We will use software to automatically compare your submitted work to others.
- If we detect you are involved in cheating you will be:
  - turned over to the Office of Student Judicial Affairs, for investigation and sanctions, additionally,
  - if you are found to have cheated, you will receive an F in the course.

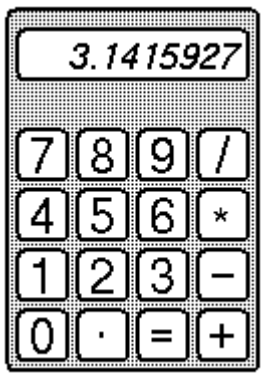
Example Digital Systems

- Digital Computer



  – Usually design to maximize performance. "Optimized for speed"

- Handheld Calculator



- Usually designed to minimize cost. “Optimized for low cost”

- Of course, low cost comes at the expense of speed.

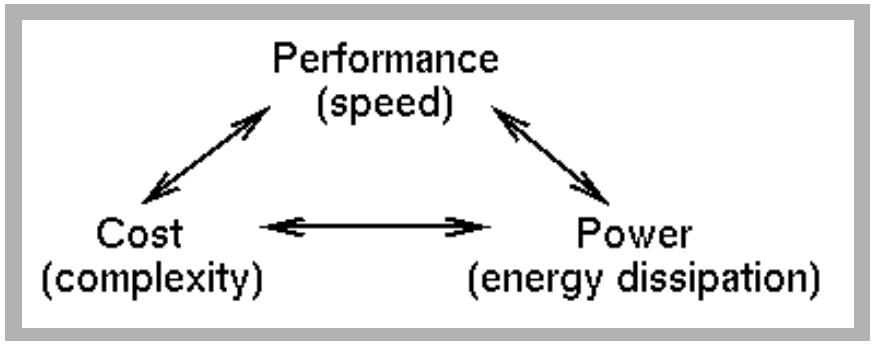
Example Digital Systems

- Digital Watch

Designed to minimize power.
Single battery must last for years.

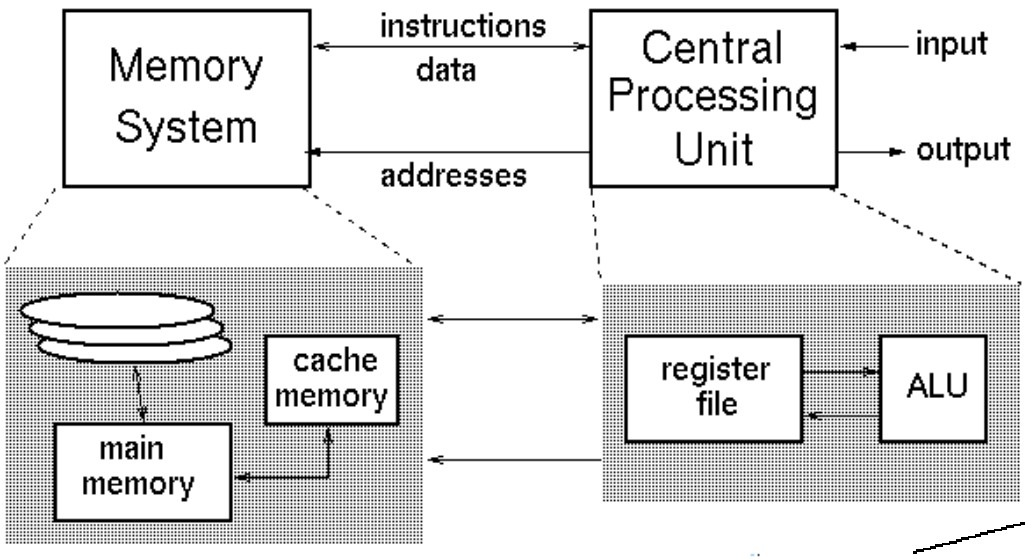
  - Low power operation comes at the expense of:
    - lower speed
    - higher cost

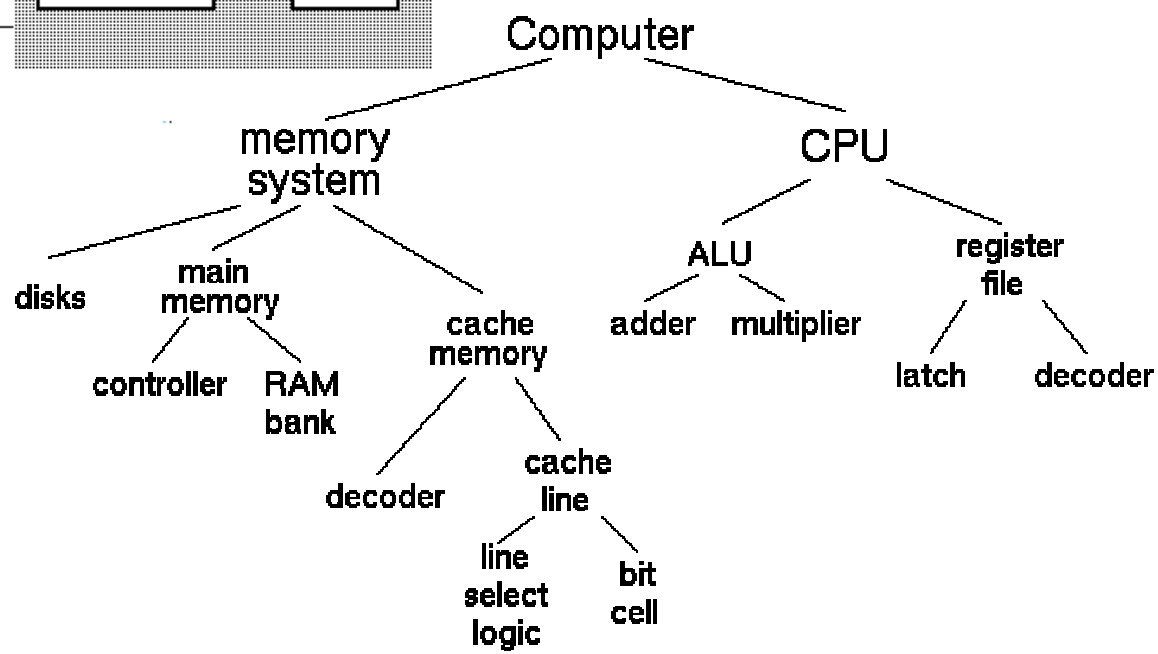
Basic Design Tradeoffs



- You can improve on one at the expense of worsening one or both of the others.
- These tradeoffs exist at every level in the system design - every sub-piece and component.
- Design Specification -
  - Functional Description.
  - Performance, cost, power constraints.
- As a designer you must make the tradeoffs necessary to achieve the function within the constraints.

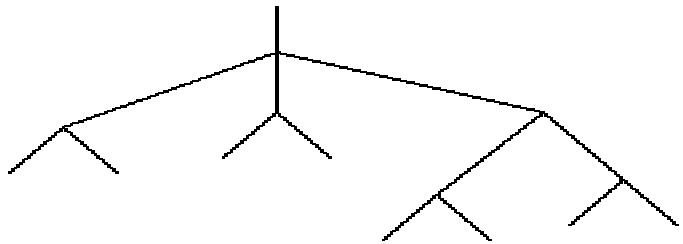
Design Representation





Hierarchy in Designs

- Helps control complexity -
  - by hiding details and reducing the total number of things to handle at any time.
- Modulalizes the design -
  - divide and conquer
  - simplifies implementation and debugging



- Top-Down Design
  - Starts at the top (root) and works down by successive refinement.
- Bottom-up Design
  - Starts at the leaves & puts pieces together to build up the design.
- Which is better?
  - In practice both are needed & used.
    - Need top-down divide and conquer to handle the complexity.
    - Need bottom-up because in a well designed system, the structure is influence by what primitves are available.

Digital Design

Given a functional description and performance, cost, & power constraints, come up with an implementation using a set of primitives.

- How do we learn how to do this?
  1. Learn about the primitives.
  2. Learn about design representation.
  3. Learn formal methods to optimally manipulate the representations.
  4. Look at design examples.
  5. Use trial and error - CAD tools and prototyping.
- *Digital design is in some ways more an art than a science. The creative spirit is critical in combining primitive elements & other components in new ways to achieve a desired function.*
- Unlike art we have objective measures of a design:

  performance cost power