

University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Sciences

EECS150
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Homework #11

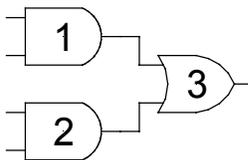
This homework is due on **Tuesday Dec 3rd by 2pm**. Homework will be accepted in the EECS150 homework box outside 125 Cory Hall. Late homework will be penalized by 50%. No late homework will be accepted after the solution is handed out.

1. Power/energy units.

- a) Consider a logic gate driving an output node with an average of one transition per eight clock cycles (clock frequency is 100MHz). The output has a total capacitance of 10fF, and $V_{dd}=3$ volts. What is the average power consumption of the gate?
- b) Battery storage is often expressed in Watt-hours. What is the energy storage capacity in Joules of a 10 Watt-hour battery? How long would it power the above gate?

2. Switching power.

Consider the simple AND/OR circuit shown below. New values are applied to the four inputs at a rate of f . Input values are applied as independent uniform random sequences to each of the four inputs; i.e., for each input, on each appearance of a new input, $\text{Prob}(1)=\text{Prob}(0)=1/2$. Write an expression for the average power consumed by gate 1 in terms of f and the switching energy E_{sw} . Do the same for gate 3.



3. Power and voltage scaling.

To first approximation, under a limited voltage range, a reduction in power supply voltage (V_{dd}) in MOS circuits results in a linear increase in gate delay and thus maximum clock rate. This fact is often used to reduce power consumption in cases where a reduction in performance can be tolerated, or compensated for in another way.

Consider a special processor inside a car engine, whose job is to control the fuel/air mixture to the injectors. Let's assume that the processor must make 100 adjustments per second and it takes 5K operations for each adjustment. Assume that we chose to use a processor that has peak performance of 1M operations/sec and at that rate uses 1 Watt. Your boss tells you that 1 Watt is too much. Without changing the supply voltage, is there a way to reduce the power consumption? If so, by how much? Is there a way to reduce the power consumption even more by lowering the supply voltage? If so, what voltage level would you use and what would be the resulting power?

4. Hamming codes.

From Mano: problems 7-10, 7-11, 7-12, 7-13.

5. Linear Feedback Shift Register (LFSR).

- a) Write out the sequence produced by a 3-bit LFSR initialized to "001".
- b) Draw the circuit diagram for a 5-bit LFSR.

6. SR and JK flip-flops.

- a) Starting from the SR latch show how to construct a level-sensitive D-flip-flop from NAND gates and inverter(s).
- b) Construct a JK flip-flop using a D flip-flop, a 2-to-1 mux, and an inverter.