UC Berkeley
College of Engineering
EECS Department

EECS150 J. Wawrzynek, J. Sampson
Fall 2002

Quiz #5 Solution

Name: _____

SID: _____Lab section number: _____

For this problem assume that your complete library of logic components comprises 2-input AND, OR, and XOR gates, inverters, and inverting tri-state buffers. Assume that inverters have cost of one unit and delay of one unit, and all other logic gates have cost of 2 units and delay of 2 units for all inputs (ignore fanout and wire delay). With these assumptions, a 2-input mux could be implemented with two inverting tri-states and 2 inverters, and would cost 6 and have delay 4 from the select input to output and a delay of 3 from data input to output.

Consider the structure of a partially hierarchical 16-bit **carry-select adder** with inputs a[15:0], b[15:0], c_{IN}, and outputs s[15:0], c_{OUT}. The hierarchy is as follows: the initial adder has been divided in half the second half duplicated, and those sub-adders have again each been divided once more in the same fashion. All of the final resulting "sub-adders" are carry-ripple adders. Assume that each ripple adder is made up only of full-adder cells (one-bit adders). **When calculating delay, please specify how you have implemented your carryout in the full adder cell.**

a) Calculate the total cost for the 16-bit carry-select adder:

Subdivision & duplication once yields 3 8-bit adders and 9 muxes. Subdividing once more yields 9 4-bit adders and 24 muxes. Therefore:

Total cost = 9 * 4 * Cost(FA) + 24*Cost(Mux) = **36 * 14 + 24 * 6 = 648** OR **36 * 10 + 24 * 6 = 504** depending on how the Full Adder cell was constructed.

b) Calculate the delay from c_{IN} to c_{OUT}:

Delay of 4 FA ripple + delay of 2->1 mux + delay of 2->1 mux = depending on FA design,

3gates*2delay*4FA +4delay +4delay = **32 delay**

OR

3gates*2delay*1FA +2gates*2delay*3FA +4delay + 4delay = **26 delay**

c) In words, describe the path with the worst case delay from any of the inputs to any of the outputs:

The path from (depending on how the full adder cell is constructed) either A0/B0 to Cout, or Cin to Cout, namely, through the first 4-bit ripple, through the carryout mux 4 bits further down the chain, and through the last carryout mux 8 bits further down the chain from that.