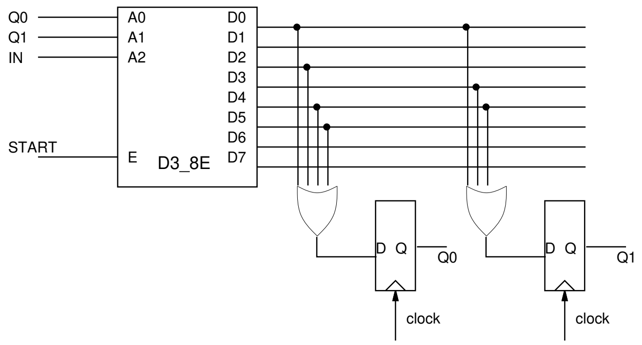
Professor Fearing EECS150/Problem Set 3 Fall 2003

Due at 10 am, Fri. Sep. 19 in box outside 125 Cory Hall

Reading Ciletti: 3-3.7, 4-4.3, 5-5.9

1. FSM Analysis (20 pts)

The D3_8E component is a 3:8 decoder, with all outputs 0 when E=0. Determine the state transition table and draw the state diagram for this FSM:



2. FSM Design (20 pts)

Design a Mealy type FSM for a sequence recognizer. The FSM should assert Output exactly once for every (possibly overlapping) sequence "110" detected in the synchronized serial input stream Z. Show timing diagram, state diagram, and state table using D-type FFs.

3. FSM Design Manchester to NRZ (30 pts)

You are given a Manchester encoded data stream M synchronized to a clock $Clock2$ which is at twice the data rate of M.

a. Design a Mealy FSM which outputs an NRZ data stream at clock rate $Clock1 = Clock2/2$.

b. Design a Moore FSM which outputs an NRZ data stream at clock rate $Clock1 = Clock2/2$.

(For each part, show state diagram, state table, and functional timing diagram. The timing diagram should show input, state transitions, and output with input data presented as 0, 0, 1, 0, 1, 1, 0.)

4. Parallel-to-Serial Converter (30 pts)

Design a system which can convert 8 parallel input bits (DataIn[7:0]) to a serial output SerialOut. A clock signal is provided which is synchronized with DataIn[7:0]. When Start is asserted, the system should first load the 8 bits, then shift out 8 bits (one bit per clock cycle), then stop shifting and assert the Done signal. The data path of the system should use an 8 bit loadable shift register (such as Fig 5-32) using 8 D-FF with clock enables. The control section should use a D-FF based Mealy FSM to control loading, shifting, or idle of the shift register. Show a timing diagram of operation, and state diagram and state table for the controller FSM. (You do not need to show state diagram or state table for the shift register.)