Professor Fearing EECS150/Problem Set 4 Fall 2003

**Due at 10 am, Fri. Sep. 26 in box outside 125 Cory Hall**

( Solution distributed Fri. 2 pm in lab lecture, hence no late HW will be accepted.)

Quiz 1: Tues. Sep. 30 210-330 pm in class. Reading Ciletti: 5-5.16, 6-6.8, 5.17, 11.2

1. Control FSM/Counter Data Path (25 pts)

Design a system with 4 outputs $Count[3:0]$ where a synchronized input $Start$ causes the system to count in the sequence $Count = 3, 4, 5, 10, 11, 12, 15, 14, 13$ and then halt, with $Count[3:0] = 4b'1101$. The $Start$ input is ignored except when in the halt state. The data path should use a 4 bit binary up/down ($U/\bar{D}$) counter with synchronous $Load$ input and count enable $CE$. Load values can be selected by a multiplexer. The controller should be a Mealy machine.

a. Draw a block diagram of datapath, using mux for load select, and comparator blocks. Label all inputs/outputs.

b. Draw a timing diagram, showing proper functioning of system and all relevant signals.

c. Draw state diagram and ASMD diagram for the controller.

d. Draw state table for the controllers using D type FF for state register.

2. Registered Mealy FSM (25 pts)

Design a Mealy type FSM for a sequence recognizer. The FSM should assert Output for every (possibly overlapping) sequence "1101" detected in the synchronized serial input stream $Z$. For example data stream, use $Z = 0, 1, 1, 0, 0, 1, 0, 1, 1, 1, 0, 1, 1, 0, 1$.

a. Using a Mealy FSM, show timing diagram for given input data stream, state diagram, and state table using D-type FFs.

b. Show timing diagram using registered Mealy outputs (Fig 6-44a) and state table.

c. Show timing diagram for Mealy machine registered on next state function (Fig 6-44c) and state table.

3. Data Path/TriState (25 pts)

Consider the register bank of Figure 3-13 as a datapath. Design a Moore type FSM, which after receiving a synchronized Start signal will tranfer the contents of R2 to R3, R1 to R2, and R0 to R1. After transfer is complete, system returns to Idle state. Show timing diagram, (making sure to avoid bus conflicts), state diagram, ASMD diagram and state table for the controller using D type FF.

4. Timing Analysis (25 pts)

Using a timing diagram, determine the minimum clock period for this circuit. (Parameters: $T_{setup} = 0.8$ ns min, $T_{hold} = 1.5$ ns, $0.5 < T_{CKO} < 1.4$ ns, $T_{delay1} = 1.0$ ns, $T_{delay2} = 0.5ns$, and inverter propagation $0.8 < t_p < 1.2$ ns.) Also, determine the fastest inverter which could be used in this circuit (i.e. if the inverter were faster than 0.5 ns, is there any potential problem?)