Professor Fearing EECS150/Problem Set 9 Fall 1999

Due at 10 am, Fri. Nov. 21 in box outside 125 Cory Hall

(This problem set may be done individually or by a group of two people maximum.)

Problems 1 and 2 use the micro-programmed control unit (MCU) on the web page, and the Ciletti CPU of Figure 7-10. Microcode should be listed in symbolic form (assume a smart micro-assembler.) Example code for the Instruction Fetch states:

Address	Label	Instruction	Operands	Comments
0	IF0	DO	SELPC, Sel2=bus1, Load_ADD_R	PC $\rightarrow$ ADD_R
1	IF1	DO	Inc_PC	PC + 1$\rightarrow$ PC
2	IF2	DO	sel2=mem, Load_IR	RAM[ADD_R] $\rightarrow$ IR

1. Microcode for Simple CPU control (25 pts)

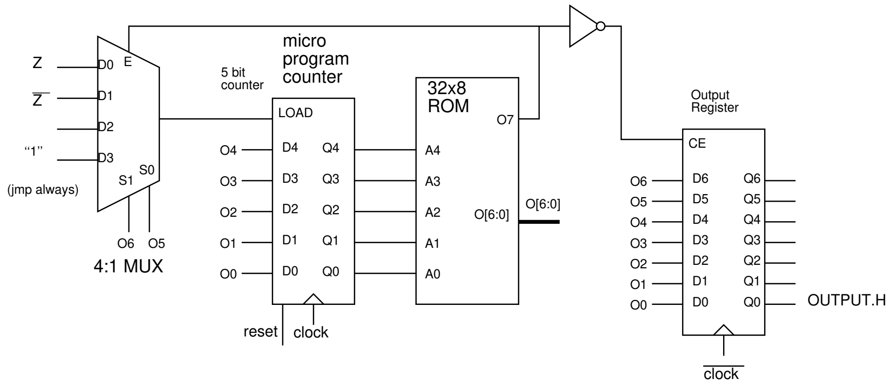
List, in symbolic form, the microcode needed to execute the *RDI* instruction from PS 8, problem 1.

2. Microcode for Simple CPU control (30 pts)

List, in symbolic form, the microcode needed to execute a new *DJNZ dst adr* instruction. The instruction decrements the contents of the destination register and branches to *adr* if the destination register is non-zero. Describe any necessary changes to the MCU.

3. Microcode for FSM emulation (25 pts)

In this problem you will emulate a Moore type FSM for a sequence recognizer, using the microprogrammed control unit (MCU) shown below. The MCU should assert OUTPUT once for every (possibly overlapping) sequence "011" or "110" detected in the synchronized input data stream Z. The MCU clock is 3 times as fast as the input bit rate of Z, thus you have time to execute three instructions for every input bit processed. Let Z, and $\overline{Z}$ be connected to D0, and D1 respectively on the 4:1 mux. Write a micro-program which will emulate the sequence recognizer listing your program in mnemonic and numeric form. (Note that branches only occur when test variables are asserted; do not add any inverters. Also note that OUTPUT may not necessarily change states on the same clock edge as Z changes, and OUTPUT could be asserted from one to three clock cycles.) Show a timing diagram with the output register OUTPUT, CLOCK, microPC LOAD, Output Register CE, and ROM O7 for the input sequence Z = 101101. Label each clock period with the current address (micro-program counter contents).



4. Pipelining (20 pts)

A Data path is being designed to calculate

$SAE_{n+1} = SAE_n + |I_1 - I_2| + |I_3 - I_4|$. I_1, I_2, I_3, I_4 are 8 bits wide. You are given 2 input N bit adder blocks, 8 bit absolute difference blocks, and registers. Draw a block diagram of a data path that maximizes throughput of this calculation. Calculate, using a timing diagram, maximum throughput for adder/abs. diff. delay of 10 ns, setup time for registers of 5 ns.