UNIVERSITY OF CALIFORNIA AT BERKELEY
COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

Fall 2003 Project
Final Check Off Instructions

Sign up for a group name and a check off slot, signup sheets are in the lab.

Make sure we can synthesize and compile your project in Synplify and Xilinx, using the standard tool flow. You may submit only *.V, *.EDN and other source files. No bitfiles, EDIFs or project files will be accepted or used. **WE WILL SYNTHESIZE AND COMPILE YOUR PROJECT. Details on file submission will be posted Thursday 11/20 by 5pm.**

We will constrain the clock to 27MHz, if you do no meet this constraint we don't care. Just make sure your project runs.

Arrive at LEAST 20min before your check off slot. If we are unable to compile your project YOU WILL LOSE POINTS! But if you are present you will get a chance to fix any problems and continue. **Rewriting verilog is NOT ALLOWED!**

If you fail early check off (if you project just doesn't work or has MAJOR bugs) you will be able to retry at regular check off. You will probably get the benefit of the doubt during early check off, it is to your advantage to check off early, even with a few minor bugs. Extra credit will compensate for a few minor bugs.

We will ask you a few questions during your check off. Think about challenges you overcame, problems you debugged, and those you still have. If there's a noticeable bug, tell us why you think its there. Better to state the bug (and the fix you didn't have time to implement) than to hope we won't notice. We will also ask about the exact BME you designed, what you do in a clock cycle, how many cycles per Kernel, that sort of thing, please come with answers, we expect you BOTH to know your project very well.

Project will be tested with:
Horizontal Moving Block
Vertical Moving Block
Spinning Wedges of various angles
Live Video
Static patterns

Features like a quality reset, and the ability to freeze frame will be appreciated. We will ask you to demo any additional features or shortcomings of your project. We will not ask about bugs we see, so if you want to explain them, you will need to do so. Think of this as a presentation of your project. Remember we expect you BOTH to know your project in detail, you should be able to explain clearly and precisely how your project works. If you broke the work between you, that's fine each partner can describe their part, but please don't rely on one person to do all the talking.