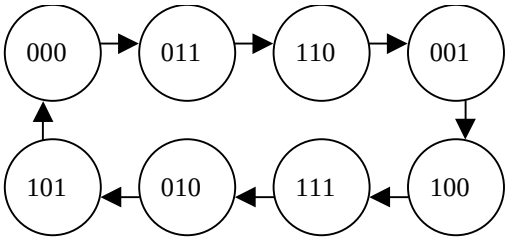
1. Counter Design

Counter Value	Q2 Q1 Q0
0	0 0 0
3	0 1 1
6	1 1 0
1	0 0 1
4	1 0 0
7	1 1 1
2	0 1 0
5	1 0 1
0	0 0 0

State Diagram:



State Transition Table:

Q2 Q1 Q0	NQ2 NQ1 NQ0
1 1 1	0 1 0
1 1 0	0 0 1
1 0 1	0 0 0
1 0 0	1 1 1
0 1 1	1 1 0
0 1 0	1 0 1
0 0 1	1 0 0
0 0 0	0 1 1

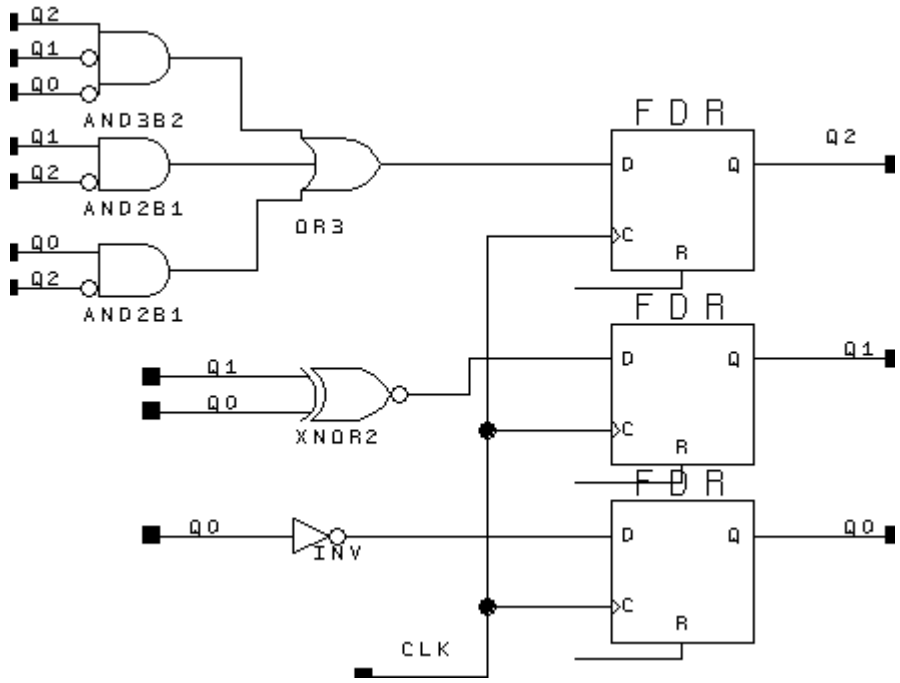
Q2 Q1 Q0 are the state variables.
NQ2 NQ1 NQ0 are the next state variables.

NQ2 = Q2 Q1’ Q0’ + Q2’ Q1 Q0 + Q2’ Q1 Q0’ + Q2’ Q1’ Q0 | sum of products
NQ2 = Q2 Q1’ Q0’ + (Q2’ Q1 Q0 + Q2’ Q1 Q0) + Q2’ Q1 Q0’ + Q2’ Q1’ Q0 | repeat Q2’ Q1 Q0 again
NQ2 = Q2 Q1’ Q0’ + (Q2’ Q1 Q0 + Q2’ Q1 Q0’) + (Q2’ Q1 Q0 + Q2’ Q1’ Q0) | rearrange terms
NQ2 = Q2 Q1’ Q0’ + Q2’ Q1 + Q2’ Q0 | simply

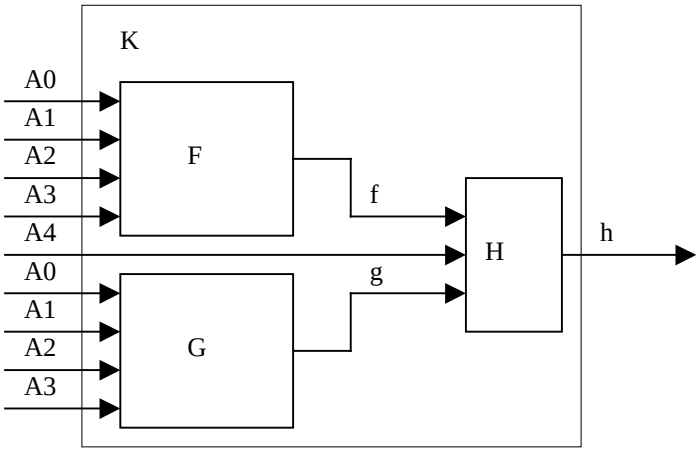
NQ1 = Q2 Q1 Q0 + Q2 Q1’ Q0’ + Q2’ Q1 Q0 + Q2’ Q1’ Q0’
NQ1 = Q1’ Q0’ + Q1 Q0
NQ1 = (Q1 XOR Q0)’ | inverse of (Q1 XOR Q0)

NQ0 = (Q2 Q1 Q0’ + Q2 Q1’ Q0’) + (Q2’ Q1 Q0’ + Q2’ Q1’ Q0’)
NQ0 = (Q2 Q0’ + Q2’ Q0’)
NQ0 = Q0’

Schematic Diagram:



2. Xilinx Combinational Logic Block
Input Variables = A4 A3 A2 A1 A0

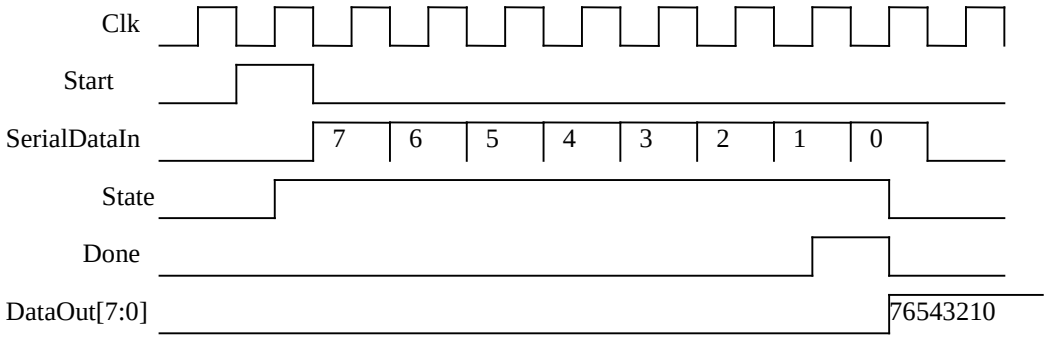


Proof:
h = H (f,A4, g)
one possible function for H is
h = A4 * f + A4' * g
f = F (A0, A1, A2, A3)
g = G (A0, A1, A2, A3)
➔ h = A4 * F(A0, A1, A2, A3) + A4' * G(A0, A1, A2, A3)
K(A0, A1, A2, A3, A4=1) = A4* F(A0, A1, A2, A3)
K(A0, A1, A2, A3, A4=0) = A4'* G(A0, A1, A2, A3)
➔ h = K(A0, A1, A2, A3, A4=1) + K(A0,A1,A2,A3,A4=0)
➔h = K(A0, A1, A2, A3, A4)

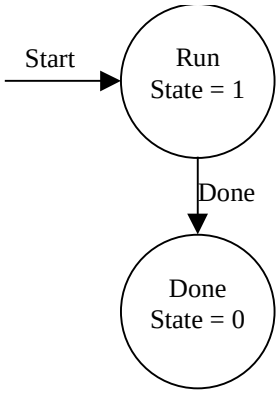
3. Serial-to-Parallel Converter

1. Specify the timing of the input and output signals (Start, SerialDataIn, Done, and DataOut[7:0]).
2. Specify the timing of the State signal for the FSM.
3. Follow the timing discipline by using all synchronous components in your design.
4. Design the data path first. Note: You can tie the reset of the SR8RE either to the Start signal or to the Ground.
5. Design the control path.

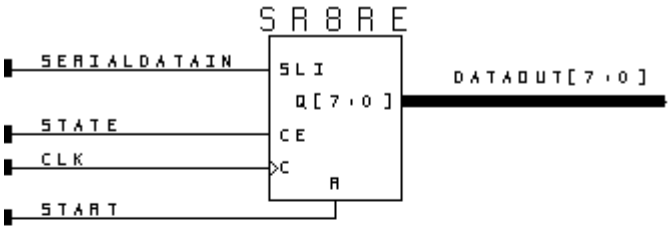
Timing Diagram:

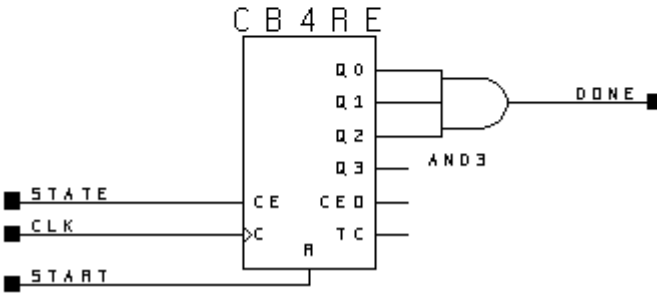
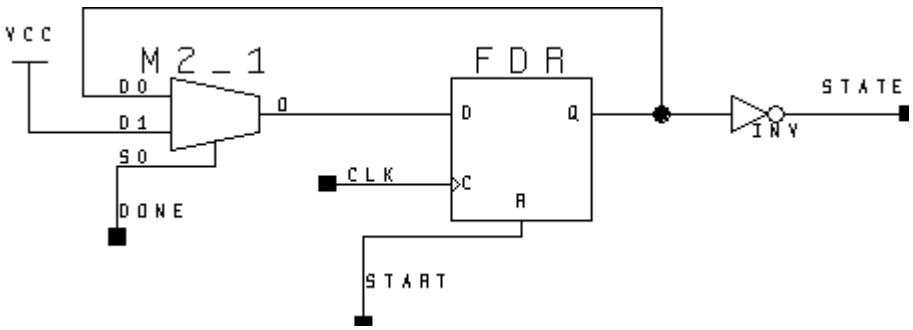


State Diagram:



Data Path:





Control Path: