UNIVERSITY OF CALIFORNIA

College of Engineering
Department of Electrical Engineering
and Computer Sciences

Professor Fearing Fall 1999

EECS 150 — FINAL EXAM

Thursday, 9 December 1999, 12:30-3:30 p.m.

Name: _____ ID#: _____

- Closed book. No notes. No calculators.
- There are 6 problems worth 100 points total. There is little room for partial credit—it's better to do half the test carefully than to do the entire test sloppily.

Problem	**Points**	**Your Score**
1	14	
2	6	
3	25	
4	28	
5	15	
6	12	
Total	**100**	

In the real world, unethical actions by engineers can cost money, careers, and lives. The penalty for unethical actions on this exam will be a grade of F in EECS150 and a letter will be written to the Department Chair and to the Office of Student Conduct.

Problem 1 (14 points)

[4 pts.] **a)** Find the minimal sum-of-products form for $Y = \sum(3, 6, 7, 8, 9, 10, 11, 15)$ using variables $A_3A_2A_1A_0$. (For example, minterm 3 = $\bar{A}_3\bar{A}_2A_1A_0$.)

Y = _____

[4 pts.] **b)** Find the minimal product-of-sums form for $Y = \sum(3, 6, 7, 8, 9, 10, 11, 15)$ using variables $A_3A_2A_1A_0$. (For example, For example, minterm 3 = $\bar{A}_3\bar{A}_2A_1A_0$.)

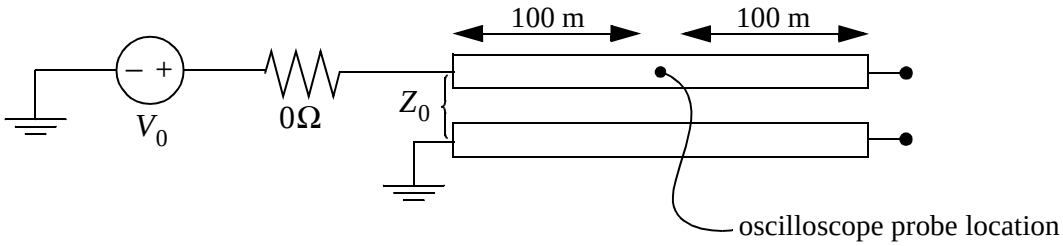
Y = _____

[6 pts.] **c)** *State minimization.* For the following state table, determine which states are equivalent.

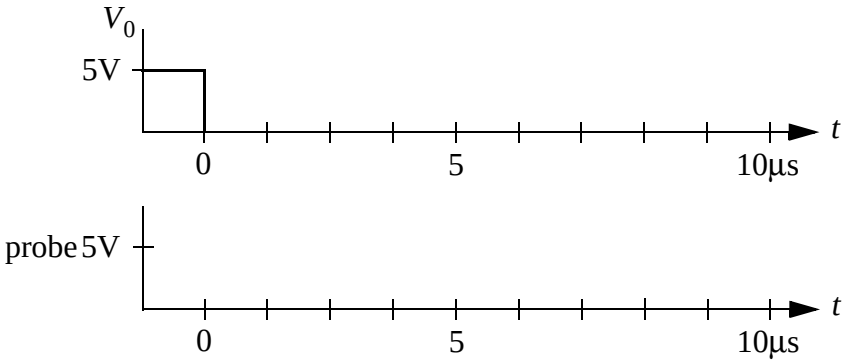
Present State	Input	Output	Next State
S0	**0**	**0**	**S0**
S0	**1**	**0**	**S1**
S1	**0**	**1**	**S0**
S1	**1**	**1**	**S1**
S2	**0**	**0**	**S2**
S2	**1**	**0**	**S3**
S3	**0**	**1**	**S2**
S3	**1**	**1**	**S3**
S4	**0**	**0**	**S2**
S4	**1**	**0**	**S0**
S5	**0**	**0**	**S0**
S5	**1**	**0**	**S2**
S6	**0**	**0**	**S4**
S6	**1**	**0**	**S5**

Problem 2 (6 points)

You are given a 200-meter length of cable with impedance 50 ohms and propagation velocity 2×10^8 m/s. The source end is driven with a 0-ohm impedance. The load end is open circuited. An oscilloscope probe (with 10-meg ohm input impedance) is connected to the cable 100 meters from the source, as shown below:

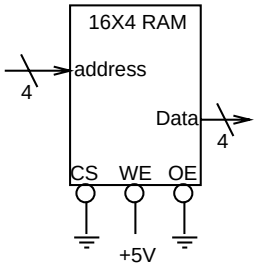


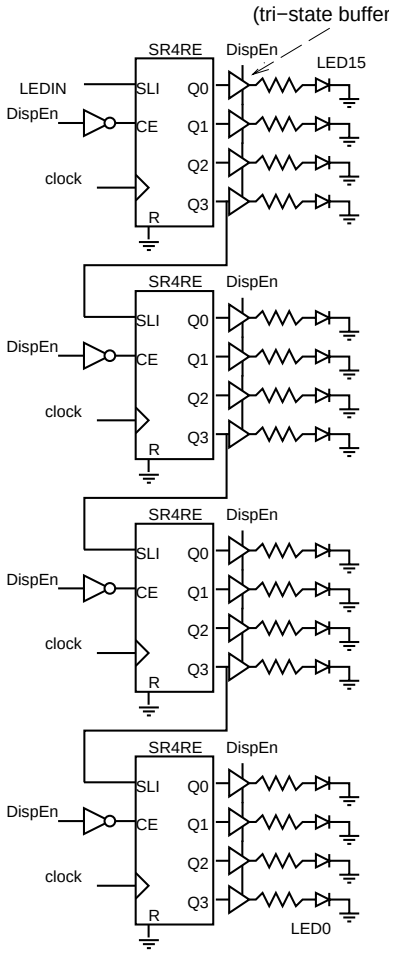
V_0 switches at time $t = 0$, as shown. Sketch the voltage seen on the oscilloscope for $0 < t < 10\mu s$. (V_0 is initially at 5V, $-\infty < t < 0$.)



Problem 3 Serial LED PWM Display (25 points)

In this problem, you will design the data path and controller state diagram for a 16-element LED display. The brightness of each LED is controlled by its duty cycle (using pulse width modulation), which is specified by a 4-bit value (0/15, 1/15, 2/15, ... , 15/15) stored in a 16×4 RAM. All components are driven by a 10MHz system clock. The data (on/off for each LED) is shifted into the display shift register in 1.6μs, then displayed for 24.0μs.





[11 pts.] a) Complete a detailed block diagram of the data path for the LED PWM Display, using up to three CB4RE synchronous binary counters, one COMPM4 4-bit magnitude comparator, and one COMP4 identity comparator. Note that CB4RE has both a TC output = $Q_3 \cdot Q_2 \cdot Q_1 \cdot Q_0$ and CEO = $TC \cdot CE$. Also, SR4RE shifts left.

Problem 3 (cont.)

[1 pts.] b) List the input signals to the data path that come from the control FSM.

[1 pts.] c) List the output signals from the data path that are inputs to the control FSM.

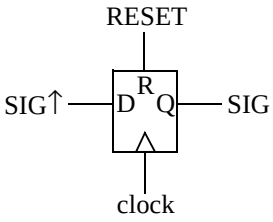
[10 pts.] d) Draw (a) state diagram(s) for a control FSM that will continuously turn on each LED for a fraction of time proportional to the value of its corresponding RAM location. (For example, if address 3 has contents 8, then LED3 should be on 8/15 of the display enable time.) Do not use more than 3 states. Ensure that FSM and data path start correctly.

[2 pts.] e) Why does the clock to the shift register need to be as fast as possible?

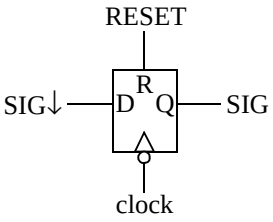
Problem 4 (28 points)

Using the data path on page 11, determine the appropriate timing diagram from page 9, and list in register transfer notation the operation(s) that is (are) occurring at the rising edge of the clock. Also, note where any bus conflicts occur. For clock edge 1.5, 2.5, 3.5, etc., list in RTN the operation occurring at the falling edge.

Consider that the FSM outputs may have glitches unless de-glitching flip flops are used. The notation for outputs is as follows: SIG output directly from FSM may have glitches, SIG↑ is passed through a rising edge-triggered DFF that generates a clean SIG, and SIG↓ is passed through a falling edge-triggered DFF that generates a clean SIG.



(please note: one clock cycle delay)



(please note: ½ clock cycle delay)

Assume that the clock is slow, say 1 MHz, but that outputs may be delayed from 0 to 100 ns because of routing delays. A BUFGS is used to prevent clock skew.

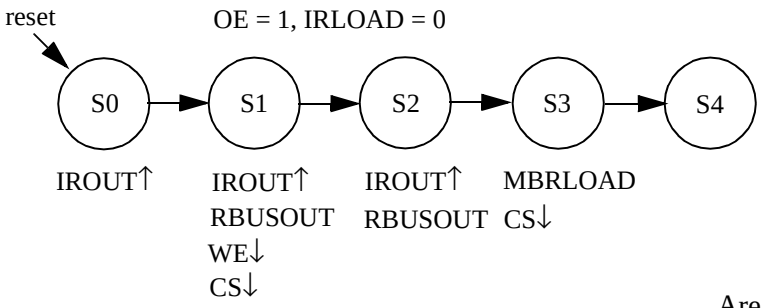
On clock edge 0, the FSM enters state S0; on clock edge 1, the FSM enters state S1, etc.

Assume that signals that are tied to “0” or “1” are glitch free. Assume worst case timing for register transfer operations.

Recall that WE over-rides OE for the static RAM in the data path. For all state diagrams, ALU operation is Y=B (ALU[1:0]=01). For RTN descriptions, assume worst case possibility.

Problem 4 (cont.) – Data paths

a.



timing diagram ☐ (from page 9)

clock edge 1: _____

clock edge 1.5:_____

clock edge 2: _____

clock edge 2.5:_____

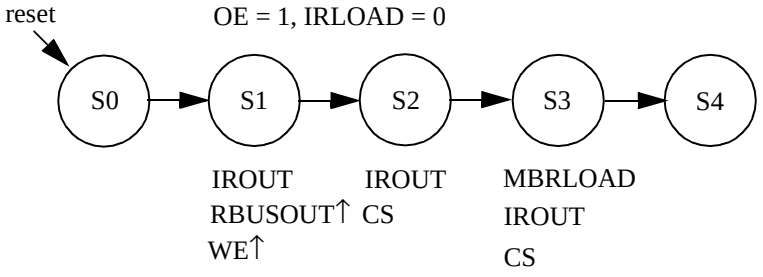
clock edge 3: _____

clock edge 4: _____

Are bus conflicts possible?

If yes, state where they occur:

b.



timing diagram ☐ (from page 9)

clock edge 1: _____

clock edge 2: _____

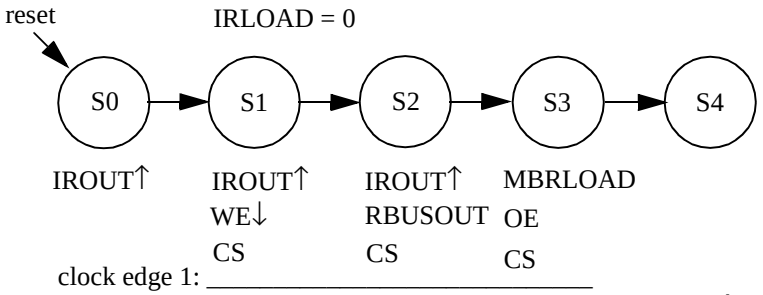
clock edge 3: _____

clock edge 4: _____

Are bus conflicts possible?

If yes, state where they occur:

c.



timing diagram ☐ (from page 9)

clock edge 1: _____

clock edge 1.5:_____

clock edge 2: _____

clock edge 2.5:_____

clock edge 3: _____

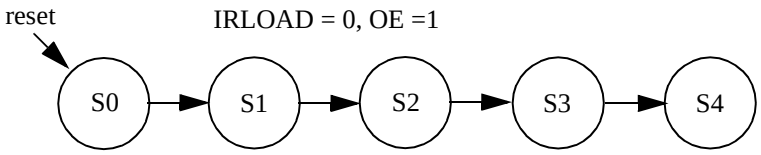
clock edge 4: _____

Are bus conflicts possible?

If yes, state where they occur:

Problem 4 – Data paths (cont.)

d.



IROUT↑ WE↑ | IROUT↑ CS↓ WE↑ RBUSOUT↑ | IROUT↑ | CS↓ MBRLOAD

timing diagram ☐ (from page 9)

clock edge 1: _____

clock edge 1.5:_____

clock edge 2: _____

clock edge 2.5:_____

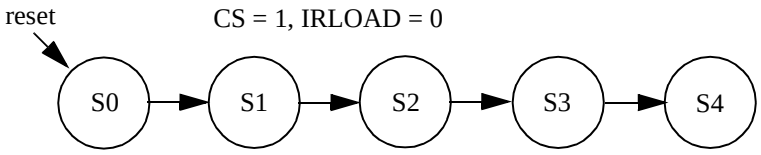
clock edge 3: _____

clock edge 4: _____

Are bus conflicts possible?

If yes, state where they occur:

e.



WE↓ IROUT | RBUSOUT IROUT | MBRLOAD OE IROUT

timing diagram ☐ (from page 9)

clock edge 1: _____

clock edge 1.5:_____

clock edge 2: _____

clock edge 2.5:_____

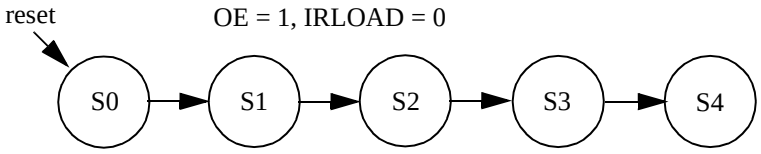
clock edge 3: _____

clock edge 4: _____

Are bus conflicts possible?

If yes, state where they occur:

f.



IROUT↑ | WE↑ CS↓ IROUT↑ | RBUSOUT IROUT↑ | MBRLOAD CS↓

timing diagram ☐ (from page 9)

clock edge 1: _____

clock edge 1.5:_____

clock edge 2: _____

clock edge 2.5:_____

clock edge 3: _____

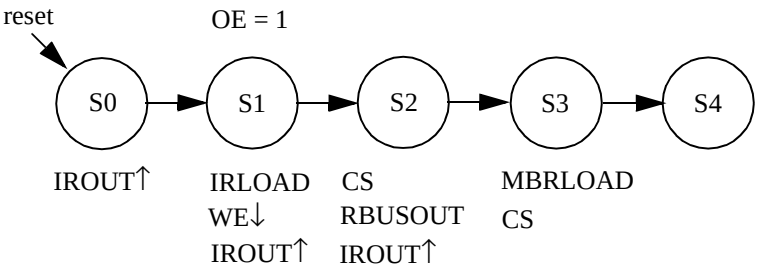
clock edge 4: _____

Are bus conflicts possible?

If yes, state where they occur:

Problem 4 – Data paths (cont.)

g.



timing diagram ☐
(from page 9)

clock edge 1: _____

clock edge 1.5:_____

clock edge 2: _____

clock edge 2.5:_____

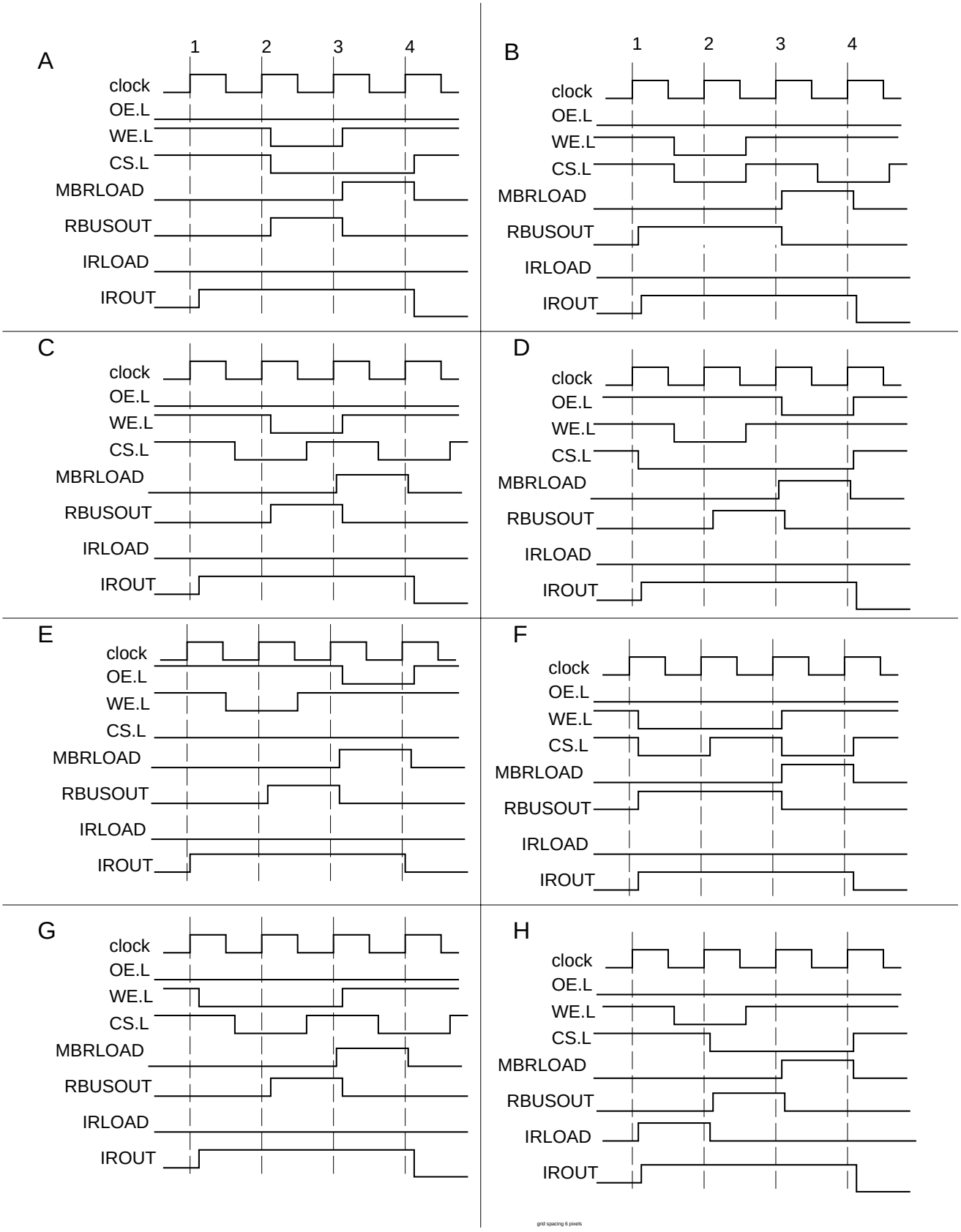
clock edge 3: _____

clock edge 4: _____

Are bus conflicts possible?

If yes, state where they occur:

Problem 4 – Timing Diagrams



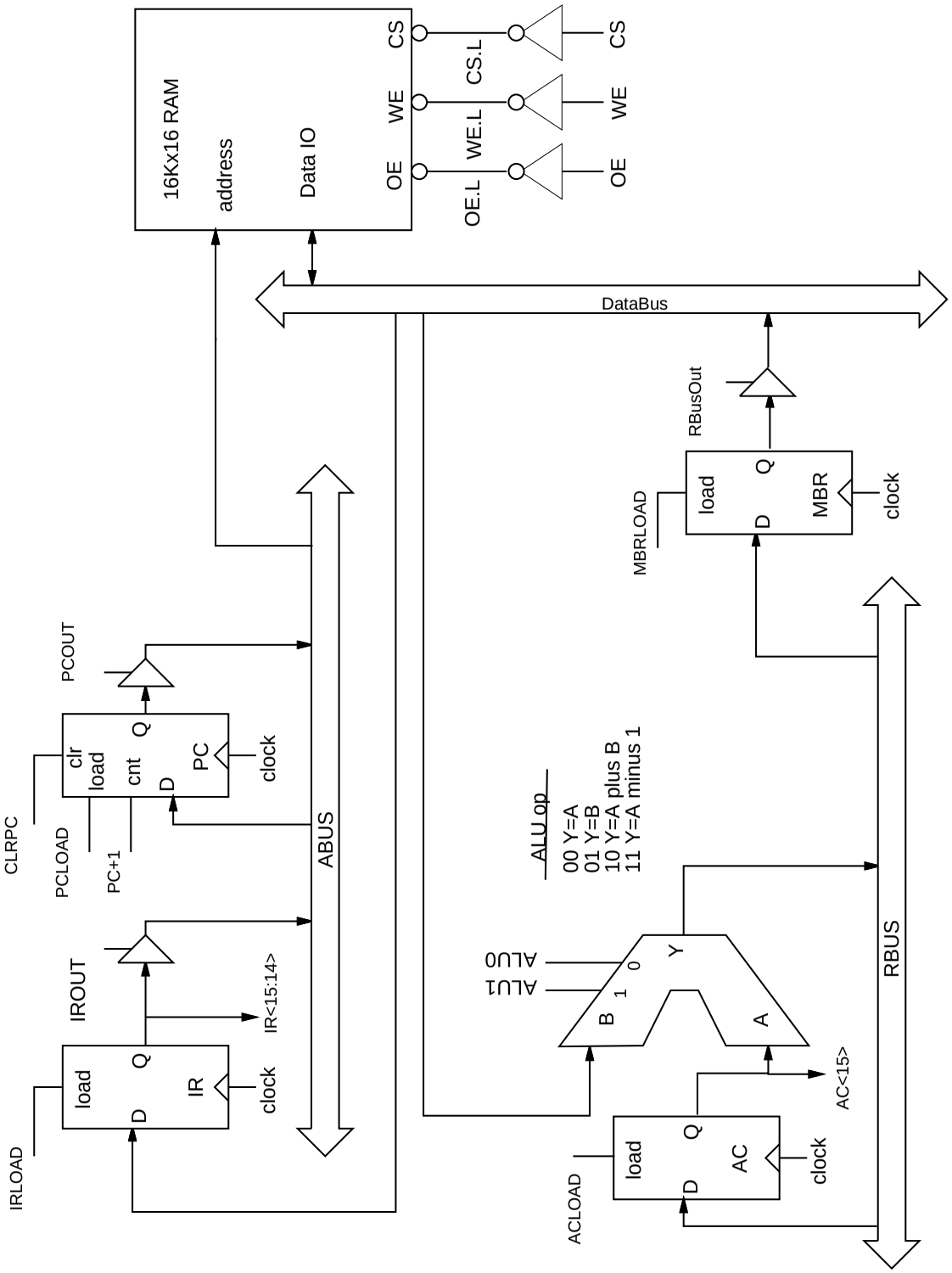
Problem 5 (15 points)

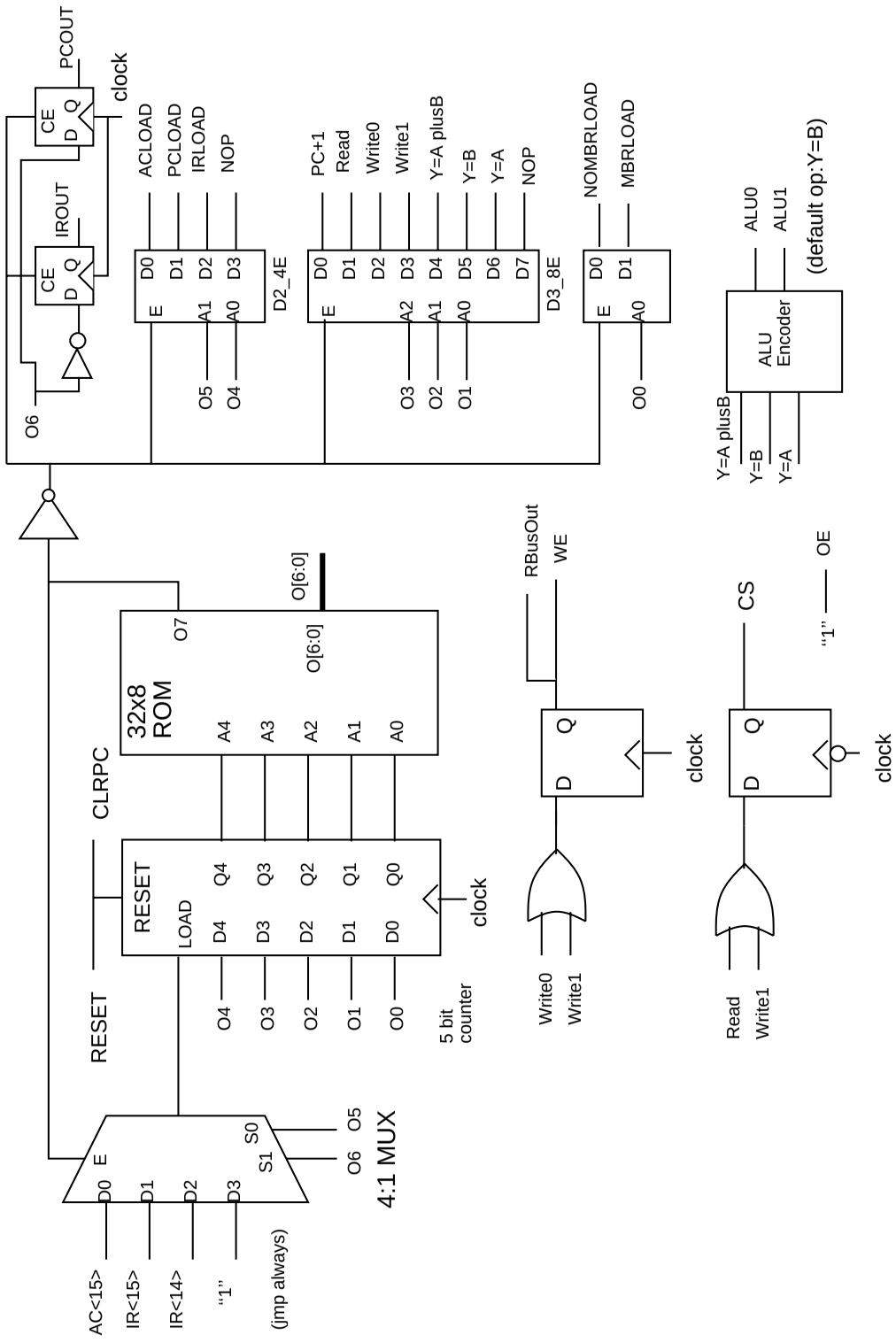
[12 pts.] a) Using the data path on page 11 and microprogrammed controller on page 12, write a microprogram, in symbolic form, to execute the following register transfer operations in the order listed:

RTN	**Microcode**
1) RAM[IR] → MBR	
2) RAM[PC] → IR	
3) MBR → RAM[IR]	
4) PC+1 → PC	

[3 pts.] b) Assuming the RTN in part (a) represents the execute portion of an instruction cycle, state in a sentence what assembly language instruction is being executed, e.g., ADD or LOAD or BRN or DJNZ or ?. (Assume the PC has already been incremented after the instruction fetch.)

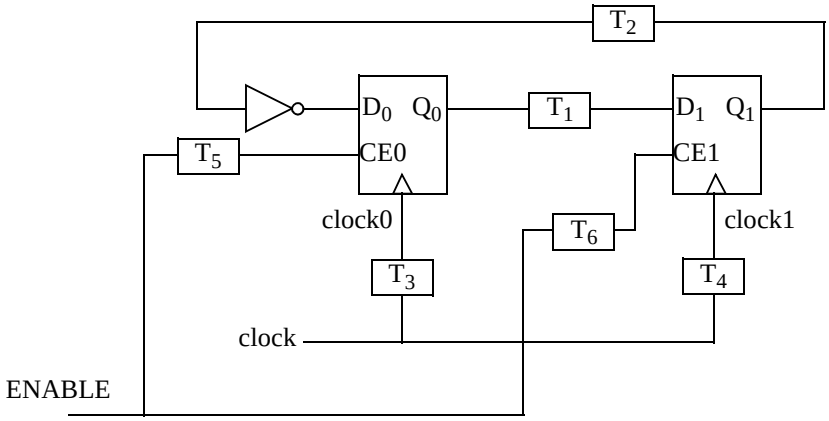
Problem 5 (cont.) – Data path




PCOUT
clock
CE
D Q
IROUT
ACLOAD
PCLOAD
IRLOAD
NOP
D2_4E
PC+1
Read
Write0
Write1
Y=A plusB
Y=B
Y=A
NOP
D3_8E
NOMBRLOAD
MBRLOAD
ALU0
ALU1
(default op:Y=B)
ALU Encoder
O6
O5
O4
O3
O2
O1
O0
Y=A plusB
Y=B
Y=A
O[6:0]
32x8 ROM
O7
A4
A3
A2
A1
A0
CLRPC
RESET
LOAD
Q4
Q3
Q2
Q1
Q0
5 bit counter
RBusOut
WE
Write0
Write1
CS
OE
"1"
Read
Write1
AC<15>
IR<15>
IR<14>
"1"
(jmp always)
4:1 MUX
S0
S1

Problem 6 FSM Microprogram Analysis (12 points)

Consider the given FSM: Each FF has setup time t_{su}, hold time t_{hld}, for D and CE inputs. Propagation delay for each FF is $\geq t_{ckoMIN}$ and $\leq t_{ckoMAX}$. Inverter delay is T_{INV}. t_{su} and t_{hld} are less than 10 ns.



[2 pts.] **a)** Assuming proper operation, draw the state diagram for the FSM, assuming $T_3 = T_4 = 0$ ns. Use notation for the state as $(Q_1\,Q_0)$.

Problem 6 (cont.)

[2 pts.] **b)** With ENABLE = 1, $T_3 = T_4 = 0$ ns, what is the minimum clock period? (Express algebraically.)

period ≥

[2 pts.] **c)** With $T_3 = T_4 = T_5 = 0$ ns, $T_6 = 50$ ns, and clock period = 100 ns, an asynchronous input ENABLE lasting 50 ns is input to the FSM. Estimate the chance of violating a setup or hold time on either FF, assuming uniform distribution of the ENABLE input change.

chance of violation:

[3 pts.] **d)** With $T_3 = T_5 = T_6 = 0$, and ENABLE = 1, what is the maximum T_4 for proper operation of the FSM?

$T_4 \leq$

[3 pts.] **e)** With $T_4 = T_5 = T_6 = 0$, and ENABLE = 1, what is the maximum T_3 for proper operation of the FSM?

$T_3 \leq$