University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Sciences

EECS 150   Spring 2000

Lab 6
Nasty Realities

1   Objectives

In this lab, you will learn about:

1. capacitive loading and its effect on propagation delays,
2. transmission lines and termination for long wires,
3. capacitive coupling on ribbon cables.

2   Prelab

All of the activity involved in this lab takes place in room 204B. Note that there is no way to work on this lab in advance, so read this write-up carefully so that you will know what to do when your lab section begins. If you are still confused, please get help from a TA *before* the start of your lab section.

3   Overview

Much of engineering is knowing what you can ignore. For example, we ignore the behavior of electrons in a digital circuit and think instead of 1's and 0's. This approximation has proven very successful, but it is important to know when we can no longer make it, or what to do to ensure that we can make it. Here are some of the assumptions we have been making:

- Wires are ideal – at any point in time, the voltage at every point on the wire is the same.
- There are exactly two logic levels – high and low.
- Transitions occur instantaneously from one voltage level to the next.

This lab is broken into two large experiments. Section 5 discusses the concepts of propagation delay and capacitive loading; Section 5.4 describes the associated experiment. Section 6 discusses the nasty realities of wires; Section 6.5 describes the associated experiment. Section 4 describes some of the miscellaneous things you need to know in order to build the circuits in this lab.

4   Details

4.1   Breadboard

We will use a breadboard to build the circuits for this lab. A breadboard is a slab of plastic, covered with holes connected in rows or columns by hidden metal contacts. By pushing stripped ends of wires, leads of discrete components or IC pins into these holes, we connect them electrically to anything in the same column or row.

The connections inside one section of the breadboard are shown in Figure 1a. Use the rows of connected holes for power and ground; use the columns for your circuit. Put chips horizontally, straddling the wide space separating the two columns of connections. Their pins should fit in the lowest row of the upper columns and the upper row of the lower columns.
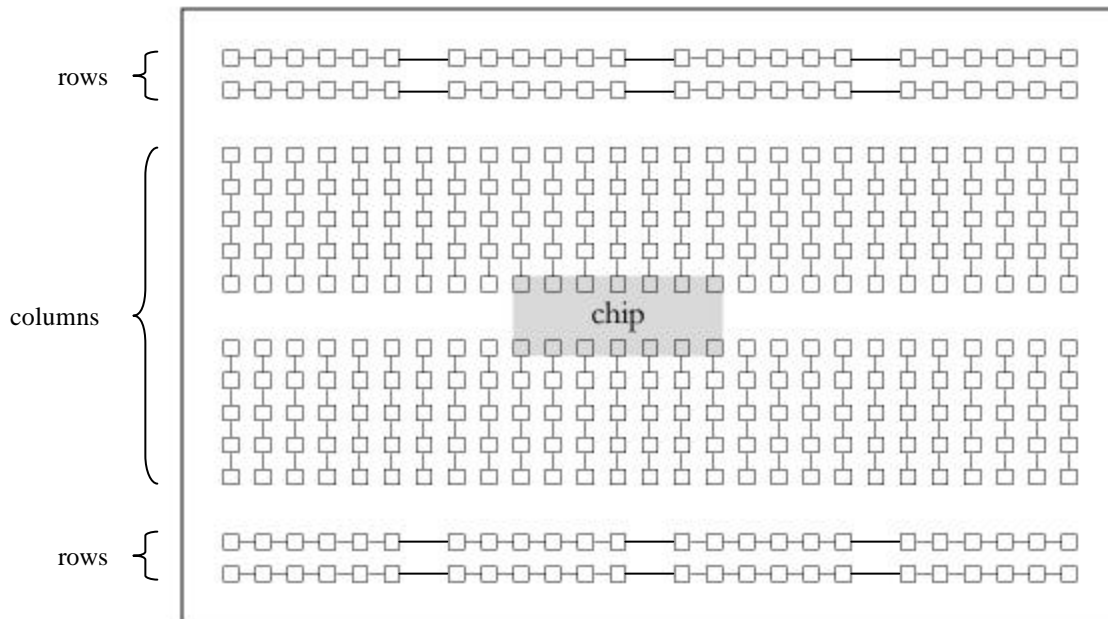

Figure 1a   Breadboard connections

Power the circuits in this lab with the HP E3630A power supply that we used in Lab 4. Connect it to the banana jacks attached to the breadboard, and run wires from the jacks to the breadboard's power/ground buses. Clamp the wires to the jacks by unscrewing the top of the jack, threading a stripped wire end into the exposed hole, and screwing down the top of the jack.

4.2   Ribbon Cable

Some of the circuits in this lab use a long (ten foot) ribbon cable, which is a flat strip of insulated parallel wires.   Adjacent wires in the cable alternate between connecting to the top and bottom pins of a 14-pin DIP connector, shown in Figure 1b (note, the figure actually shows a 16-pin configuration).
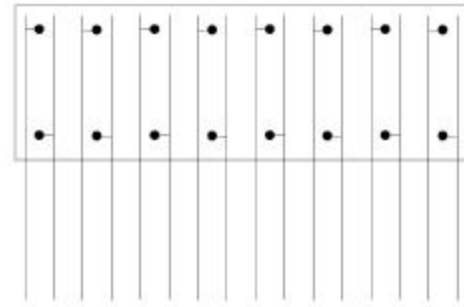
Figure 1b   Ribbon cable DIP plug

4.3   Resistors and Capacitors

Resistors are marked with a code consisting of three colored bands.   Each color corresponds to a number, as listed below.

Black	Brown	Red	Orange	Yellow	Green	Blue	Violet	Grey	White
0	1	2	3	4	5	6	7	8	9

The first two bands represent the first two digits of the resistance, and the third represents the number of zeroes following the first two numbers.   For example, a resistor labeled yellow-violet-red would be interpreted as 4700Ω, or 4.7 kΩ.   A fourth band, if present, represents the tolerance specification for the resistor value.   Gold indicates 5% tolerance and silver 10%.

Capacitors are labeled similarly, though usually with three digits rather than colored bands. The number printed is the number of picofarads (pF).   For example, a capacitor labeled "104" corresponds to 100000 pF, or 0.1 μF.

5   Transients and Delay Measurement

5.1   Propagation Delay

Contrary to what simulation software would have you believe, logic levels do not change instantaneously.   In reality, a transition from 0 to 5 V or vice-versa requires a gradual change from one voltage to the next.   What happens is that transistors switches on or off, charging or discharging a capacitor to produce the output voltage.

The propagation delay t_p of a gate defines how quickly its output responds to a change at its input.   Thus the propagation delay expresses the delay experienced by a signal when passing through a gate.   It is measured between the 50% transition points of the input and output waveforms.   Because a gate usually displays different response times for rising or falling input waveforms, two definitions of the propagation delay are necessary.   The t_{pLH} defines the response time of the gate for a low to high (or positive) output transition, while t_{pHL} refers to a high to low (or negative) transition.   Overall propagation delay is often defined as the average of t_{pLH} and t_{pHL}, but in this class we propagation delay more conservatively as the maximum of t_{pLH} and t_{pHL}.

5.2   Capacitive Loading

In a given logic family, the propagation delay of a gate is dependent largely on the capacitance that its output must drive. This means that if one gate tries to drive many others, its capacitive load will be large and propagation delay will increase. The incremental delay is directly related to the load capacitance. Each additional load adds a constant amount to the overall delay.

5.3   Ring Oscillator

A standard circuit for delay measurement is the ring oscillator, which consists of an odd number of inverters connected in a circular chain. Due to the odd number of inversions, this circuit does not have a stable operating point, so it oscillates. The period T of the oscillation is determined by the propagation time of a single transition through the complete chain, or $T = 2 \times t_p \times N$, where N is the number of inverters in the chain. The factor 2 results from the observation that a full cycle requires both a low-to-high and a high-to-low transition.

5.4   To Do

We will build a ring oscillator and observe the output on the oscilloscope, enabling us to calculate the t_p for a single inverter. We will then add additional capacitive loads on the individual inverters and observe the effect on the ring oscillator frequency.

1. Build the ring oscillator circuit in Figure 2a on your breadboard. Use a 74F04PC hex inverter chip, whose pinout is shown in Figure 2b. Remember to connect pin 14 to +5V and pin 7 to ground!
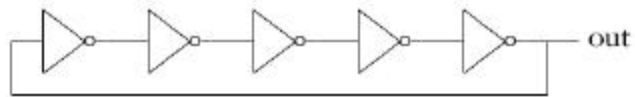

Figure 2a   5-stage ring oscillator

2. Using the oscilloscope, observe the output at pin 2, or equivalently at any of the five inverter outputs. Measure the period T of the ring oscillator and calculate the t_p for a single inverter. Record this value on the checkoff sheet and show your waveform to the TA. To really impress your TA, explain why the waveform looks more like a sine wave than a square wave.
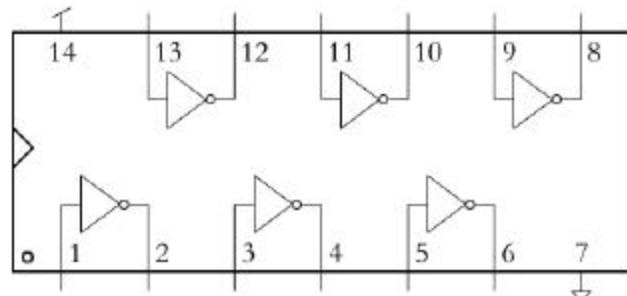

Figure 2b   74F04PC hex inverter pinouts

3. Connect a 100 pF capacitor from pin 4 to ground. What effect does this have on T? Now, connect additional load capacitors from pin 6 to ground, and pin 8 to ground. After adding each capacitor, measure the ring oscillator period. Record these three values on the checkoff sheet, and show that the relationship between load capacitance and propagation delay is roughly linear. Show your final waveform to the TA.

6 Wires

6.1 Nasty Realities

The nasty reality of wires is that they have so-called "parasitic" resistance, capacitance and inductance. Usually, these parasitics are small enough to be ignored, but their effect can dominate when a wire is long or when a high-speed signal is used.

Figure 3 is a model of these parasitics. The resistors are due to the wire conducting imperfectly, the capacitors are due to nearby conductors and the inductors are due to current in the wire producing a magnetic field.

Parasitic capacitance slows a wire's response to a sudden change in voltage, while parasitic inductance slows the response to a sudden change in current. Most digital logic lines conduct little current but require the voltage to change quickly. Power supply lines have the opposite problem – their voltage is constant, but they may need to provide a sudden burst of current when a large collection of signals change together (typically on a clock edge). Such current spikes limit the power supply's ability to maintain a constant voltage.

Together, inductance and capacitance make the wire behave like a *transmission line* with a *characteristic impedance* determined by the values of L and C. The characteristic impedance (abbreviated Z_0) is analogous to resistance but applies to dynamic rather than static signals. The hallmark of a transmission line is that signals propagate down its length at finite speed, so we can no longer treat the wire as having the same voltage everywhere.

A major problem with wires is their tendency to slow signals down – to roughly half the speed of light in a vacuum. This is not important at low frequencies but can become a problem at high frequencies. For a 1 GHz square wave clock, the signal will have the opposite phase just 8 cm (~3") away from the driving circuit! Circuit board designers routinely balance the lengths of clock lines on motherboards to ensure that all the logic circuits receive their clocks simultaneously.
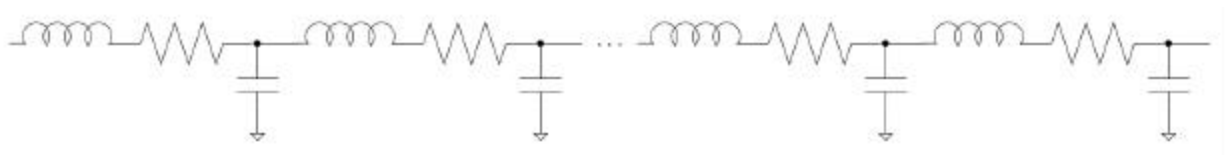

Figure 3 More realistic model of a wire

6.2 Transmission Line Termination

Accounting for the speed of signals is not the only difficulty with transmission lines. Any time a signal encounters a change in characteristic impedance, a fraction of the original signal is reflected back toward the source. The amount of reflection is proportional to the mismatch ratio of the two line segments. The same phenomenon occurs with visible light as it travels from air to glass to water. In wires, impedance mismatches can happen at connectors, when traces on the circuit board split, and most commonly, when the signal reaches its destination circuit.

Reflections are *never* good in digital logic – they always degrade the signal. The reflected signal is superimposed on the incoming signal, causing voltage overshoot, ringing, reduced rise

times, transition glitches, and bad karma. Reflections can cause double clock pulses, reduced timing margin, and even damage to chips in extreme cases.

Proper termination can eliminate reflections. Connecting a resistor with a value equal to the characteristic impedance of the transmission line is the simplest form of termination. This causes signals traveling along the transmission line to dissipate in the resistor, eliminating reflection. Ribbon cable (what you will use in today's lab) and twisted pair have a characteristic impedance of about 100Ω. RG-58 coaxial cable, which we used to connect the signal generator to the oscilloscope in Lab 4, has a characteristic impedance of 50Ω.

6.3 Capacitive Coupling

Capacitance exists between any and every pair of conductors, whether they are two wires in a cable or the space shuttle orbiting earth. The amount of capacitance is inversely proportional to the distance between the conductors and directly proportional to the amount of conductor (wire) in the pair of interest.

In cables, too much capacitance is a problem for two reasons: it reduces the characteristic impedance, making it harder to drive the cable, and it contributes to the coupling of signals between pairs of wires.[1] This coupling, or *crosstalk*, degrades the signal quality, lowering the maximum usable frequency for a given cable.

The traditional remedy for crosstalk is to reduce the capacitive coupling by mechanical means (conductor size, separation and dielectric constant) or by placing an electrostatic shield between the conductors, as described in Section 6.4. In cases where there is a mathematical model for the crosstalk, fast processors running clever algorithms can reverse the effect. This is exactly what's being done with DSL, where the phone companies are sending megabits/second of data over lines that "traditionally" would only support 56 kb/s.

6.4 Shielding

The most common way to reduce capacitive coupling is to surround the conductor of interest with a metal shield. Coaxial cable is the best example – the inner conductor is insulated and encircled by the grounded shield. Although there is capacitive coupling between the two conductors, the shield prevents the inner conductor from affecting any neighboring signal conductors. The problem with coaxial cables is that they are big and expensive.

Fortunately, partial shielding is often sufficient. Placing a grounded wire between two signal-carrying wires in a ribbon cable is a simple form of incomplete shielding that works well in practice.

6.5 To Do

1. Disconnect your ring oscillator circuit and hook up a 1 MHz 0-3V square wave from the 8112A pulse generator to the pin 1 of the hex inverter (or equivalently, to any inverter input). Hook up 50Ω from this pin to ground – this presents the proper load to the pulse generator so that the voltage you set is the voltage you get. Use four 200Ω resistors in parallel rather than

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[1] Inductive coupling also exists, but it is insignificant compared to capacitive coupling.
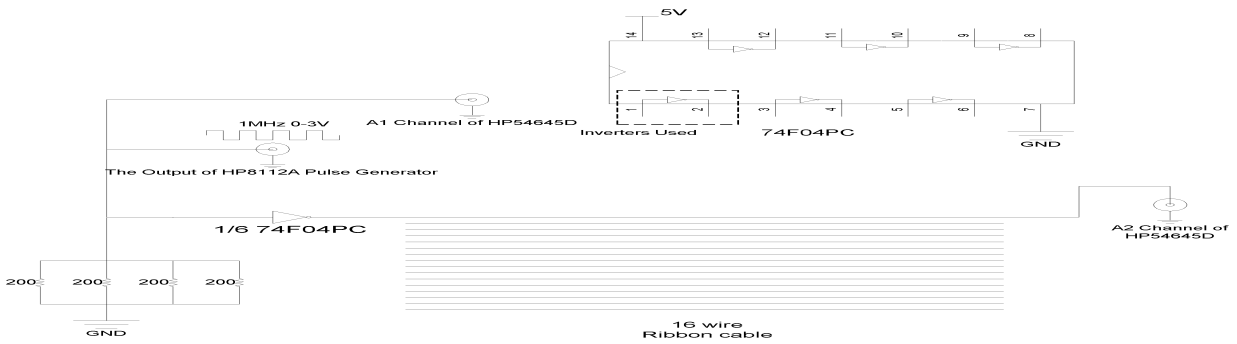
Figure 5 Schematic for Sec. 6.5.1-2

a single 50Ω resistor. Connect the output of the inverter to one of the wires on the ribbon cable. Refer to Figure 5 for schematic.

2. Using the oscilloscope, measure the signal at the inverter input on channel 1, and measure the signal at the opposite end of the ribbon cable on channel 2. Use the metal base of the breadboard as a common ground for both your oscilloscope probes and the pulse generator. Compare the two signals – ideally, the signal at the end of the ribbon cable would be a perfect inversion of the square wave. Is this the case? Why or why not?

3. Measure the peak-to-peak voltage V_{pp} (including any overshoot) for the high-to-low as well as low-to-high transitions on channel 2. Given that the output range of the 74F04 is approximately 0-3V, comment on the V_{pp} measured at the end of the transmission line. Record your measurements on the checkoff sheet and show the waveform to the TA.

4. Terminate the transmission line by placing two resistors at the end of the ribbon cable – 330Ω to V_{CC} and 200Ω to ground. Since these resistors are being placed in parallel with respect to the transmission line, the effective resistance is about 125Ω. This value is sufficiently close to the characteristic impedance of the ribbon cable (100Ω) for our purposes. How does this termination affect the waveform? Measure the new V_{pp}, record it on the checkoff sheet, and show the waveform to the TA. Refer to Figure 6 for schematic.
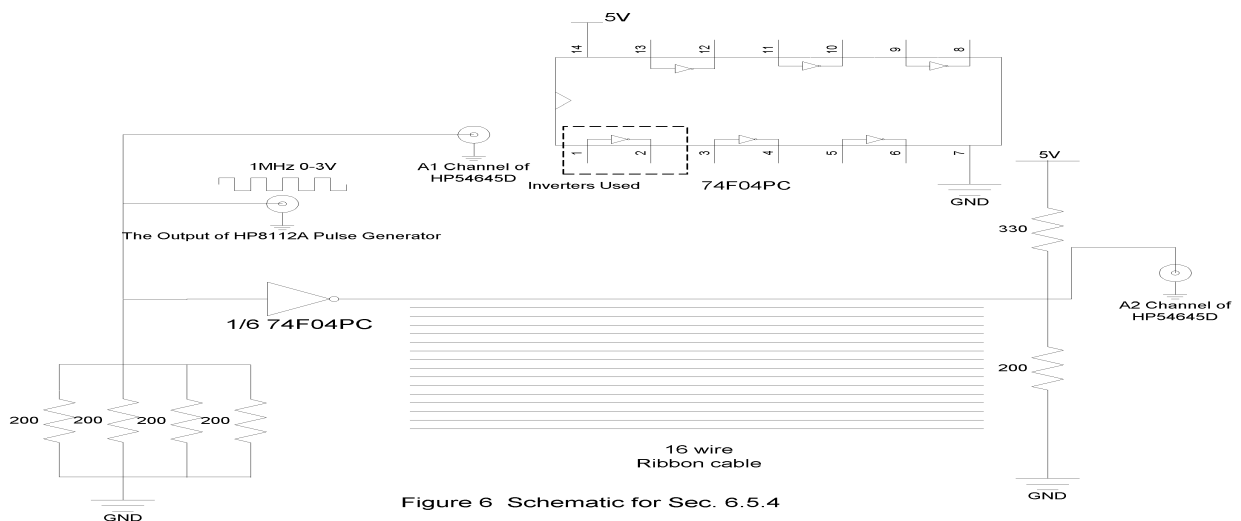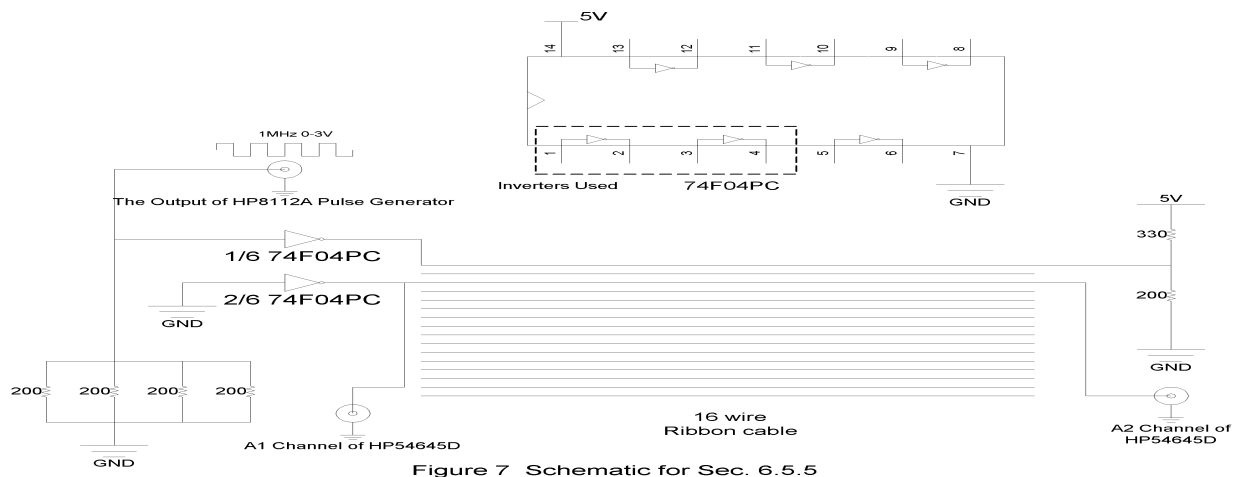

Figure 6 Schematic for Sec. 6.5.4

Figure 7 Schematic for Sec. 6.5.5

5. Leaving the rest of the circuit intact, select an unused inverter and connect its input to ground. Then connect its output, which should be V_{CC} (a DC signal), to the input of a wire two steps over (refer to Figure 1b to see how the pins correspond to the physical layout of the wires). You will now have a square wave on one wire and V_{CC} on another, with one wire between them carrying no signal. On the oscilloscope, simultaneously display the V_{CC} signal at each end of the cable (use either a 2V or 5V scale on both channels). Your source waveform should be a fairly clean 5V signal, but the signal at the other end should display some oscillation. Explain why this happens. Refer to Figure 7 for schematic.

6. Finally, connect the wire carrying no signal to ground, thus introducing a shield between the two signals. How does this affect the settling time and overshoot of the V_{CC} signal's oscillation? Show the TA the difference in the two waveforms and explain what is happening. Refer to Figure 8 for schematic.

7 Acknowledgements

5V

14 13 12 11 10 9 8

1MHz 0-3V

Inverters Used   74F04PC

1   2   3   4   5   6   7

GND

The Output of HP8112A Pulse Generator

5V

330

1/6 74F04PC

2/6 74F04PC

GND

200

16 wire
Ribbon cable

GND

200 200 200 200

GND

A1 Channel of HP54645D

A2 Channel of
HP54645D

Figure 8 Schematic for Sec. 6.5.6

7   Checkoff

1. Ring oscillator built (unloaded), waveform displayed on oscilloscope   **TA:** _____ (25%)

    t_p = _____

2. Capacitive loads added to ring oscillator, final waveform displayed on
    oscilloscope

    100 pF: $T_{overall}$ = _____

    200 pF: $T_{overall}$ = _____

    300 pF: $T_{overall}$ = _____   **TA:** _____ (20%)

3. Square wave measured at end of ribbon cable

    V_{pp} (high-to-low transition) = _____

    V_{pp} (low-to-high transition) = _____

    Explanation?   **TA:** _____ (20%)

4. Square wave measured at end of terminated ribbon cable, waveform displayed
    on oscilloscope

    V_{pp} = _____   **TA:** _____ (20%)

5. Waveforms of V_{CC} with and without shielding displayed on oscilloscope

    Explanation?   **TA:** _____ (15%)

6. Turned in on time   **TA:** _____ (full credit)

7. Turned in up to one week late   **TA:** _____ (half credit)