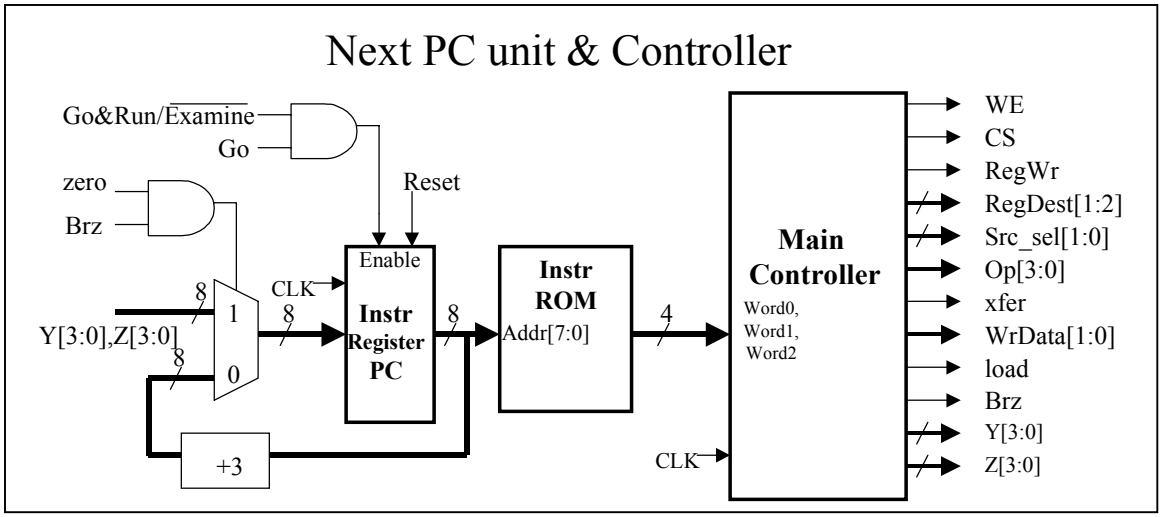
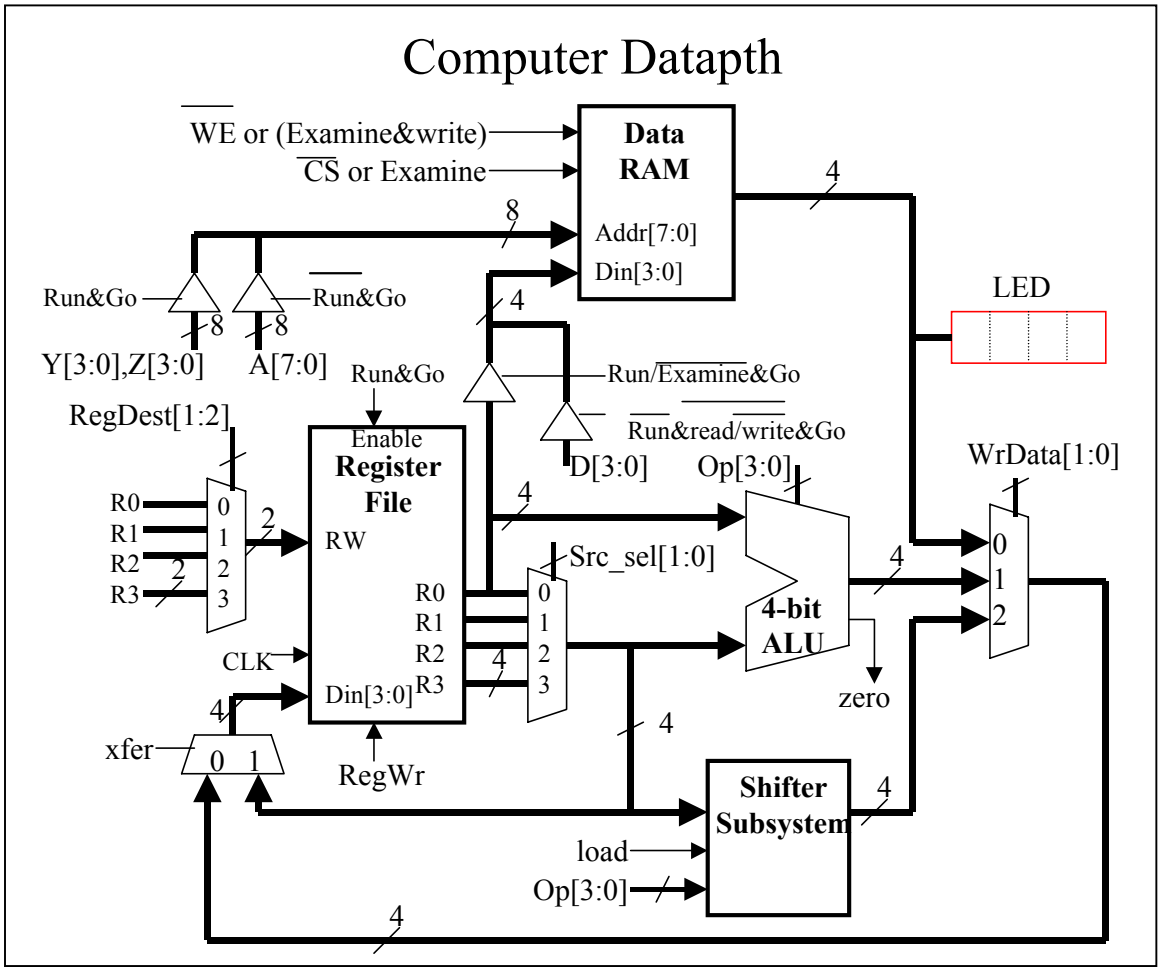
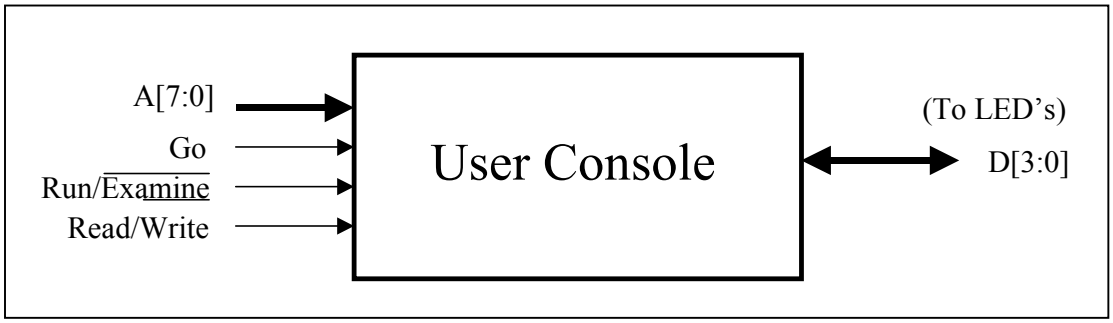
CS 150 Problem Set# 10/11 Solutions Wen Hui Guan

1. Processor Datapath
   Additional assumptions:
   a. It's a single-cycle processor implementation
   b. Each instruction fetch requires burst reading 3 sequential words from the instruction ROM based on the current PC
   c. Register decoding is done by the controller from the first or second words read, depending on the decoded instruction.
   d. The machine starts once the Go button is pressed







2.

Controller Output Signals

Control Signals		RegWr	RegDest	Src_sel	Op <3:0>	Load	WrData <1:0>	Brz	WE	CS	Xfer
Instructions	**ADD**	1	0	R[x1x0]	00xx	x	01	0	0	0	0
	NAND	1	0	R[x1x0]	01xx	x	01	0	0	0	0
	LSR	1	0	0	1000	1	10	0	0	0	0
	LSL	1	0	0	1001	1	10	0	0	0	0
	ASR	1	0	0	1010	1	10	0	0	0	0
	RSL	1	0	0	1011	1	10	0	0	0	0
	Xfer	1	R[y3y2]	R[y1y0]	1100	x	x	0	0	0	1
	LOAD	1	0	x	1101	x	0	0	0	1	0
	STOR	0	x	x	1110	x	x	0	1	1	x
	BRZ	0	x	0	1111	x	x	1	0	0	x

Register Transfer Operations

Transfer Operations	*Control Signals*
R[0] ← R[0]	RegDest = 00, Src_sel = 00, xfer=1
R[0] ← R[1]	RegDest = 00, Src_sel = 01, xfer=1
R[0] ← R[2]	RegDest = 00, Src_sel = 10, xfer=1
R[0] ← R[3]	RegDest = 00, Src_sel = 11, xfer=1
R[1] ← R[0]	RegDest = 01, Src_sel = 00, xfer=1
R[1] ← R[1]	RegDest = 01, Src_sel = 01, xfer=1
R[1] ← R[2]	RegDest = 01, Src_sel = 10, xfer=1
R[1] ← R[3]	RegDest = 01, Src_sel = 11, xfer=1
R[2] ← R[0]	RegDest = 10, Src_sel = 00, xfer=1
R[2] ← R[1]	RegDest = 10, Src_sel = 01, xfer=1
R[2] ← R[2]	RegDest = 10, Src_sel = 10, xfer=1
R[2] ← R[3]	RegDest = 10, Src_sel = 11, xfer=1
R[3] ← R[0]	RegDest = 11, Src_sel = 00, xfer=1
R[3] ← R[1]	RegDest = 11, Src_sel = 01, xfer=1
R[3] ← R[2]	RegDest = 11, Src_sel = 10, xfer=1
R[3] ← R[3]	RegDest = 11, Src_sel = 11, xfer=1

3. Controller (Moore Machine implementation)
   Outputs are control signals to the datapath.