

**University of California at Berkeley**  
**College of Engineering**  
**Department of Electrical Engineering and Computer Science**

EECS 150  
Spring 2001

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**Problem Set # 2 (Assigned 25 January, Due 2 February)**

1. Simplify the following expressions using the laws and theorems of Boolean Algebra:
  - (a)  $W(A,B,C) = A' B C' + A' B C + A B' C' + A B' C$
  - (b)  $X(A,B,C) = A' B' C' + A' B C + A B' C' + A B C$
  - (c)  $Y(A,B,C,D) = A' B' C' D' + A' B' C' D + A' B' C D' + A' B' C D + A B' C' D' + A B' C D'$
2. Use K-maps on the expressions of Problem 1. Show your work in K-map form. For 1(a)-(c):
  - (a) Find the minimized sum of products form.
  - (b) Find the minimized product of sums form.
  - (c) Find the minimized sum of products form of the function's complement.
  - (d) Find the minimized product of sums form of the function's complement.
3. Consider the following multilevel Boolean expressions:
  - (i)  $F(A,B,C,D,E) = (((A B) + C)(D + E)) + (A' D')$
  - (ii)  $G(A,B,C) = (A B C')$ ;  $H(A,B,C,D) = (D + G) G'$Perform the following:
  - (a) Show how to implement each function as a multilevel NAND only gate level implementation.
  - (b) Repeat (a), but using NOR gates only.
  - (c) Find the two level minimized Sum of Products forms.
  - (d) Find the two level minimized Products of Sums forms.
  - (e) Briefly compare the implementation complexities in terms of gates and literals. For each function, which achieves the "simplest" implementation.
4. Develop a minimized Boolean implementation of a "ones count" circuit that works as follows. The subsystem has four binary inputs A, B, C, D, and generates a 3-bit output, XYZ. XYZ is 000 if none of the inputs are 1, 001 if one input is 1, 010 if two are one, 011 if three inputs are 1, and 100 if all four inputs are 1.
  - (a) Draw the truth tables for XYZ (A, B, C, D).
  - (b) Minimize the functions X, Y, Z using 4-variable K-maps. Write down the Boolean expressions for the minimized Sum of Products form of each function.
  - (c) Repeat the minimization process, this time deriving Product of Sums form.
5. Consider a combinational logic subsystem that performs a two-bit addition function. It has two 2-bit inputs A B and C D, and forms the 3-bit sum X Y Z.
  - (a) Draw the truth tables for XYZ(A,B,C,D).
  - (b) Minimize the functions using 4-variable K-maps to derive minimized Sum of Products forms.
  - (c) In your textbook and in class we have introduced the Full Adder circuit. What is the relative performance to compute the resulting sum bits of the 2-bit adder compared to two full adders connected together? (Hint: which has the worst delay in terms of gates to pass through between the inputs and the final outputs, and how many gates is this?).
6. EXTRA CREDIT: Generalize Problem 5 by adding a fifth input, CIN (carry in) and a fourth output COUT (carry out). Minimize the three sum bit functions and the COUT function using 5-variable K-maps. WARNING: Not for the faint of heart!