University of California at Berkeley
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EECS 150 R. H. Katz
Spring 2001

Problem Set # 5 (Assigned 22 February, Due 2 March)

1. In lecture, we presented an R-S latch based on cross-coupled NOR gates. It is also possible to construct an R'-S' latch using cross-coupled NAND gates.
   (a) Draw the R'-S' latch, labeling the R' and S' inputs and the Q and Q' outputs.
   (b) Show the timing behavior across the four configurations of R' and S'. Indicate on your timing diagram the behavior in entering and leaving the forbidden state when R'=S'=0.
   (c) Draw the state diagram that shows the complete input/output and state transition behavior of the R'-S' latch.
   (d) What is the characteristic equation of the R'-S' latch.
   (e) Draw a simple schematic for a gated R'-S' latch with an extra enable input, using NAND gates only.
2. In lecture, we presented a Master-Slave flip-flop using R-S latches in the master and slave stages. Consider an alternative implementation that uses R'-S' latches instead.
   (a) Draw the circuit schematic for the Master-Slave flip-flop constructed in this way.
   (b) Does the flip-flop implemented in this way suffer from the ones catching problem? Explain why or why not.
   (c) Does the flip-flop implemented in this way suffer from the zeros catching problem? Explain why or why not.
3. Consider a new (and slightly weird) kind of flip-flop dubbed the A-B flip-flop. When A and B are identical, the flip-flop resets. When A and B are different, the flip-flop sets.
   (a) Give an excitation table and characteristic equation for the A-B flip-flop.
   (b) Show how to implement an A-B flip-flop with a D flip-flop.
   (c) Show how to implement a D flip-flip using an A-B flip-flop.
   (d) Show how to implement an A-B flip-flop with a J-K flip-flop.
   (e) Show how to implement a J-K flip-flop using an A-B flip-flop.
4. In lecture, we presented a positive edge-triggered D flip-flop using NOR gates.
   (a) Show how to implement such a function using NAND gates only.
   (b) Explain the timing behavior of this circuit, showing with a timing diagram how the edge-triggering works.
   (c) How should you modify the circuit to become negative edge-triggered?
   (d) Modify your timing diagram to explain how the circuit works with negative edge-triggered.