

University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Science

EECS 150
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R. H. Katz

Homework Quiz # 4 (16 February)

Name: _____ **SID:** _____

You are to design a simple combinational subsystem to the following specification. The system has the ability to pass its inputs directly to its outputs when a control input, S , is not asserted. It interchanges its inputs when the control input S is asserted. For example, given four inputs A, B, C, D and four outputs W, X, Y, Z , when $S=0$, $WXYZ=ABCD$ and when $S=1$, $WXYZ=BCDA$.

Show how to implement this functionality using building blocks that are restricted to be 2:1 multiplexers and 2:1 demultiplexers. Draw your solution below, using black boxes for the mux/demux blocks.

