

LAB 3 Finite State Machines On Xilinx

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OVERVIEW

- ◆ Schematics capture and simulation (lab 2)
- ◆ Add IO interface components
- ◆ Map netlists to implementation
- ◆ Download circuits to Xilinx board
- ◆ Debugging

Things to do before lab

- ◆ Have a working version of lab 2
- ◆ Make sure that the necessary signals are in BUS form.
- ◆ Finish the prelab questions for lab 3

Copy Lab 2

- ◆ Open Lab 2
- ◆ Go to FILE->COPY PROJECT and resave Lab 2 as Lab 3
- ◆ Open the new Lab3 project
- ◆ Now you can build on it.

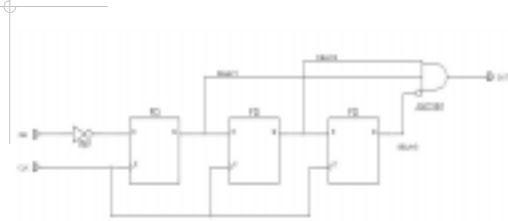
Xilinx IO

- ◆ Interface components
 - IPAD OPAD
 - BUFG OBUF
 - IBUF
- ▶ Debounce circuit ensures ENTER and RESET go high for exactly one clock cycle

Debounce Circuit

- ◆ After pressing a mechanical switch once, without debouncing the arcing between the two contacts might "make or break" the connection several times before it settles into the desired position.
- ◆ This can result in erratic behavior in the circuit.

The Debounce Circuit



The interface has been done for you

- ◆ You DO NOT need to do your own interface for lab 3
- ◆ You DO need to add the library under `u:\cs150` to your projects
- ◆ The name of the library is "Library"
- ◆ A macro called IO contains all of the interface components you need for the lab.

TA library suggestion

- ◆ **PROBLEM:** When you try to access the library there are access problems
- ◆ This happens when too many people try to access the file at once
- ◆ You should COPY the library to your own directory BEFORE you add it.

Implementation

- ◆ Open the project window and click on implementation
- ◆ If implementation is successful, the PROGRAMMING block turns black.

Implementaion Tip

- ◆ If you want to reimplement, it is a good idea to clear the implementaion data from the last implementation.
- ◆ This is done in PROJECT->CLEAR IMPLEMENTATION DATA on the Project Manager screen.

Downloading Circuit

- ◆ Power up the board
- ◆ Attach the Xchecker cable
- ◆ Be careful of the orientation of the cable and the delicate pins
- ◆ Click on the programming box in the Project Manager (below implementation)
- ◆ When the window pops up, choose Hardware Debugger

Communication Problems

- ◆ Make sure that the board has power
- ◆ Make sure that the Xchecker is hooked up correctly
- ◆ Make sure that the cable is configured correctly. It should be Xchecker on Com1.

Test Circuit

- ◆ The NUMLED on the right displays the state of the FSM
- ◆ NUMLED displays the state in hex
- ◆ State only has 3 bits, but hex needs 4 bits.
- ◆ State3 (MSB) is wired to ground.

More Test Circuit

- ◆ Make sure that sw4-7 is closed.
- ◆ Start the clock in the Hardware Debugger
- ◆ Watch the internal signals in the Hardware Debugger