University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Sciences

EECS150 J. Wawrzynek
Spring 2002

Homework #3

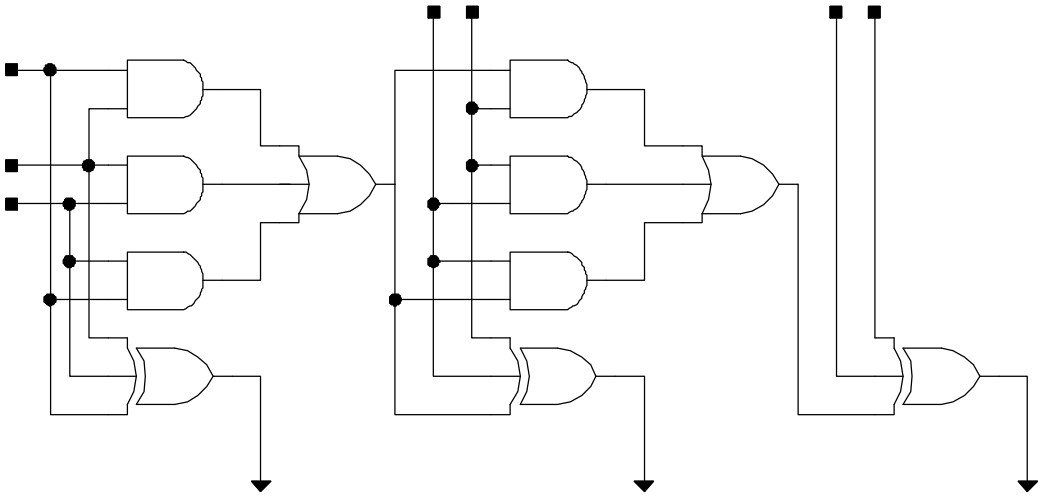
This homework is due on **Friday February 15th by 11am**. Homework will be accepted in the EECS150 box on the door to room 218 Cory Hall. Late homework will be penalized by 50%. No late homework will be accepted after the solution is posted.

1. As a design engineer for the digital engine control system for a new automobile, you are asked to choose an implementation technology (discrete gates, custom ICs, microprocessors, or FPGA's).
   a) Rank order each technology with respect to 1) NRE cost, and 2) manufacturing cost.
   b) What combination of the above technologies would you decide to use? Discuss the tradeoffs you considered.

2. Read the online Xilinx Data book (check the class website) pages 6-9 - 6-35. You will probably not understand everything in the data book, but do your best.
   a) Based on Figure 1 for the simplified block diagram of the CLB, estimate the number of *configuration bits* needed to configure a CLB. Remember configuration bits are used to set all internal multplexors and fill in the tables in the LUTS.
   b) Referring to Figure 15, what is the purpose of the “Passive Pull-up / Pull down” circuitry? ie. Why is it included?

3. Draw a simple diagram that shows how you could construct a *5-LUT* from a collection of *4-LUTs*. Is there a simpler way to do this if you where allowed to use something in addition to 4-LUTs?

4. For the circuit diagram below, show how you would partition it into 4-LUTs, minimizing the total number of 4-LUTs:



5. From Mano: Problems 2-1, 2-3, 2-4, 2-6, 2-8, 2-10, & 2-11.