University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Sciences

EECS150 J. Wawrzynek
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Homework #4

This homework is due on **Friday February 22nd by 11am**. Homework will be accepted in the EECS150 box on the door to room 218 Cory Hall. Late homework will be penalized by 50%. No late homework will be accepted after the solution is posted.

1. Multi-level logic.

   a) Consider the following function expressed in two-level and/or form. Using algebraic manipulation, express the function in three-level or/and/or form:

   $$F = ac + ad + bc + bd + e$$

   b) Now assume that you can only use two-input and and or gates to implement this function. For both the two-level and the three-level forms, determine the cost in transistors, and the delay in terms of "gate delay".

2. From Mano: Problems 3-1, 3-8, 3-12, 3-13, 3-15, 3-33, 3-34, 3-35, & 3-36.

3. Using the World Wide Web assemble a list of software tools related to Verilog. For each tool briefly describe its function and include a URL. Try to make your list reasonable complete.