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Spring 2002 2/22/02

Midterm Exam I

1. [12 pts] Short Answers.

a) [2 pts] Choose between **FPGAs** and **Custom ICs** for each of the following design constraints:

	choice
For smaller NRE cost	*FPGA*
For faster time to market	*FPGA*
For smaller high-volume manufacturing cost	*Custom IC*
For higher performance	*Custom IC*

b) [1 pt] Moore's law says that the number of transistors on a chip double every ____*18*_____ months.

c) [1 pt] What is the minimum number of transistors required to implement a 3-input AND gate in the complementary MOS style?

8 (Eight)

d) [1 pt] Rebuffering signals sent on long wires on ICs is an effective way to control power, delay, cost (choose one): ___*delay*___

e) [2 pt] Write a Boolean expression for the exclusive-or of three variables x, y, & z.

$x'y'z + x'yz' + xy'z' + xyz$

f) [2 pt] Write a Boolean expression for the carry-out signal of a one-bit adder with inputs a, b, and ci.

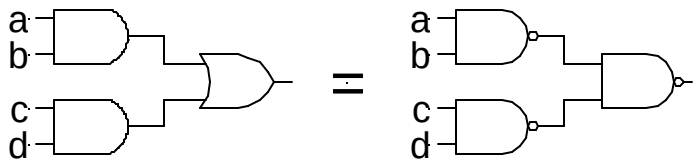
$ab + ac + bc$

g) [2 pt] Rewrite the Boolean expression (x+y)(x+z) as one with only 3 literals.
$x + yz$

h) [1 pt] Write an expression for the total number of Boolean functions that exist for n input variables. 2^{2^n}

2. [7 pts]

a) Showing all steps, us *algebraic manipulation* to show that an AND/OR circuit has equivalent function to an NAND/NAND circuit. In particular show that:



LHS

= **ab + cd**

= **((ab + cd)’)’**

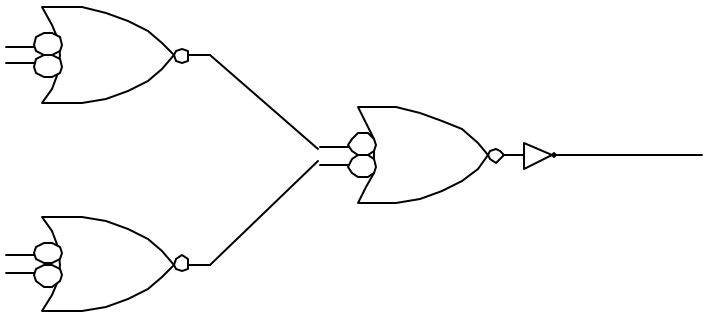
= **((ab)’.(cd)’)’** = RHS

b) Also through algebraic manipulation, show how to implement an AND/OR circuit with NORs and (if needed) inverters. Draw your NOR circuit implementation of ab+cd.

ab + cd

= **(a’’b’’ + c’’d’’)’’**

= **(((a’+b’)’ + (c’+d’)’)’)’**



3. [15pts] We will define a binary encoder as a combinational logic circuit that takes a one-hot encoded word (only one bit is ever equal to 1) and generates a binary number representing the bit position of the single bit equal to 1. We will number input bits from right to left starting at 1. The inputs bits are labeled as follows: [x4 x3 x2 x1], and the outputs are labeled as [y2 y1 y0]. If the input to the encoder was 0100 then the output will be $3_{10} = 011_2$.

a) Write the canonical forms - both some of products (SOP) and products of sums (POS) for y0, y1, and y2.

x_4	x_3	x_2	x_1	y_2	y_1	y_0
1	0	0	0	1	0	0
0	1	0	0	0	1	1
0	0	1	0	0	1	0
0	0	0	1	0	0	1
All other inputs				-	-	-

SOP:

$y_2 = x_4x_3'x_2'x_1'$

$y_1 = x_4'x_3x_2'x_1' + x_4'x_3'x_2x_1'$

$y_0 = x_4'x_3x_2'x_1' + x_4'x_3'x_2'x_1$

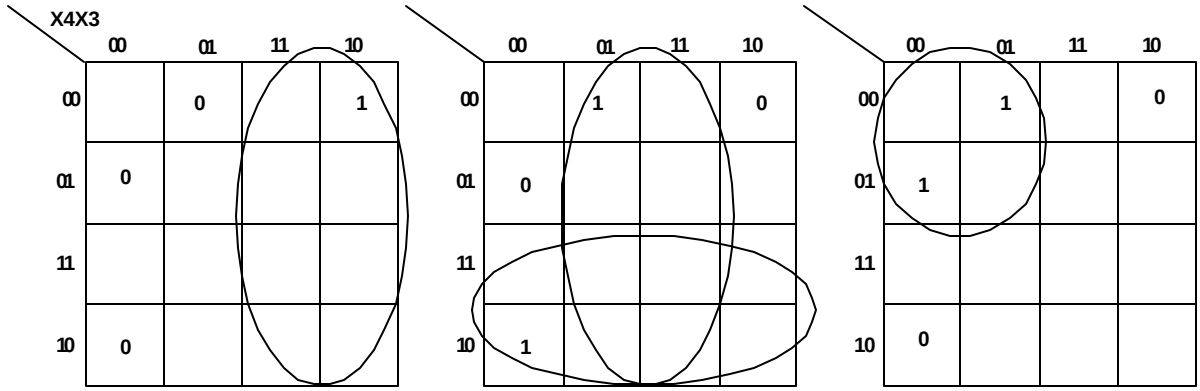
POS:

$y_2 = (x_4+x_3'+x_2+x_1)\ (x_4+x_3+x_2'+x_1)\ (x_4+x_3+x_2+x_1')$

$y_1 = (x_4'+x_3+x_2+x_1)\ (x_4+x_3+x_2+x_1')$

$y_0 = (x_4+x_3'+x_2+x_1)\ (x_4+x_3+x_2+x_1')$

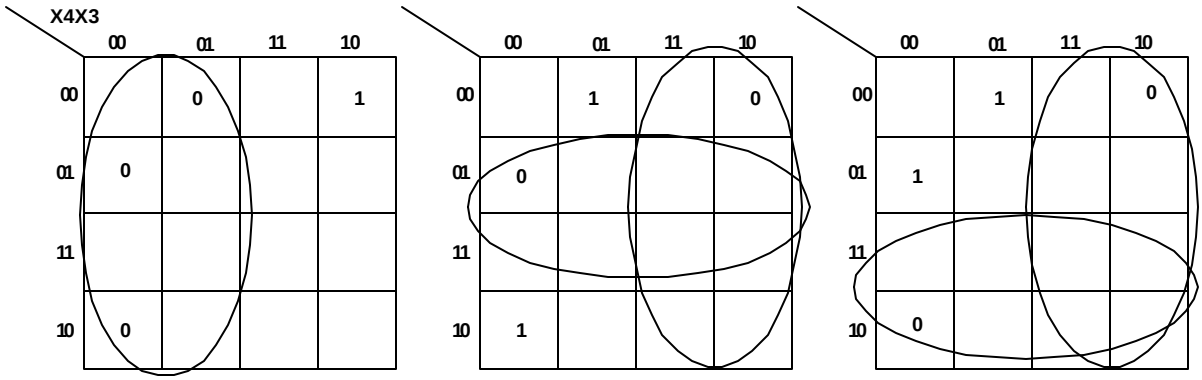
b) Using the k-map technique derive the minimized SOP equations for the three bits of the output, y0, y1, and y2.



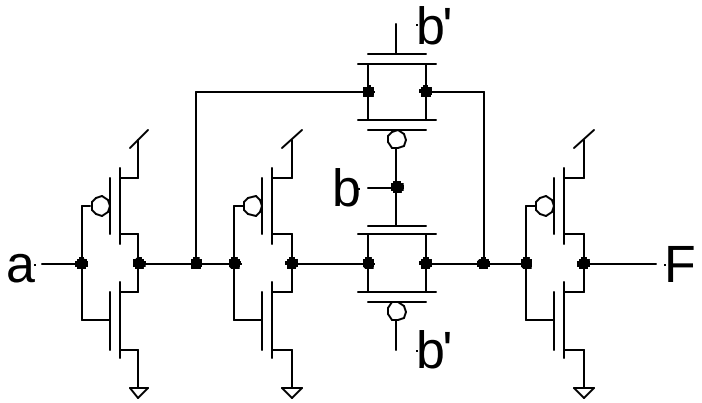
Y2 = X4 Y1 = X3 + X2 Y0 = X2' X4'

c) Using the k-map technique derive the minimized POS equations for the three bits of the output, y0, y1, and y2.

Y2 = X4 Y1 = X1' X4' Y0 = X2' X4'



4. [5 pts] Consider the circuit shown below. Write a simple Boolean expression that describes its function.

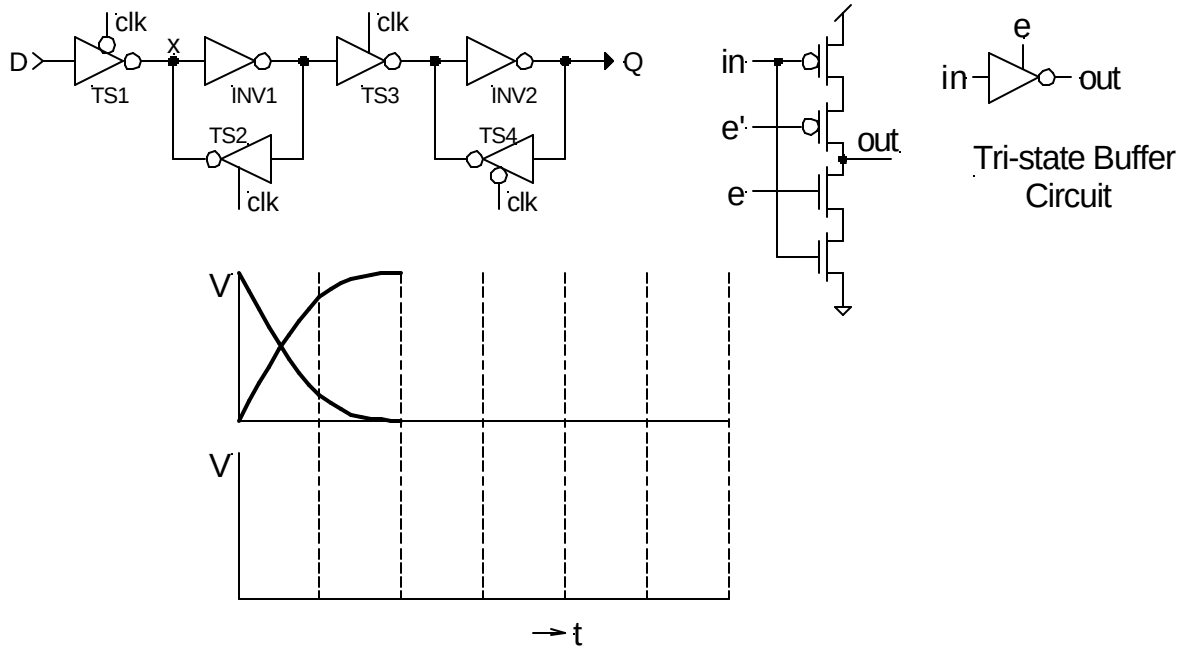


$F = a \oplus b = a'b + ab'$

5. [12pts] Consider the edge-triggered flip-flop circuit shown below. Assume that all the transistors in the flip-flop circuit are of the same size. Ignore delay due to wires. The propagation delay of the tri-state buffer and the inverter, respectively, can be expressed as:

$T_{TS\text{-}LH} = 4 + 4F$	delay for tri-state buffer low to high transition
$T_{TS\text{-}HL} = 2 + 2F$	delay for tri-state buffer high to low transition
$T_{INV\text{-}LH} = 2 + 2F$	delay for inverter low to high transition
$T_{INV\text{-}HL} = 1 + F$	delay for inverter high to low transition

where F is the fan-out in units of gate inputs (one n-type and one p-type transistor gate connection). The tri-state buffer delay is the same for both the in-to-out delay and the e-to-out delay.



a) Write an expression for the clock to Q delay (T_{CQ}) of the flip-flop in terms of the fan-out of the flip-flop.

$T_{C\text{->}Q}$ HL $= T_{TS\text{-}LH} + T_{inv\text{-}HL} = 4 + 4F^{\text{->}1} + 1 + F^{\text{->}1+F} = 4 + 4 + 1 + 1 + F = 10+F$

$T_{C\text{->}Q}$ LH $= T_{TS\text{-}HL} + T_{inv\text{-}LH} = 2 + 2F^{\text{->}1} + 2 + 2\,F^{\text{->}1+F} = 2 + 2 + 2 + 2 + 2F = 8+2F$

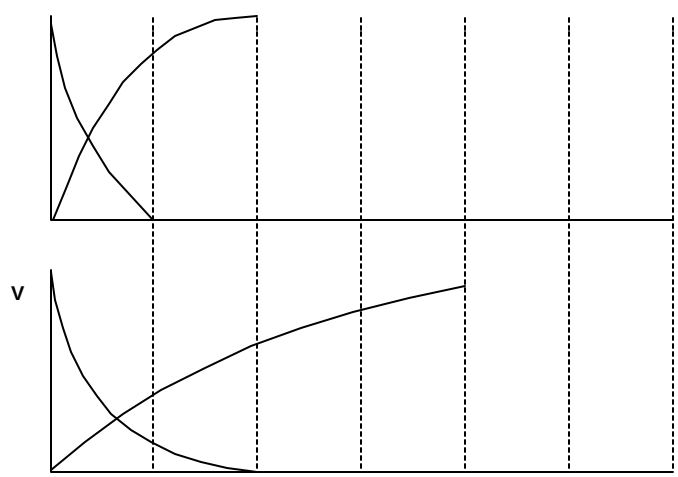
b) Determine the setup time of the flip-flop (T_{SU}).

Same as a) expect that fanout is known

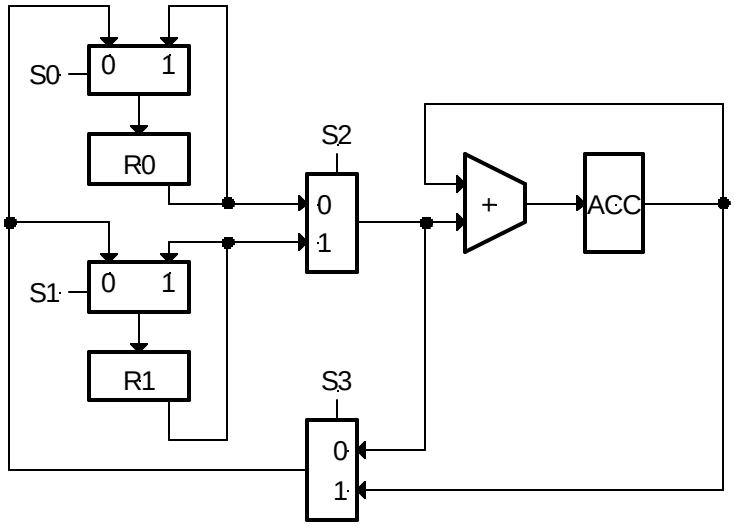
$T_{S_{HL}} = 10+F^{->1} = 11$

$T_{S_{LH}} = 8+2F^{->1} = 10$

c) The waveforms shown in the illustration represent the low-to-high and high-to-low transitions of a single inverter driving another single inverter. Using this as your guide, in the place provided, draw a sketch of the waveforms for both low-to-high and high-to-low transitions at node x. Assume that CLK=0.



6. [10 pts] The circuit shown below includes three registers (labeled R0, R1, and ACC) implemented with positive-edge triggered flip-flops, an n-bit adder, and 2-to-1 multiplexors.



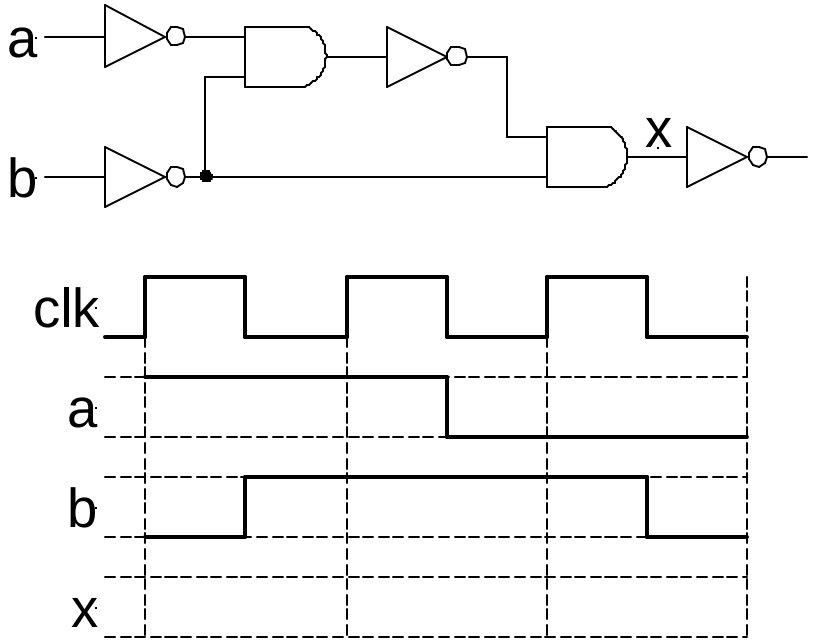
a) The table below has one row for each clock cycle of interest. A clock cycle goes from the rising edge of the clock to the next rising edge. The table is filled in with the values of S0, S1, S3, and the register contents (in base 10) as applied to the circuit by some external method. These values are applied after the rising edge of the clock (so that they can be ready for the *next* rising edge of the clock). Trace the operation of the circuit and fill in the empty squares in the table with the proper values as they would be appear at the end of each clock cycle.

Cycle #	S0	S1	S2	S3	R0	R1	ACC
1	1	0	0	0	1	0	4
2	-	-	-	-	*1*	*1*	*5*
10	1	1	1	1	2	3	0
11	1	1	0	0	*2*	*3*	*3*
12	1	0	0	1	*2*	*3*	*5*
13	0	1	1	1	*2*	*5*	*7*
14	-	-	-	-	*7*	*5*	*12*

b) Write an expression for the minimum achievable clock period with this circuit in terms of the mux delay (T_{MUX}), adder delay (T_{ADD}), flip-flop setup time (T_{SU}), and clock to Q delay ($T_{C\text{-}Q}$). Assume perfect clock distribution.

$T_{clk} >= T_{setup} + T_{clk\text{->}Q} + \max(T_{mux} + T_{add}, 3.\ T_{mux})$

7. [10 pts] Consider the simple combinational logic circuit shown below. Inputs a and b are applied over three clock cycles as shown in the waveforms. The clock period is 10ns.

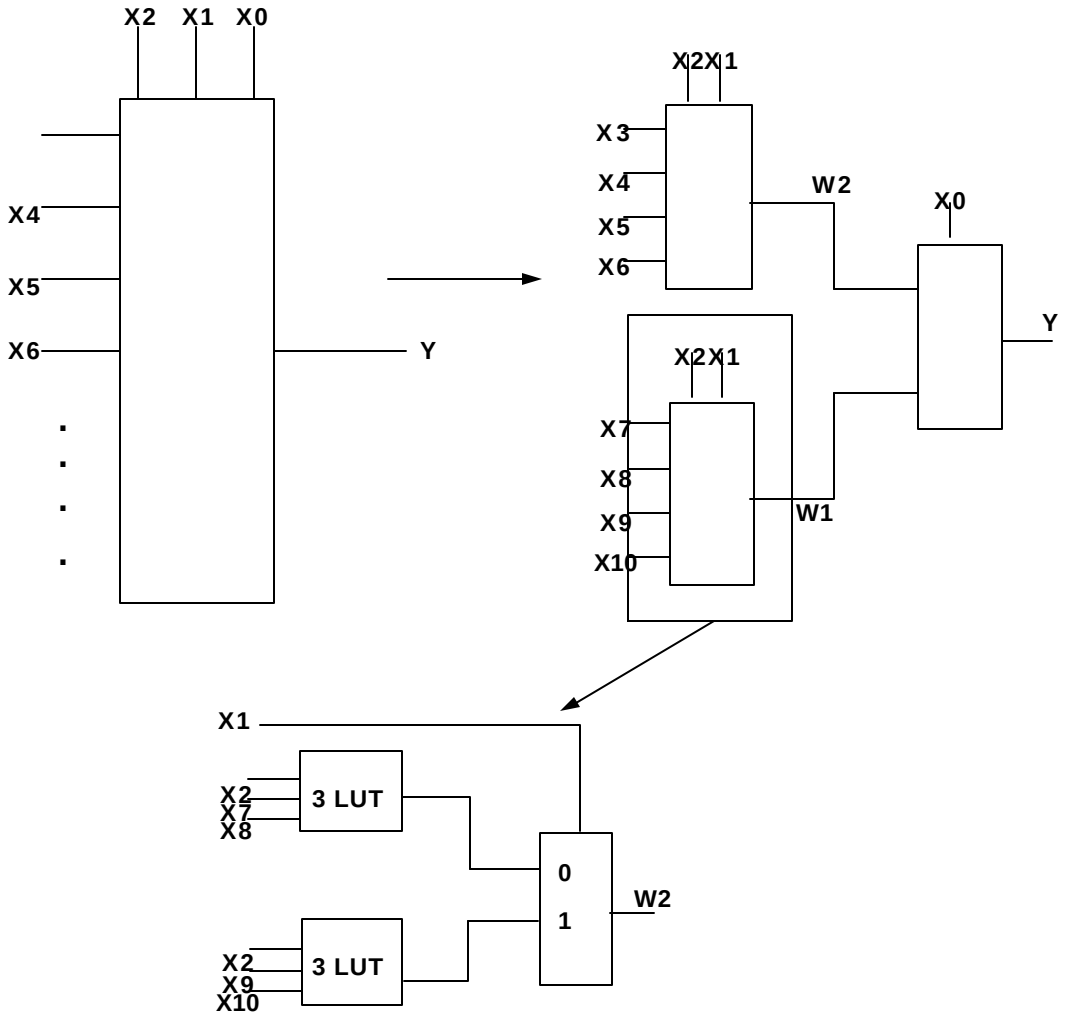


a) Draw the waveform for node x in the place provided. *Don't forget to account for gate delays.*

b) Write an expression for the total energy consumed by the output of the AND gate driving node x over these three clock cycles.

c) Write an expression for the average power consumption by the output of the AND gate driving node x over these three clock cycles.

8. [8pts] Given the logic function shown in the circuit below and the configurable logic block (CLB), partition the circuit so that it can be implemented with a collection of CLBs. Indicate your answer by filling in the table: one row per CLB used: write in the name of the signal wire from the logic circuit that corresponds to the CLB input or output; for the configuration bit, s, write in a "0" or "1". *Try to use as few a number of CLBs as possible.* You can extend the table or leave some rows blank. If you add any new signal wires, label the wires.



a	**b**	**c**	**d**	**e**	**f**	**g**	**s**	**h**
X_1	X_2	X_3	X_4	X_2	X_5	X_6	1	W_1
X_1	X_2	X_7	X_8	X_2	X_9	X_{10}	1	W_2
X_0	W_1	ϕ	ϕ	W_2	ϕ	ϕ	1	h