

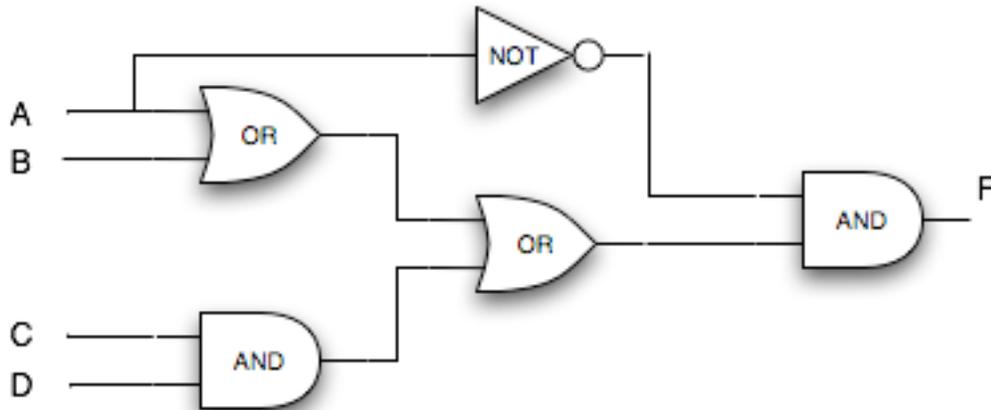
University of California at Berkeley
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EECS 150
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Problem Set #2: Programmable Logic
Assigned 23 January 2007, Due 2 February at 2 PM (REVISED)

1. Consider the following multilevel schematic constructed from AND-OR gates.



- a. What is the Boolean algebra equation derived from this schematic?
 - b. What is the minimized AND-OR schematic that is equivalent to this schematic? Show your work using a K-map.
 - c. Suppose that the schematic is restricted to only using NAND, NOR, and NOT gates. Convert the original schematic to a similar one making use of these gates only.
 - d. Suppose that the schematic is restricted to only using NAND gates. Convert the original schematic to a similar one using only NAND gates. NOTE: You may have to add some gates to make the mapping work!
 - e. Suppose that the schematic is restricted to only using NOR gates. Convert the original schematic to a similar one using only NOR gates. NOTE: You may have to add some gates to make the mapping work!
2. Consider the following to be implemented in Programmable Logic Arrays:
- $$F(A,B,C,D) = \Sigma m(3,6,7,9,11,13,14,15)$$
- $$G(A,B,C,D) = \Sigma m(5,7,9,13,15)$$
- $$H(A,B,C,D) = \Sigma m(3,9,11,13)$$
- $$I(A,B,C,D) = \Sigma m(5,6,13,14)$$
- a. Use K-maps to minimize in sum of products form each of the four functions independently. Write down the Boolean expressions that result.
 - b. How many unique product terms span the four functions?
 - c. Now minimize the four functions, seeking to find the minimum number of

- product terms across all four functions simultaneously.
- d. How many unique terms does your solution require? Is it a savings compared with your answer to part b?
 - e. Show how you would program the AND-OR array to implement the four functions using your solution to part c.
3. Programmable logic arrays as presented in class are based on AND-OR two-level logic. It is also possible to implement logic arrays in OR-AND logic. Repeat parts (a) through (d) except where the target is product of sums expressions for the functions F, G, H, I described above.
 - e. Which solution is better and why, 2(d) versus 3(d)?
 4. Given the function $F(A,B,C) = \Pi M(1,4,6)$:
 - a. Show how to implement F with an 8:1 multiplexer.
 - b. Show how to implement F with a 4:1 multiplexer (HINT: put A and B on the selection inputs).
 5. Given the function $G(A,B,C,D) = \Sigma m(0,1,2,5,6,7,8,10,12,13)$:
 - a. Show how to implement G with a 16:1 multiplexer.
 - b. Show how to implement G with an 8:1 multiplexer (HINT: put A, B, and C on the selection inputs).
 6. Given the function $H(A,B,C,D) = \Pi M(2,3,4,5,6,7,8,10)$, show how to implement H with a single 4:1 multiplexer and no other logic.
 7. Given the same function from problem 6:
 - a. Implement H using a 4:16 decoder as a function generator along with a single large fan-in OR gate.
 - b. Implement H using a 3:8 decoder as a function generator along with a 5-input OR gate and two 2-input AND gates (HINT: use A, B, C as the control inputs to the decoder).
 8. How many whole and half Xilinx CLBs does it take to implement the following functions:
 - a. 2:1 Multiplexer, considered as a logic function of 2 data inputs, one selection input (3 inputs total), and one output.
 - b. 4:1 Multiplexer, considered as a logic function of 4 data inputs, 2 selection inputs (6 inputs total), and one output.
 - c. 8:1 Multiplexer, considered as a logic function of 8 data inputs, 3 selection inputs (11 inputs total), and one output. (HINT: construct as a cascaded implementation of several multiplexers of lesser number of inputs).
 - d. 16:1 Multiplexer, considered as a logic function of 16 data inputs, 4 selection inputs (20 inputs total), and one output. (HINT: same as part c).
 - e. Given the functions F and G of Problems 4 and 5, how many Xilinx CLBs would it take to implement these functions directly from their truth tables?

How would your answer change, if at all, given your answers to Problems 4 a,b and 5 a,b.