

University of California at Berkeley
College of Engineering
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EECS 150
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Problem Set # 9 (Assigned 3 April, Due 13 April)

1. Consider the design of two Finite State Machines PARENT and CHILD that need to communicate with each other. The PARENT FSM outputs a signal named START when it wants the CHILD FSM to begin performing some kind of processing on behalf of the parent. The CHILD FSM asserts its output END to indicate that it has completed the processing requested by the parent.
 - (a) Assuming that the Parent and the Child share a common clock, draw a simple timing diagram and associated state diagram that implements the handshake in as few states and transitions as possible. You can assume that the Child has nothing else to do except perform some function for the Parent: it starts in an idle state waiting for START and returns to that state when done.
 - (b) Now assume that the Parent and the Child do not share a common clock. Describe a scenario, and demonstrate its behavior with a simple timing diagram, that shows that your solution to Part (a) will no longer work, i.e., there is a sequence of timing events in which either the Parent's START or the Child's end can be missed by the other state machine.
 - (c) Now redesign your solution to Part (a) so it can handle the situation of Part (b). HINT: make use of four-cycle "return to zero" signaling. Redraw your state diagram and timing diagram to show how it would work.
 - (d) An alternative to four-cycle signaling is two-cycle signaling, also known as "non-return to zero" signaling. Redesign the state diagrams you developed for Part (c) so it implements two-cycle signaling. What are the implementation advantages/disadvantages of using the two-cycle approach versus the four-cycle approach of Part (c)?