# CS 150
# Digital Design

# Lecture 24 – Power and Energy

**2012-4-17**

**Professor John Wawrzynek**

**today's lecture by John Lazzaro**

TAs: Shaoyi Cheng, Daiwei Li, James Parker

**www-inst.eecs.berkeley.edu/~cs150/**

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**Sad fact:** Computers turn electrical energy into heat. Computation is a byproduct.

# Energy and Performance

Air or water carries heat away, or chip melts.

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The Joule: Unit of energy. Can also be expressed as Watt-Seconds. Burning 1 Watt for 100 seconds uses 100 Watt-Seconds of energy.

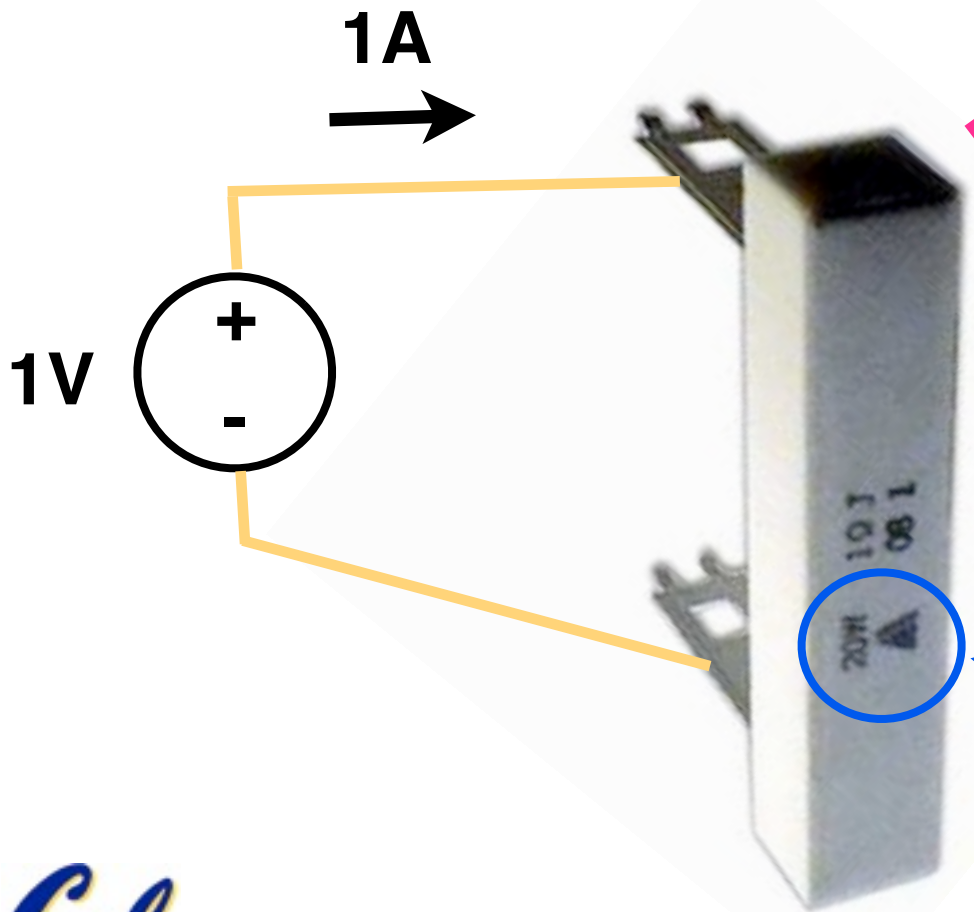
This is how electric tea pots work ...

1 Joule heats 1 gram of water 0.24 degree C

1 Joule of Heat Energy per Second

1 Watt

The Watt: Unit of power. The amount of energy burned in the resistor in 1 second.




1 Ohm Resistor

20 W rating: Maximum power the package is able to transfer to the air. Exceed rating and resistor burns.



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# Cooling an iPod nano ...

**Like resistor on last slide, iPod relies on passive transfer of heat from case to the air.**

Why? Users don't want fans in their pocket ...

**To stay "cool to the touch" via passive cooling, power budget of 5 W.**

If iPod nano used 5W all the time, its battery would last 15 minutes ...



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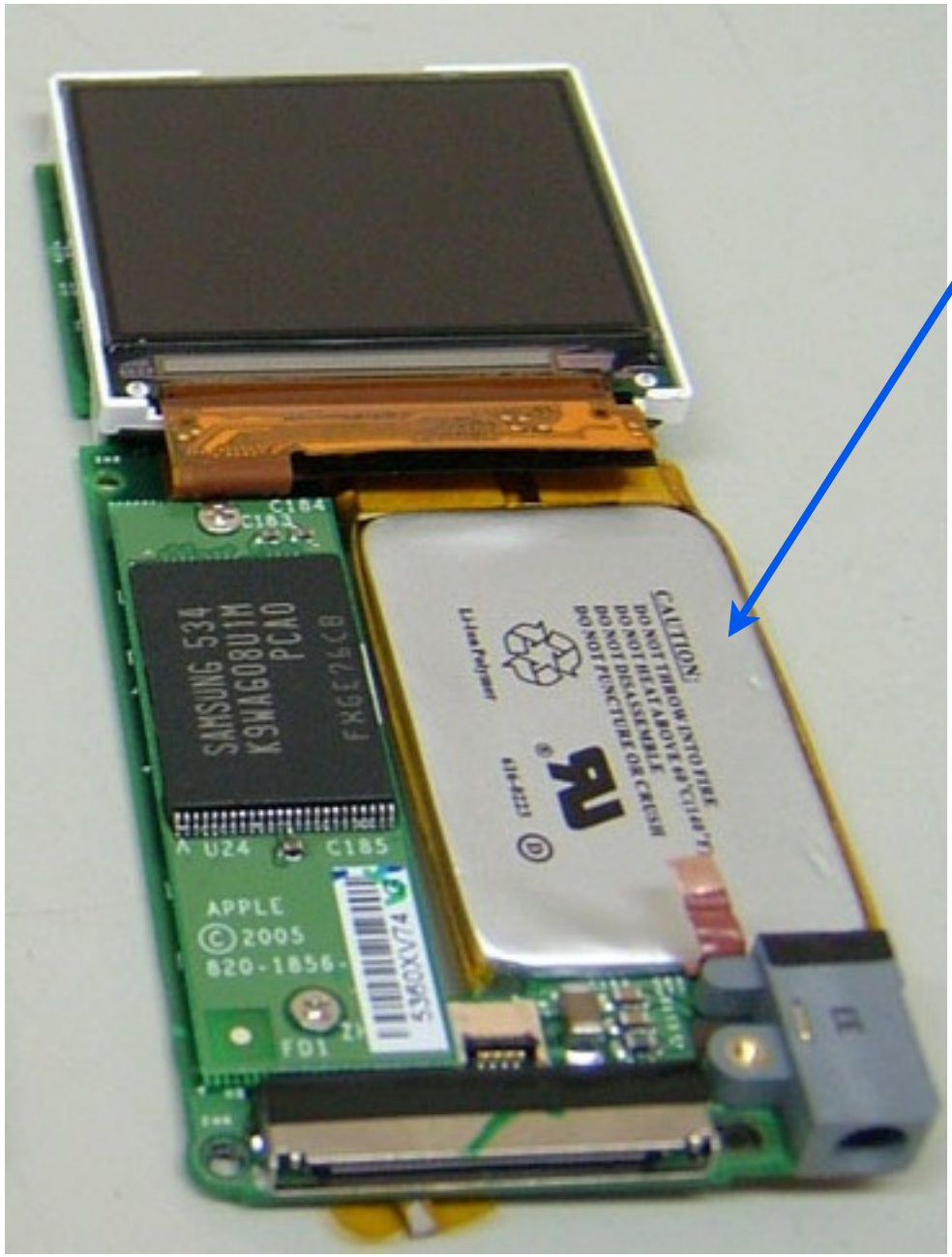
# Powering an iPod nano (2005 edition)




1.2 W-hour battery:
Can supply 1.2 watts
of power for 1 hour.

1.2 W / 5 W = 15 minutes.

More W-hours require bigger battery
and thus bigger "form factor" --
it wouldn't be "nano" anymore :-).

**Real specs for iPod nano :**

**14 hours for music,**
**4 hours for slide shows.**

85 mW for music.
300 mW for slides.



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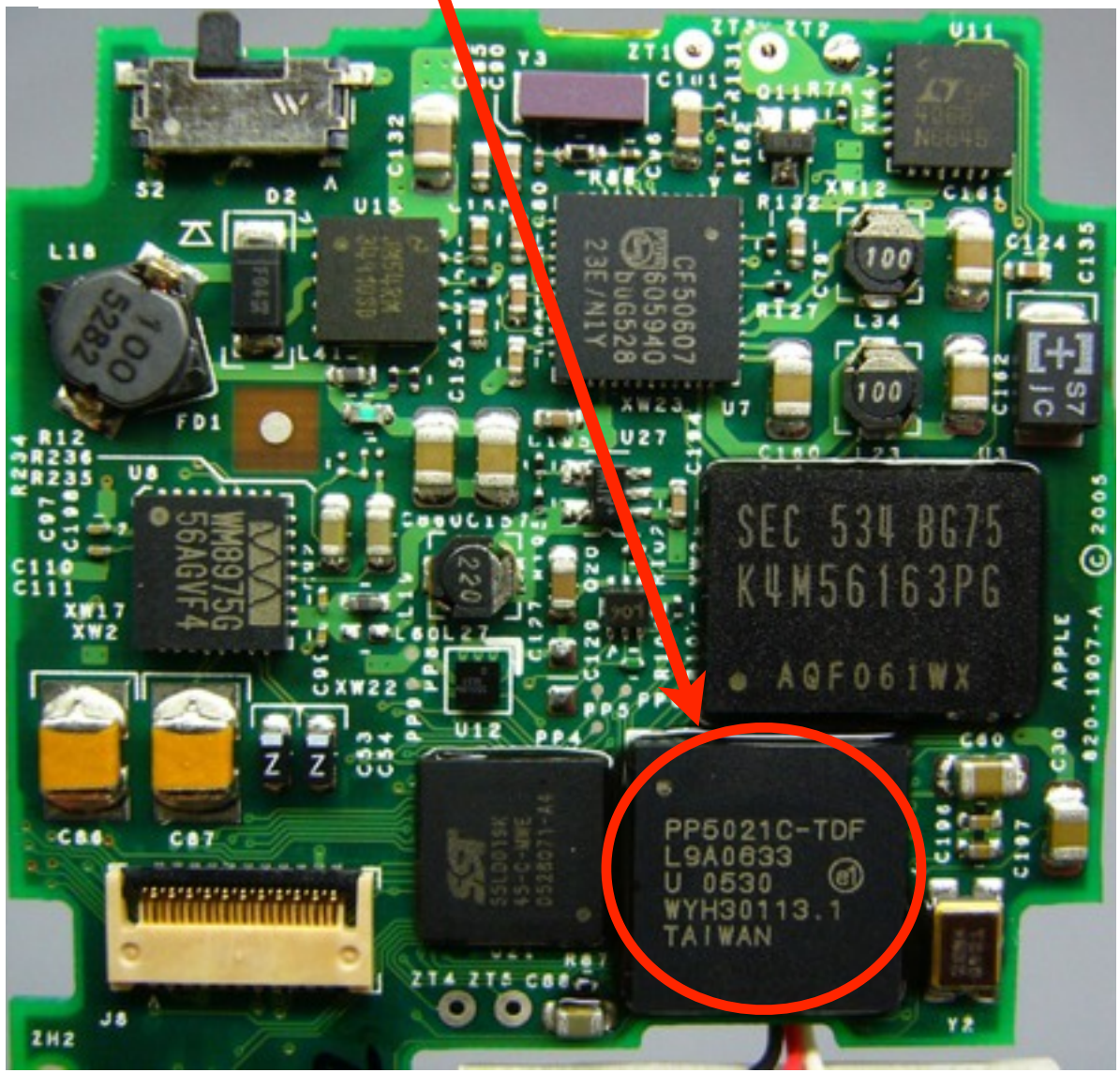
# Finding the (2005) iPod nano CPU ...

portalplayer™

A close relative ...

**PP5020**

digital media management system-on-chip




Two 80 MHz CPUs. One CPU used for audio, one for slides.

Low-power ARM roughly 1mW per MHz ... variable clock, sleep modes.

85 mW system power realistic ...



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# Year-to-year: continuous improvements

iPod nano
2005
14 hours
battery
life
(audio
playback)

iPod nano
2006
24 hours
battery
life
(audio
playback)

What
changed
inside ?

Source: ifixit.com



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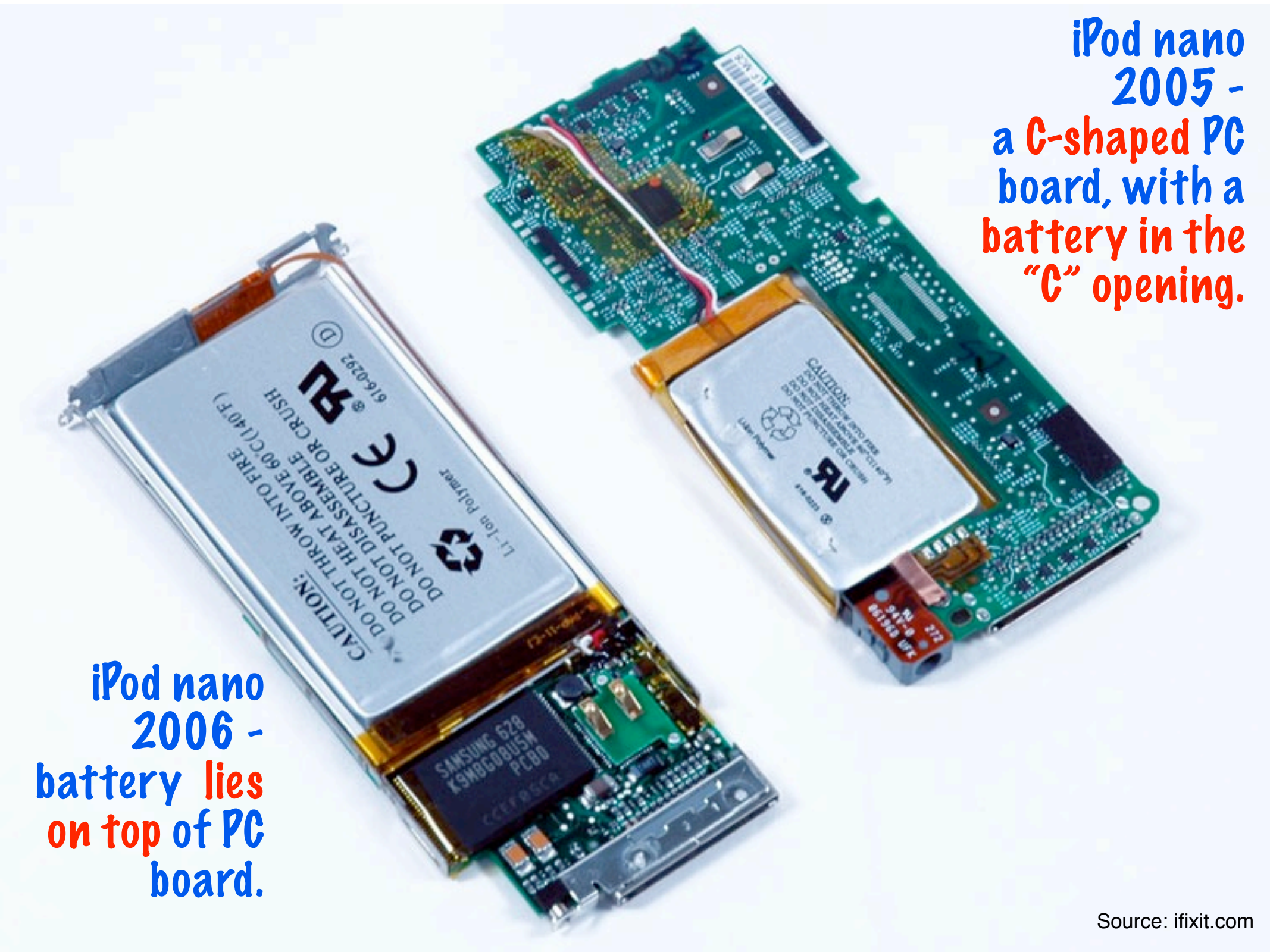
Source: ifixit.com

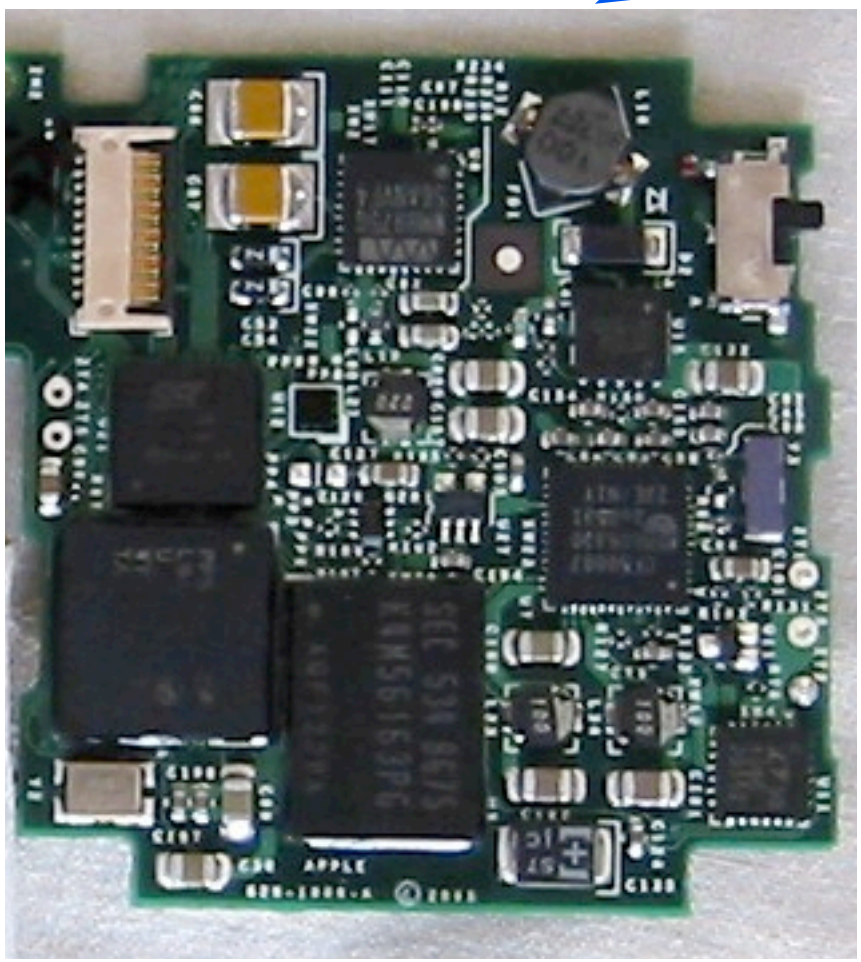
Source: ifixit.com


iPod nano 2005 - a C-shaped PC board, with a battery in the "C" opening.
iPod nano 2006 - battery lies on top of PC board.
Source: ifixit.com

# How? Small IC packages, fewer parts

iPod nano 2006 →

iPod nano 2005 →



Source: arstechnica.com

# Aluminum permits thinner case ...

Source: ilounge.com

nearly the same depth

## 2010 Nano

0.74 ounces

## 2010 Shuffle

0.44 ounces

2010 Nano:
"up to" 24 hours
audio playback

2010 Shuffle:
"up to" 15 hours
audio playback

0.39 W Hr
(33% of 2005 Nano)

0.19 W Hr

Sources: iFixit, Apple



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| | 2007 | 2008 | 2009 | 2010 | 2011 | Today |
|---|---|---|---|---|---|---|
| | iPhone | iPhone 3G | iPhone 3GS | iPhone 4 | iPhone 4 (CDMA) | iPhone 4S |
| Display | 3.5" TFT LCD, 480 x 320 pixels | 3.5" TFT LCD, 480 x 320 pixels | 3.5" TFT LCD, 480 x 320 pixels | 3.5" IPS LCD, 960 x 640 Pixels | | 3.5" IPS LCD, 960 x 640 Pixels |

Desired screen size sets smartphone W x L

Depth? : Thin body vs. battery life

| | 2007 | 2008 | 2009 | 2010 | 2011 | Today |
|---|---|---|---|---|---|---|
| | iPhone | iPhone 3G | iPhone 3GS | iPhone 4 | iPhone 4 (CDMA) | iPhone 4S |
| Battery | Li-Ion Polymer, 3.7V, 1170mAh | Li-Ion Polymer, 3.7V, 1150mAh | Li-Ion Polymer, 3.7V, 1220mAh | Li-Ion Polymer, 3.7V, 1420mAh | | Li-Ion Polymer, 3.7V, 1430mAh |

# 22% gain in battery energy over 5 iterations

# iPhone (2007)

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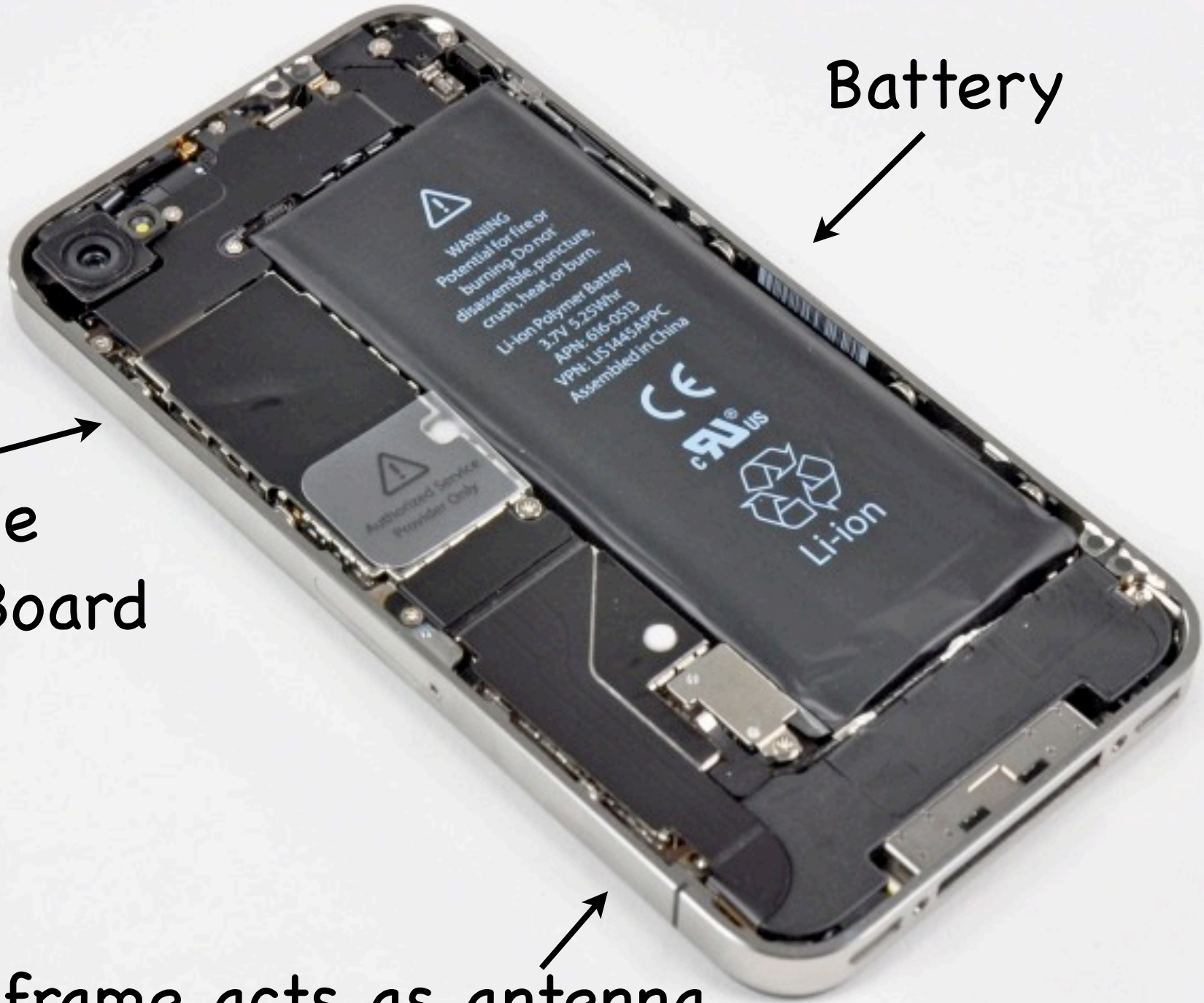
iPhone
4{,S}


Battery
L-shape
Main Board
Metal frame acts as antenna
WARNING
Potential for fire or
burning. Do not
disassemble, puncture,
crush, heat, or burn.
Li-ion Polymer Battery
3.7V 5.25Whr
APN: 616-0513
VPN: LIS1445APPC
Assembled in China
Li-ion

| | 2007 | 2008 | 2009 | 2010 | 2011 | Today |
|---|---|---|---|---|---|---|
| | iPhone | | | | | iPhone 4S |
| Apps Processor | Samsung S5L8900B01 ARM Core | | | | | Apple A5 Dual ARM Core Processor |
| Process Geometry | 90nm | | | | | 45nm |
| Die Size | 8.5 x 8.5 mm | | | | | 12.15 x 10.1 mm |
| Pin Count | 424 | | | | | 1360 |
| ARM Core (Instruction Set) | ARM9 (ARMv5) | | | | | Cortex-A9 (ARMv7) |
| Clock Speed | ~600MHz | | | | | ~800MHz |
| GPU | PowerVR MBX | | | | | PowerVR SGX (dual core) |
| SDRAM | 1Gb Mobile DDR | | | | | 4Gb Mobile DDR2 |

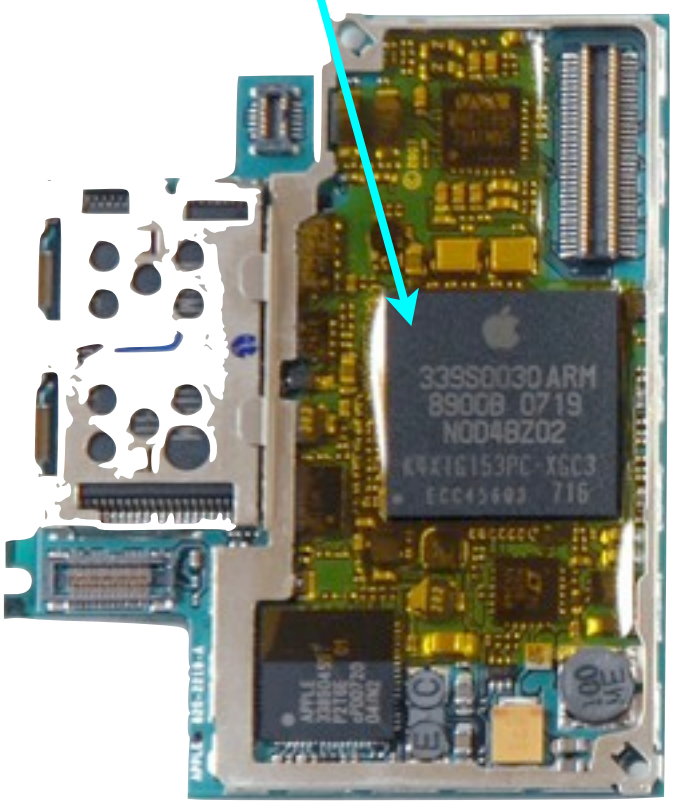
In 4 years:

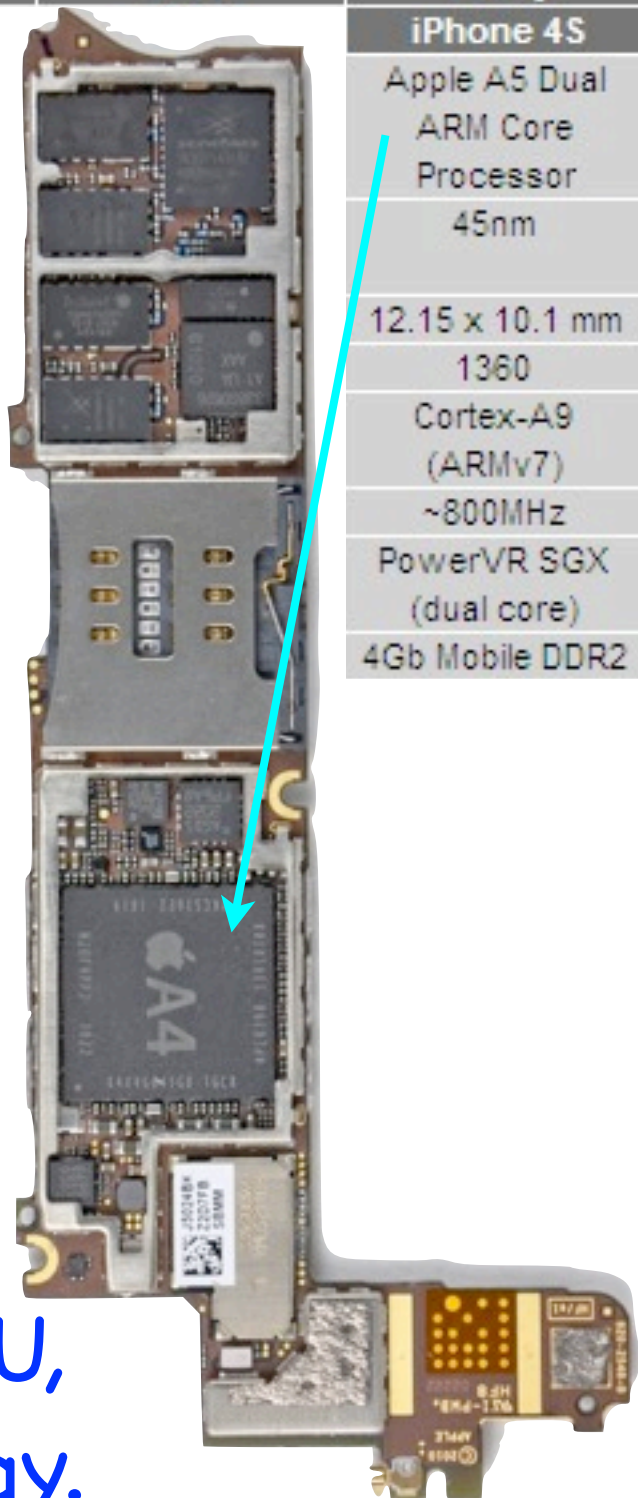
6.8x increase in transistor count

33% max clock speed increase

Attached DRAM:
128 MB -> 512 MB

6.8x transistors:
Dual CPU and GPU,
and to save energy.



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# Notebooks ... as designed in 2006 ...

2006 Apple MacBook -- 5.2 lbs

- **Performance:** Must be "close enough" to desktop performance ... most people no longer used a desktop (even in 2006).
- **Size and Weight.** Ideal: paper notebook.
- **Heat:** No longer "laptops" -- top may get "warm", bottom "hot". Quiet fans OK.


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# Battery: Set by size and weight limits ...

46x more energy than iPod nano battery. And iPod lets you listen to music for 14 hours!

Battery rating: 55 W-hour.

At 2.3 GHz, Intel Core Duo CPU consumes 31 W running a heavy load - under 2 hours battery life! And, just for CPU!

Almost full 1 inch depth. Width and height set by available space, weight.

At 1 GHz, CPU consumes 13 Watts. "Energy saver" option uses this mode ...



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55 W-hour battery
stores the energy of
1/2 a stick of dynamite.
If battery short-circuits,
catastrophe is possible ...

# MacBook Air … design the laptop like an iPod

2011 Air: 11.8 in x 7.56 in x 0.68 in; 2.38 lbs

2006 Macbook: 12.8 in x 8.9 in x 1 in; 5.2 lbs



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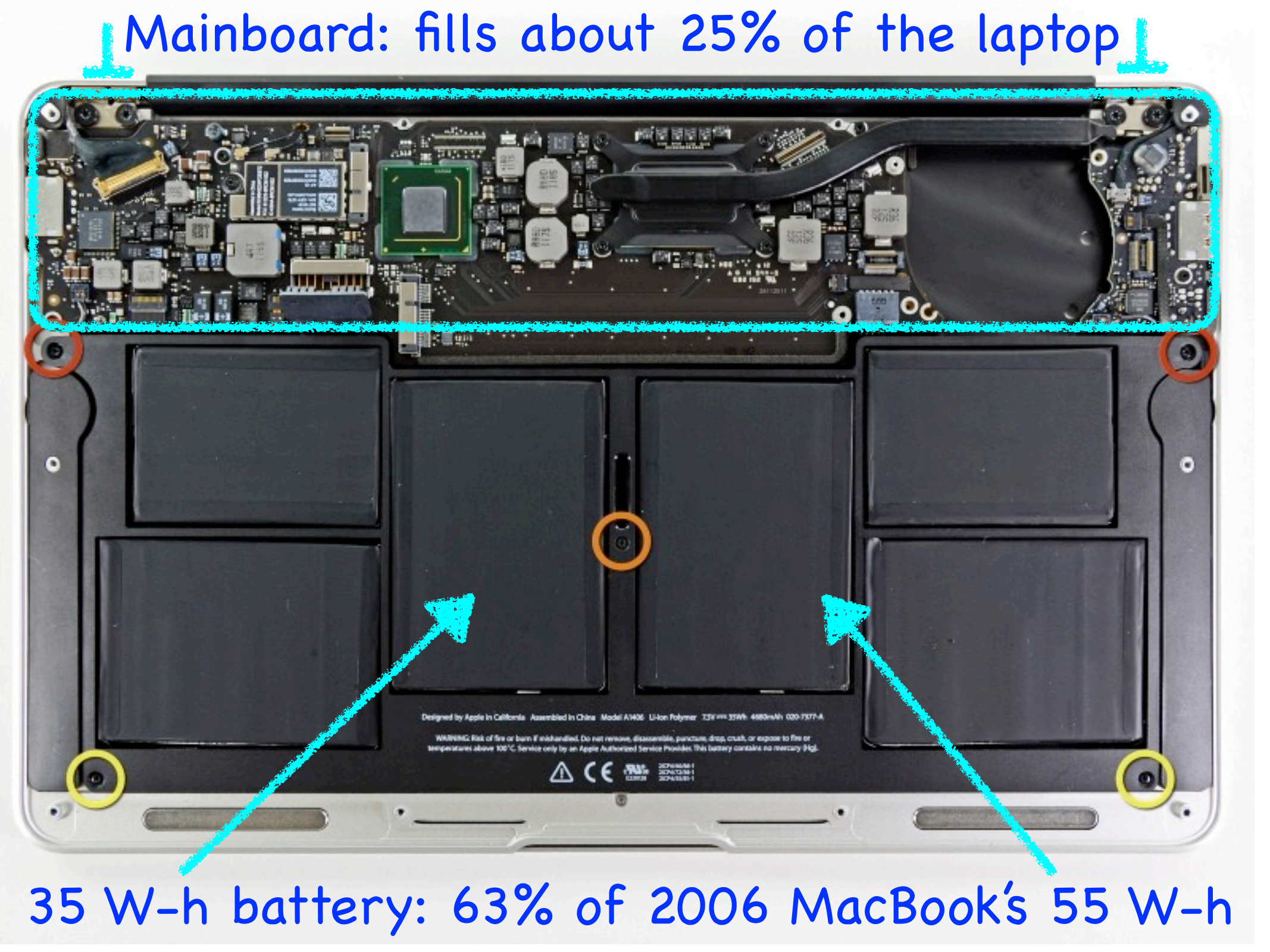
Mainboard: fills about 25% of the laptop
35 W-h battery: 63% of 2006 MacBook's 55 W-h

Condé Nast: The Evil Empire
703
$2.99
iPad

2011 Air: 35 W-h battery, 5 hour battery life*

2012 iPad: 42.5 W-h battery, 10 hour battery life*

*For a content-consumption workload.

Battery-Life-Hour/W-h: 1.7x iPad advantage



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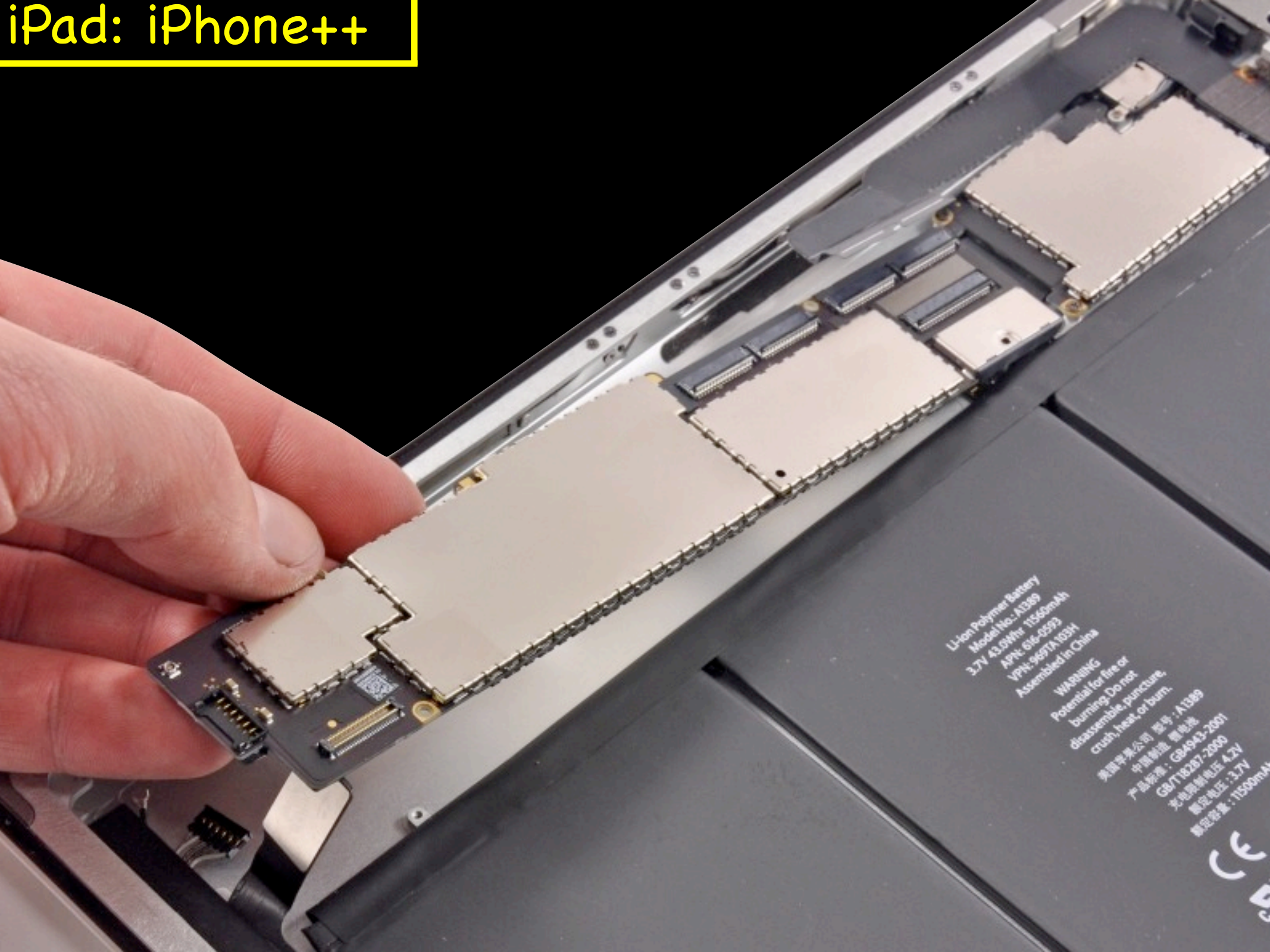
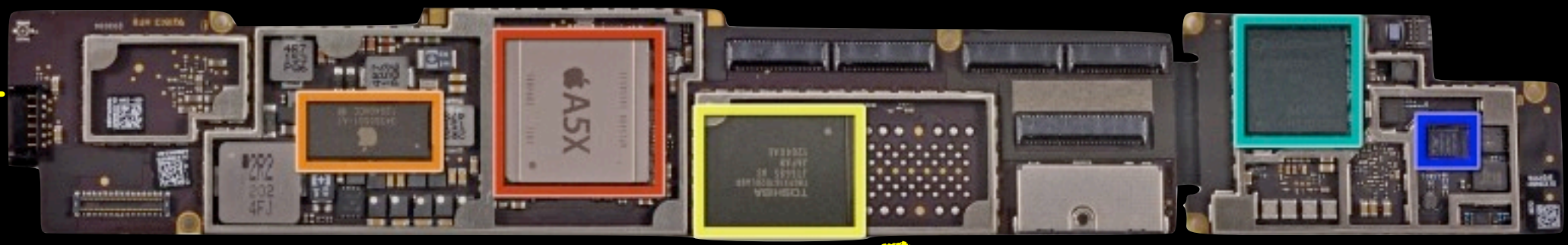
# iPad: iPhone++


Li-ion Polymer Battery
Model No.: A1389
3.7V 43.0Whr 11560mAh
APN: 616-0593
VPN: 969TA1031H
Assembled in China
WARNING
Potential for fire or
burning. Do not
disassemble, puncture,
crush, heat, or burn.

# iPad: iPhone++

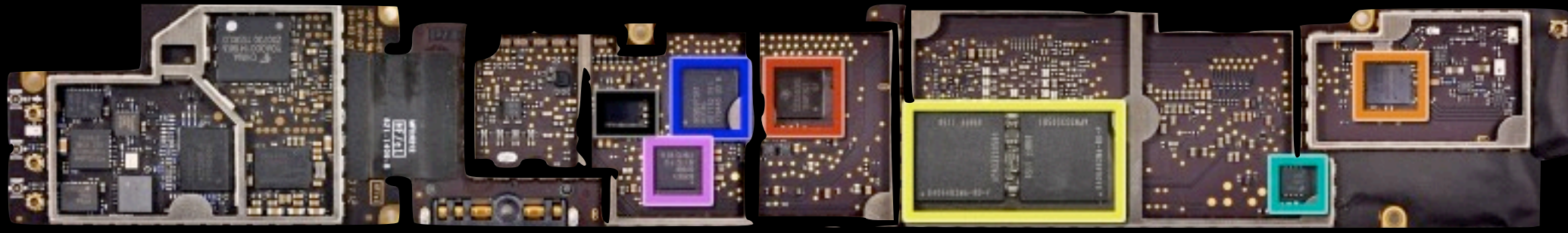
A5X: 2 ARM Cortex9 Cores, expanded PowerVR GPU

Top



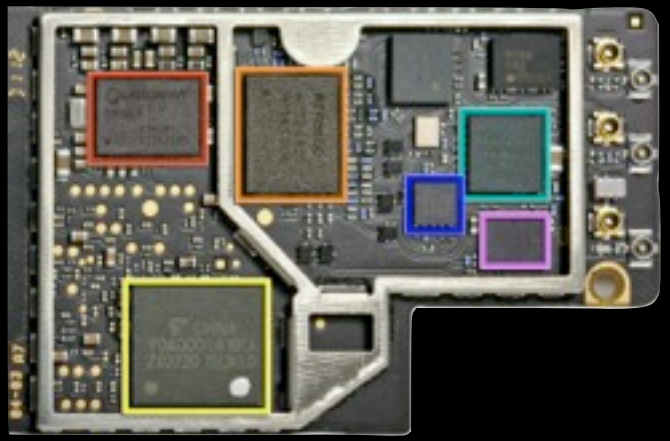

Up to 64 GB Flash

Bottom

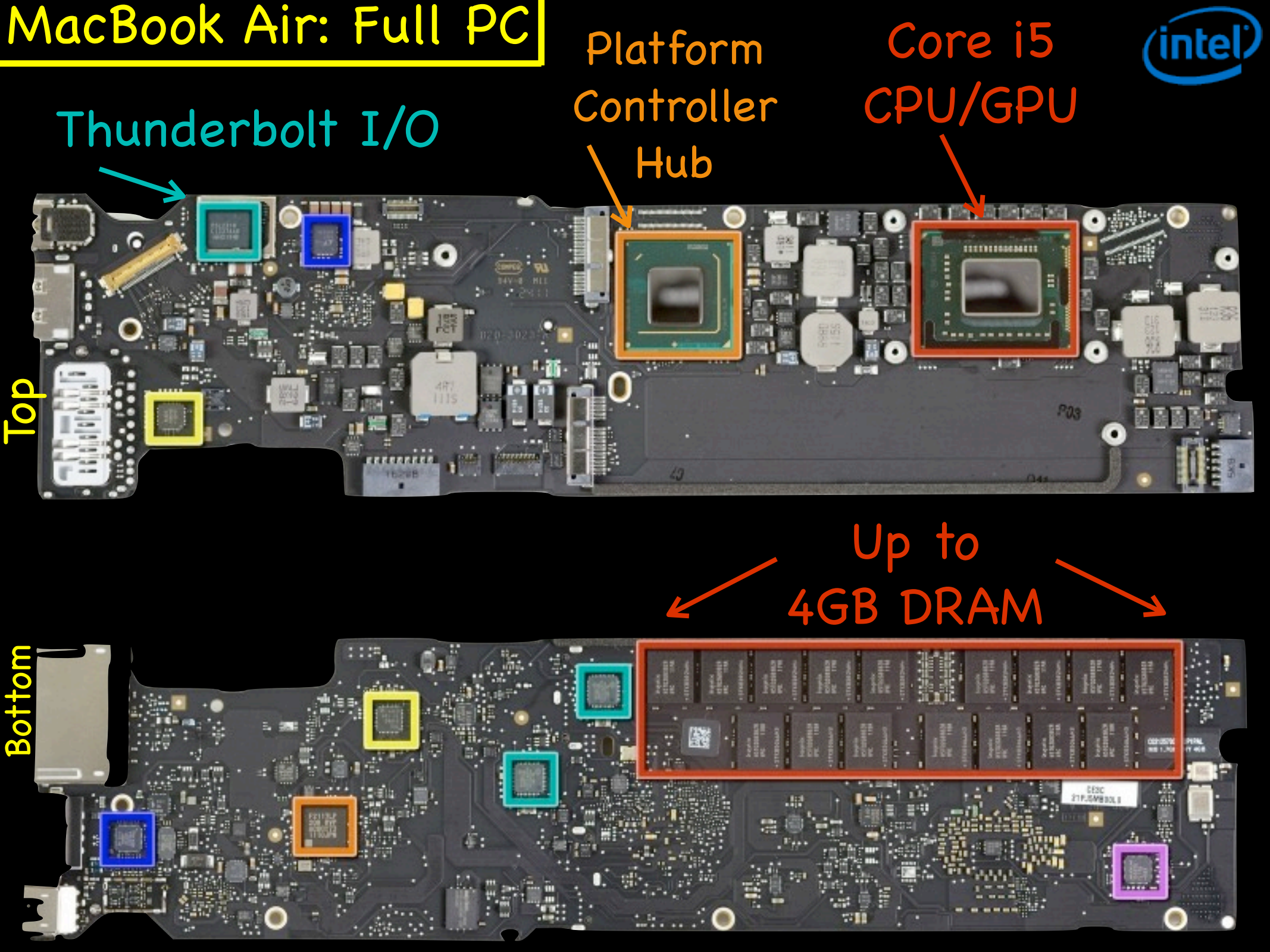


1 GB DRAM

Cellular RF



Cellular front-end chips on separate board.


MacBook Air: Full PC
Thunderbolt I/O
Platform Controller Hub
Core i5 CPU/GPU
Top
Up to 4GB DRAM
Bottom

2011 Air: $999 -- 64 GB SSD, 2 GB RAM, x86

2012 iPad: $699 -- 64 GB SSD, 1 GB RAM, ARM

iPad 2012 CPU: iPhone 4S, with 2X GPU and RAM

"Content Creation vs. Content Consumption"



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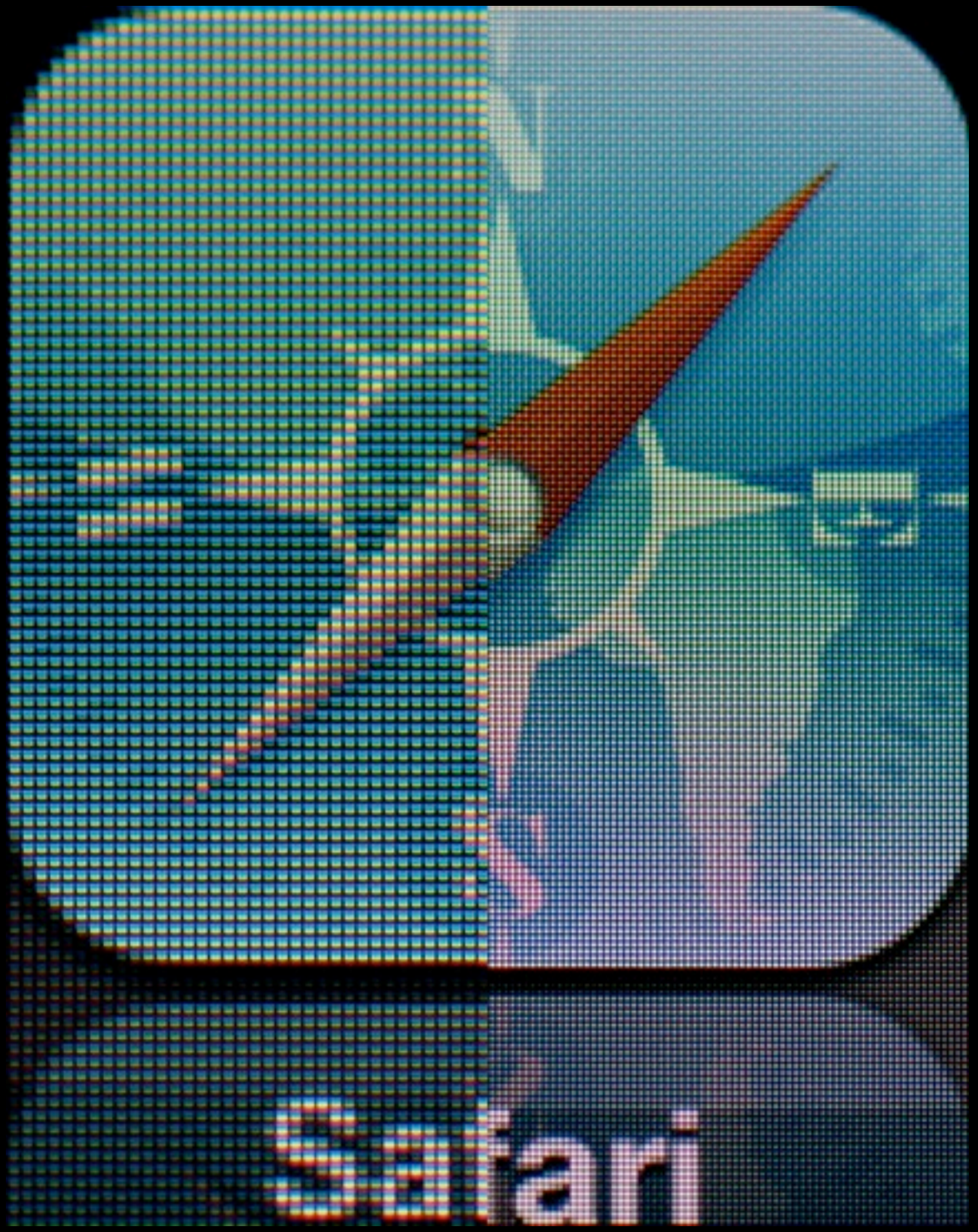
iPad 2011→2012, battery W-hours increased by 70%

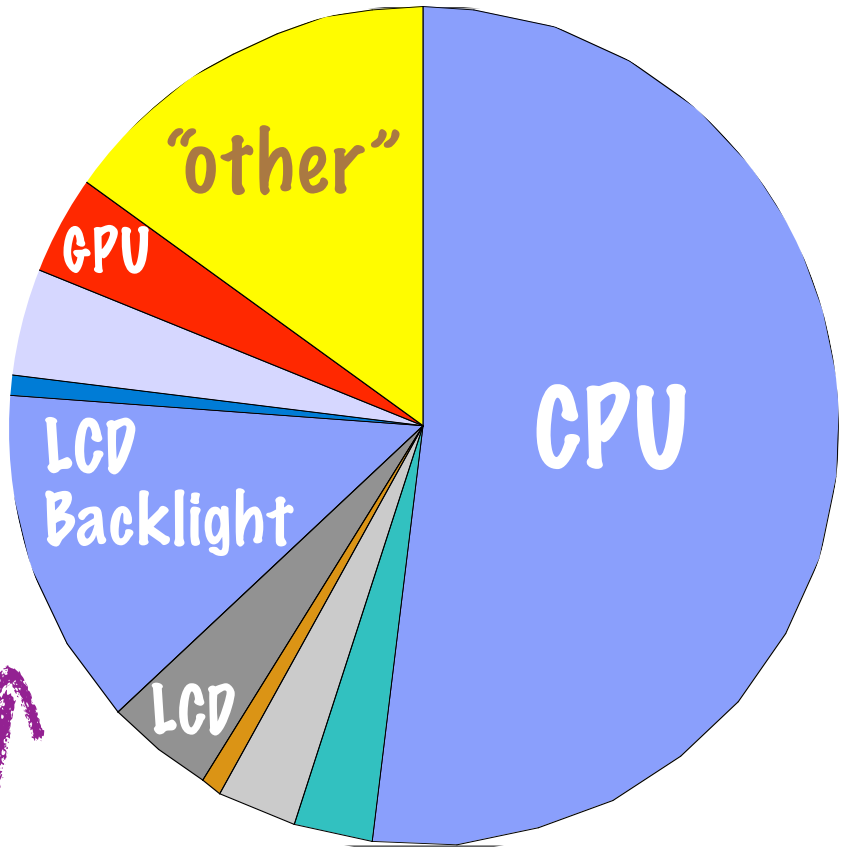
Weight increase of 0.11 pound, thicker by 0.03 inches.

Increase needed to double display resolution while keeping battery life @ 10 hours.



# The CPU is only part of power budget!

2004-era notebook running a full workload.




"Amdahl's Law for Power"

If our CPU took no power at all to run, that would only double battery life!

iPad 2011→2012 power++ comes from this side.

 Data courtesy Mahesri et al., U of Illinois, 2004 UC Regents Spring 2012 © UCB

# Servers: Total Cost of Ownership (TCO)

Machine rooms are expensive. Removing heat dictates how many servers to put in a machine room.

Electric bill adds up! Powering the servers + powering the air conditioners is a big part of TCO.

Reliability: running computers hot makes them fail more often.



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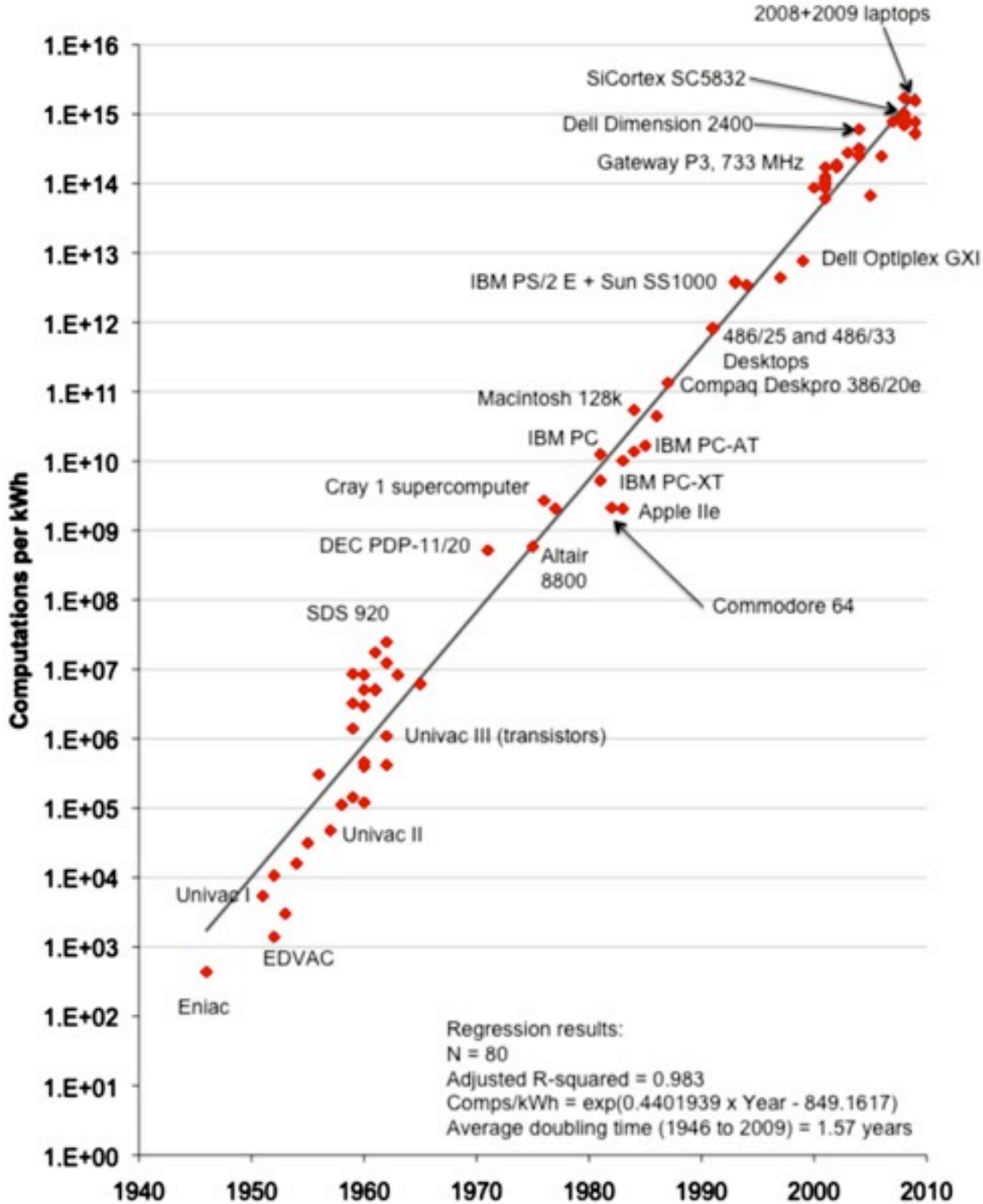
Computations per W-h doubles every 1.6 years, going back to the first computer.

(Jonathan Koomey, Stanford).



# Processors and Energy

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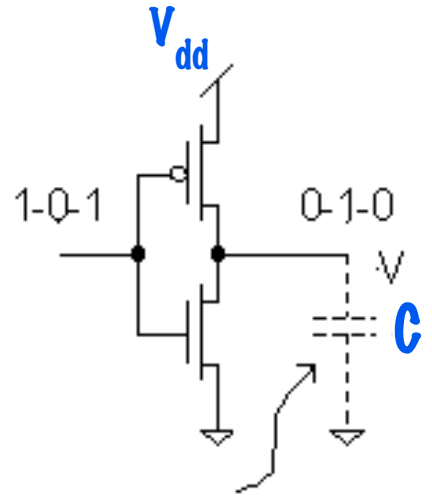
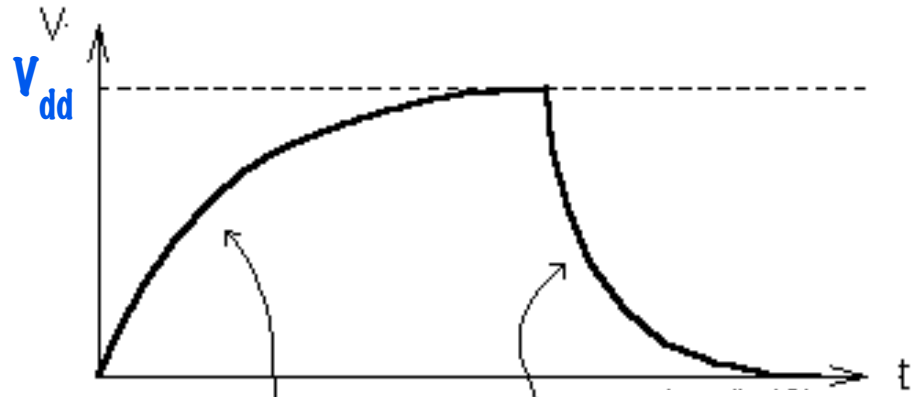
# Switching Energy: Fundamental Physics

## Every logic transition dissipates energy.




$$E_{0\to1} = \frac{1}{2} C V_{dd}^2 \qquad E_{1\to0} = \frac{1}{2} C V_{dd}^2$$

Strong result: Independent of technology.

**How can we limit switching energy?**

(1) Reduce # of clock transitions. But we have work to do ...

(2) Reduce Vdd. But lowering Vdd limits the clock speed ...

(3) Fewer circuits. But more transistors can do more work.

(4) Reduce C per node. One reason why we scale processes.



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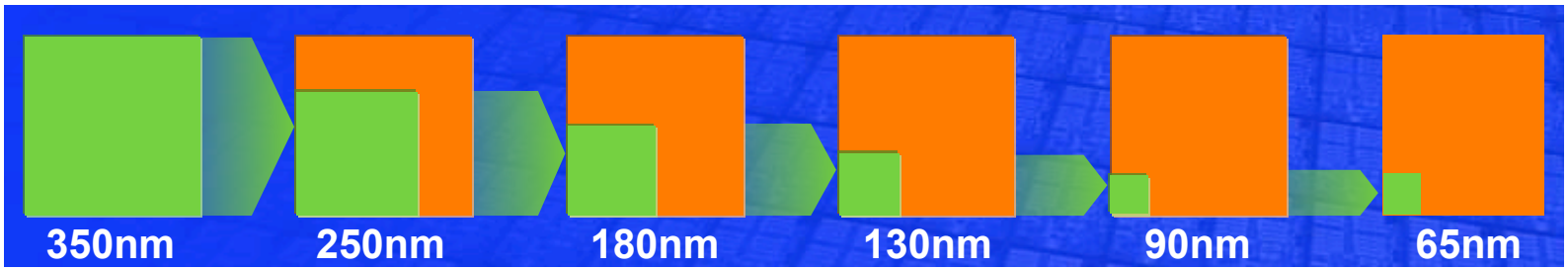
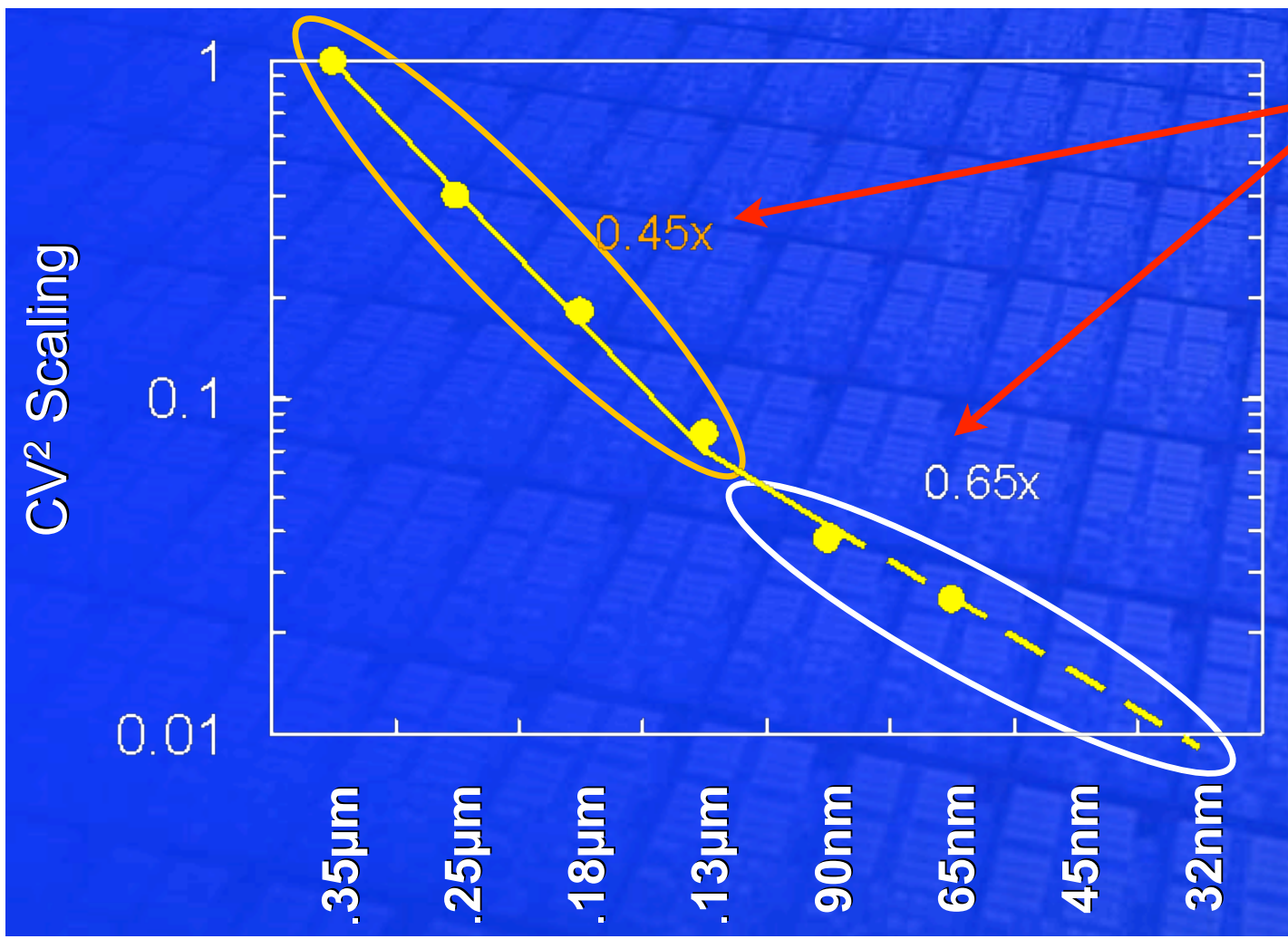
# Scaling switching energy per gate ...




IC process scaling ("Moore's Law")




Due to reducing V and C (length and width of Cs decrease, but plate distance gets smaller).

Recent slope more shallow because V is being scaled less aggressively.

From: "Facing the Hot Chips Challenge Again", Bill Holt, Intel, presented at Hot Chips 17, 2005.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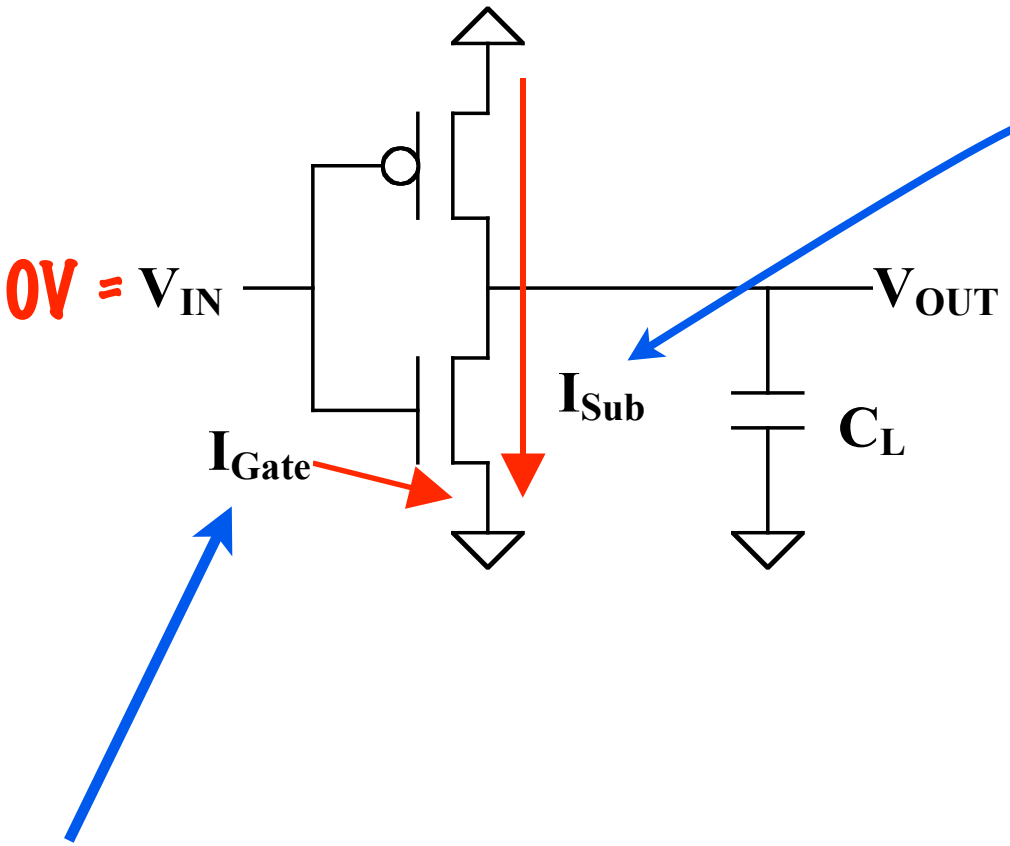
# Second Factor: Leakage Currents

Even when a logic gate isn't switching, it burns power.

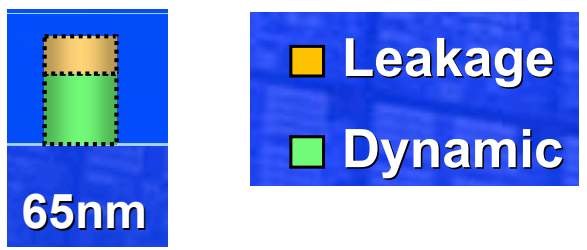



Isub: Even when this nFet is off, it passes an Ioff leakage current.

We can engineer any Ioff we like, but a lower Ioff also results in a lower Ion, and thus a lower maximum clock speed.

Igate: Ideal capacitors have zero DC current. But modern transistor gates are a few atoms thick, and are not ideal.

## Intel's 2006 processor designs, leakage vs switching power




A lot of work was done to get a ratio this good ... 50/50 is common.

Bill Holt, Intel, Hot Chips 17



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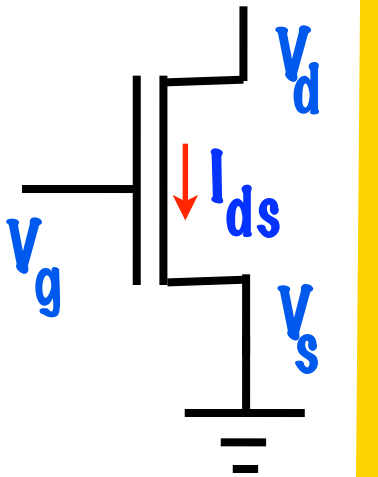
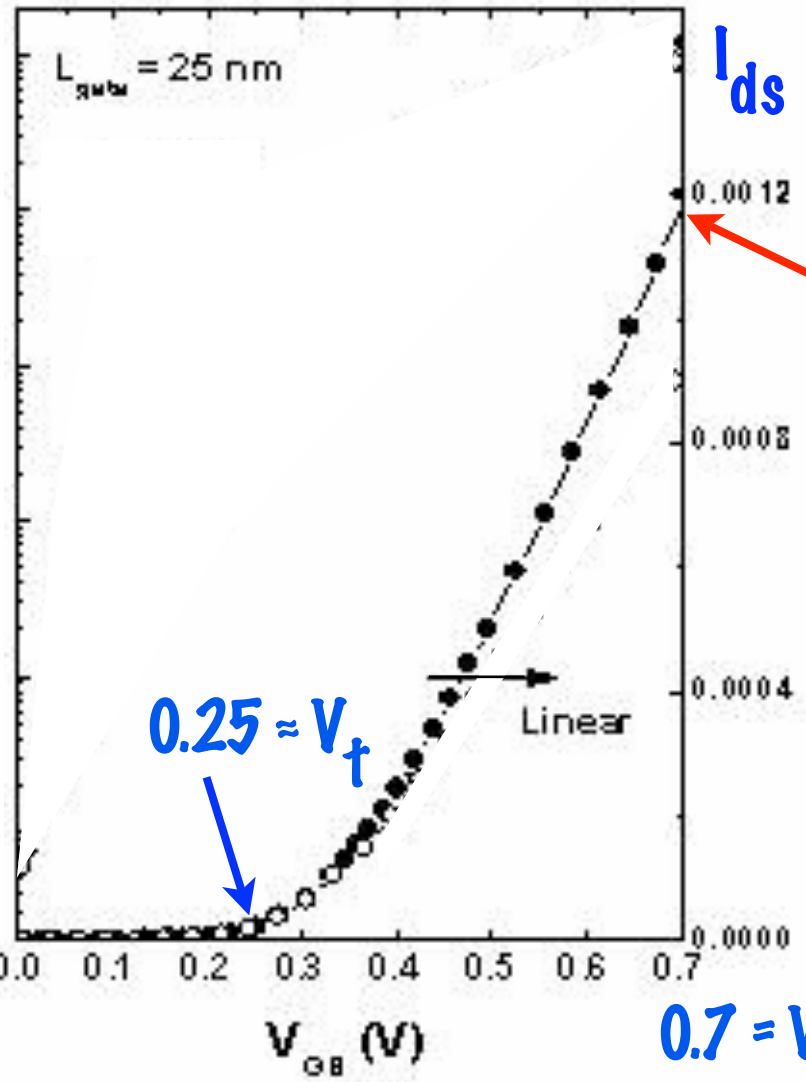
# Engineering "On" Current at 25 nm …




We can increase $I_{on}$ by raising $V_{dd}$ and/or lowering $V_t$.



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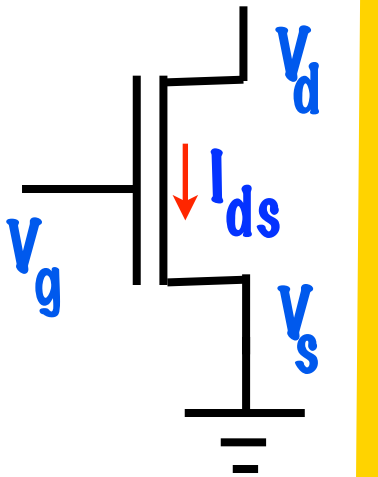
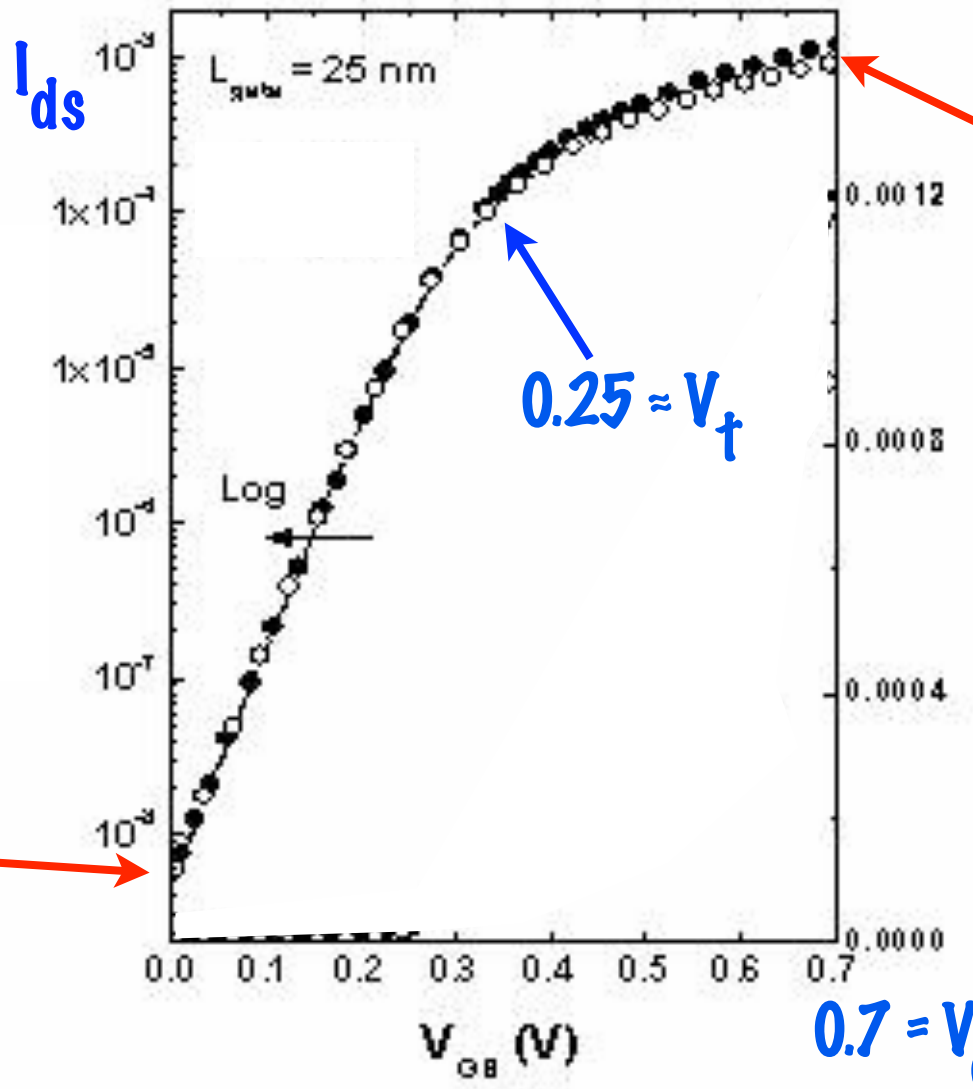
# Plot on a "Log" Scale to See "Off" Current




We can decrease $I_{off}$ by raising $V_t$ - but that lowers $I_{on}$.




$I_{off} \approx 10$ nA



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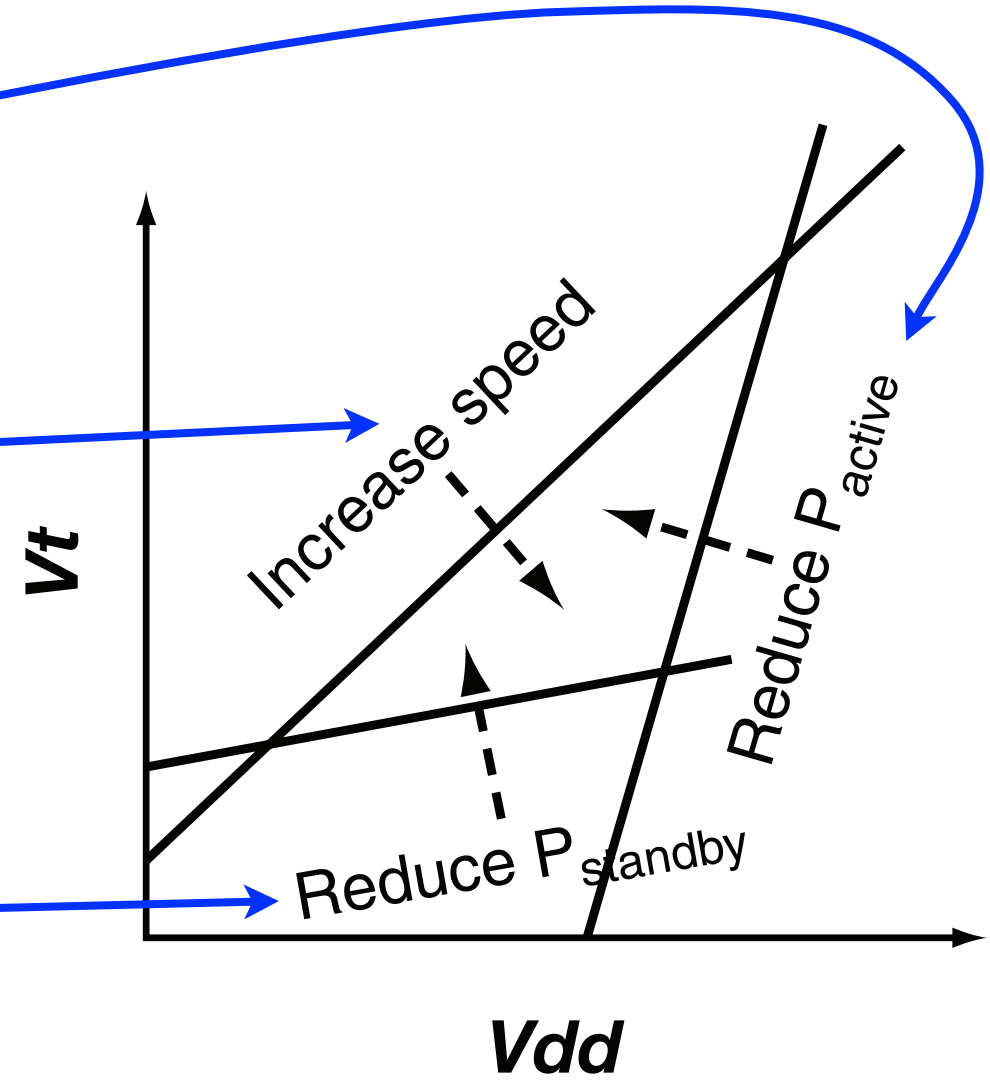
# Device engineers trade speed and power

We can reduce $CV^2$ ($P_{active}$) by lowering $V_{dd}$.

We can increase speed by raising $V_{dd}$ and lowering $V_t$.

We can reduce leakage ($P_{standby}$) by raising $V_t$.




From: Silicon Device Scaling to the Sub-10-nm Regime

Meikei Ieong,[1*] Bruce Doris,[2] Jakub Kedzierski,[1] Ken Rim,[1] Min Yang[1]



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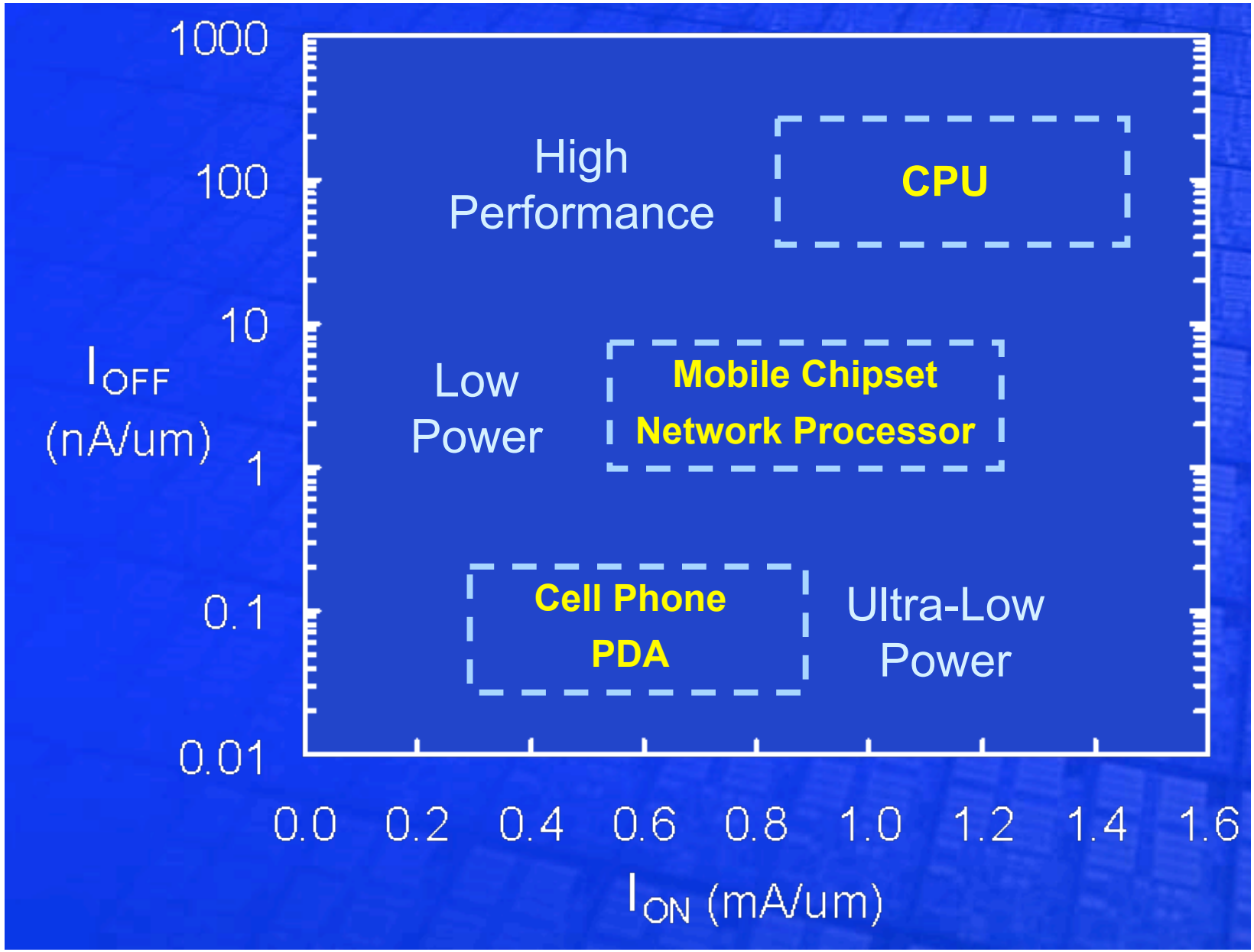
# Customize processes for product types ...




From: "Facing the Hot Chips Challenge Again", Bill Holt, Intel, presented at Hot Chips 17, 2005.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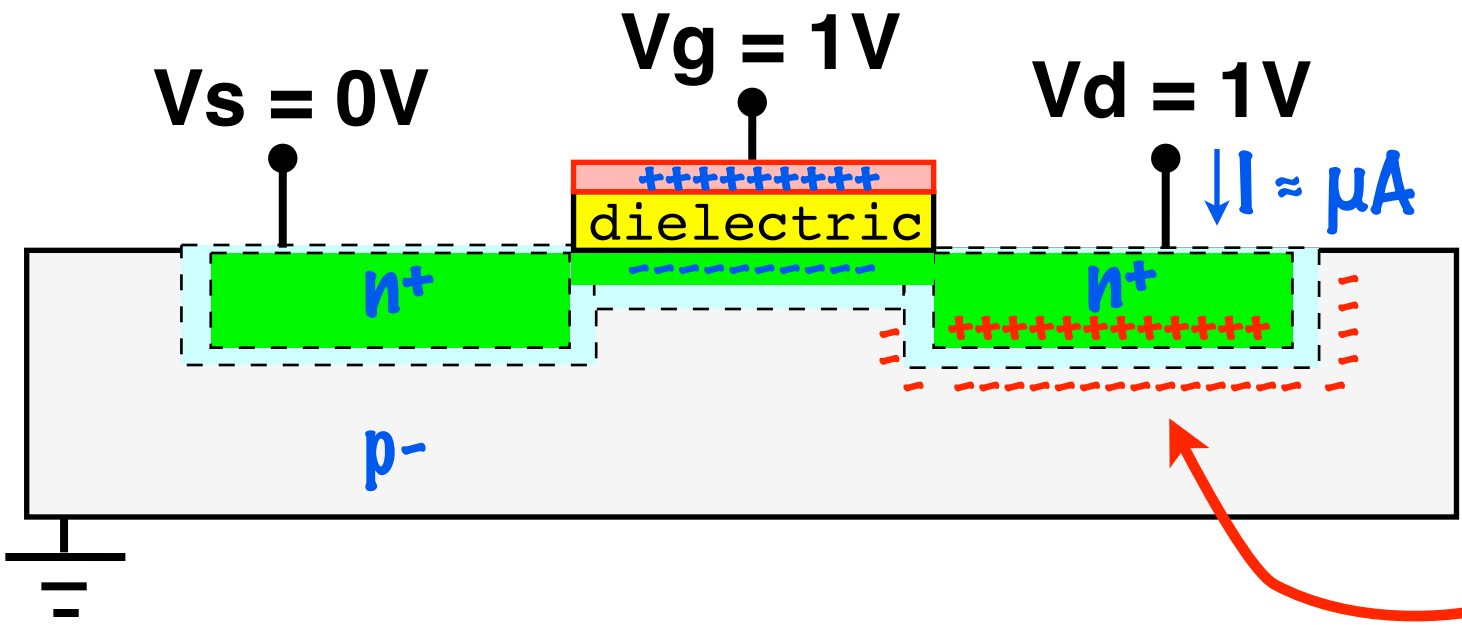
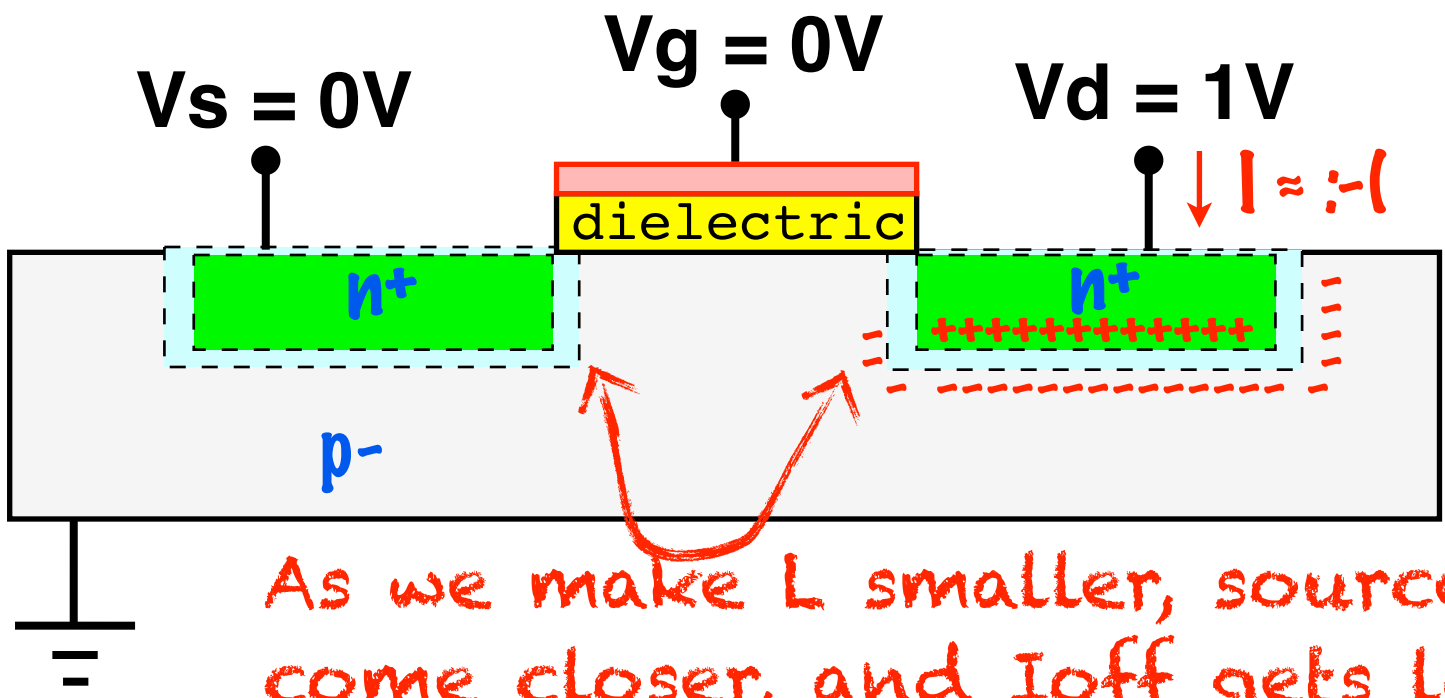
# Transistor physics revisited ...




The drain junction is also a capacitor, and puts - charges in the substrate.




Away from the surface, the drain-induced charges remain even when the gate is off!

As we make L smaller, source and drain come closer, and Ioff gets larger!



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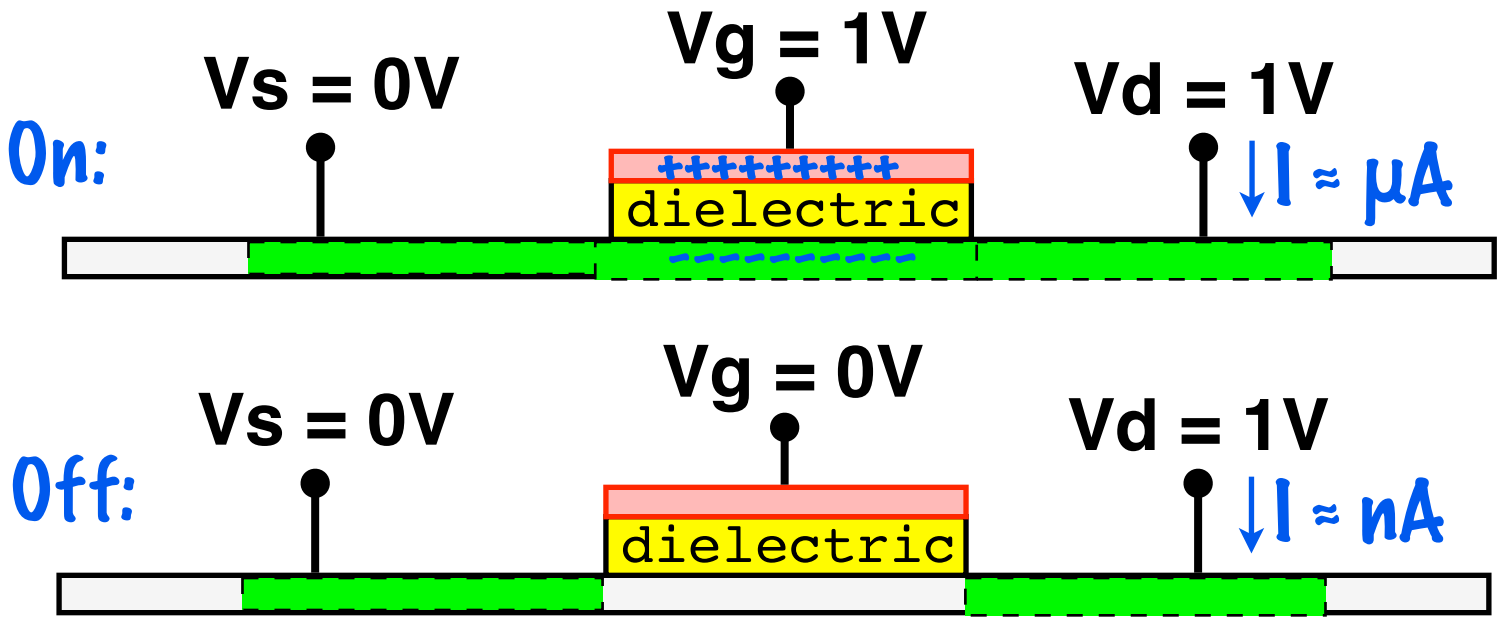
# Solution concept: Fully-depleted channel




**We limit the depth of the channel so that the gate voltage "wins" over the drain voltage.**

**Done as shown, 5 to 7 nm depth for a 20 nm transistor.**

Requires expensive wafers

"FD-SOI" -- Fully-Depleted Silicon-On-Insulator



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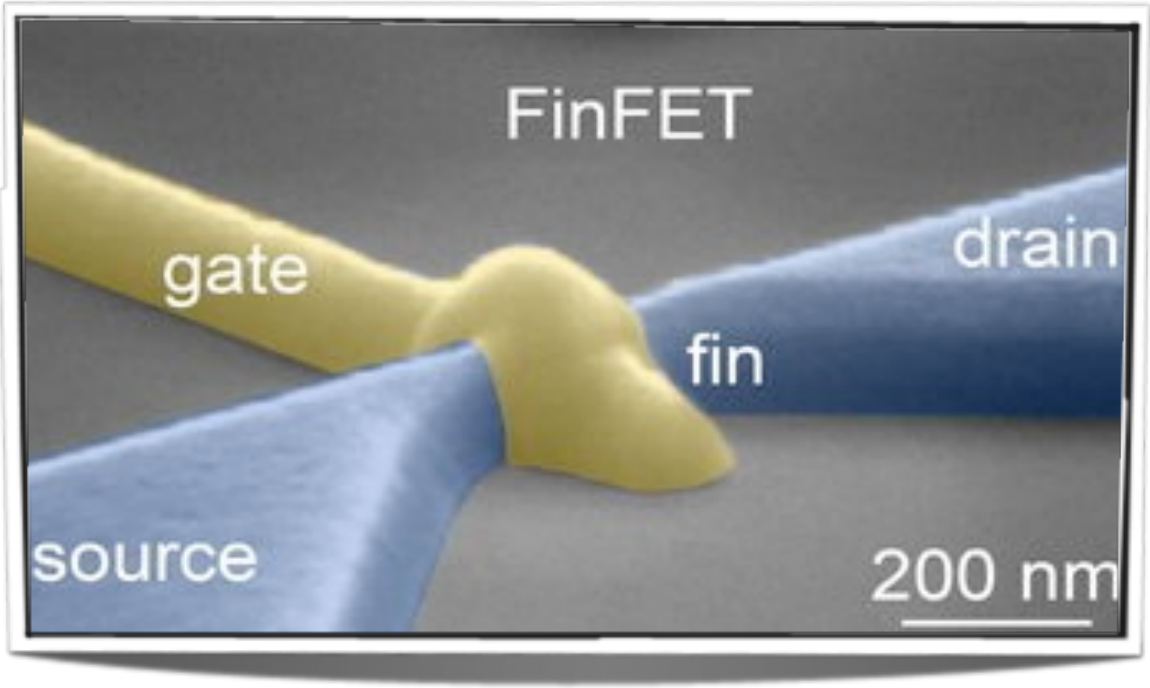
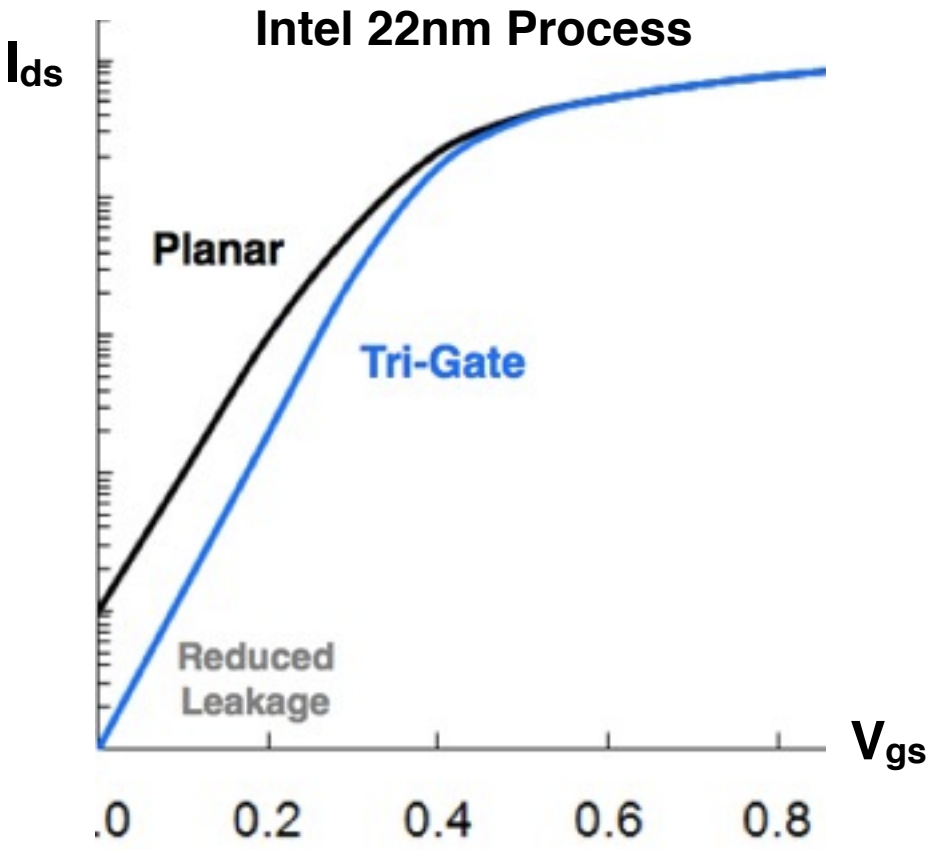



Transistor channel is a raised fin.

Gate controls channel from sides and top.

Channel depth is fin width. 12-15nm for L=22nm.

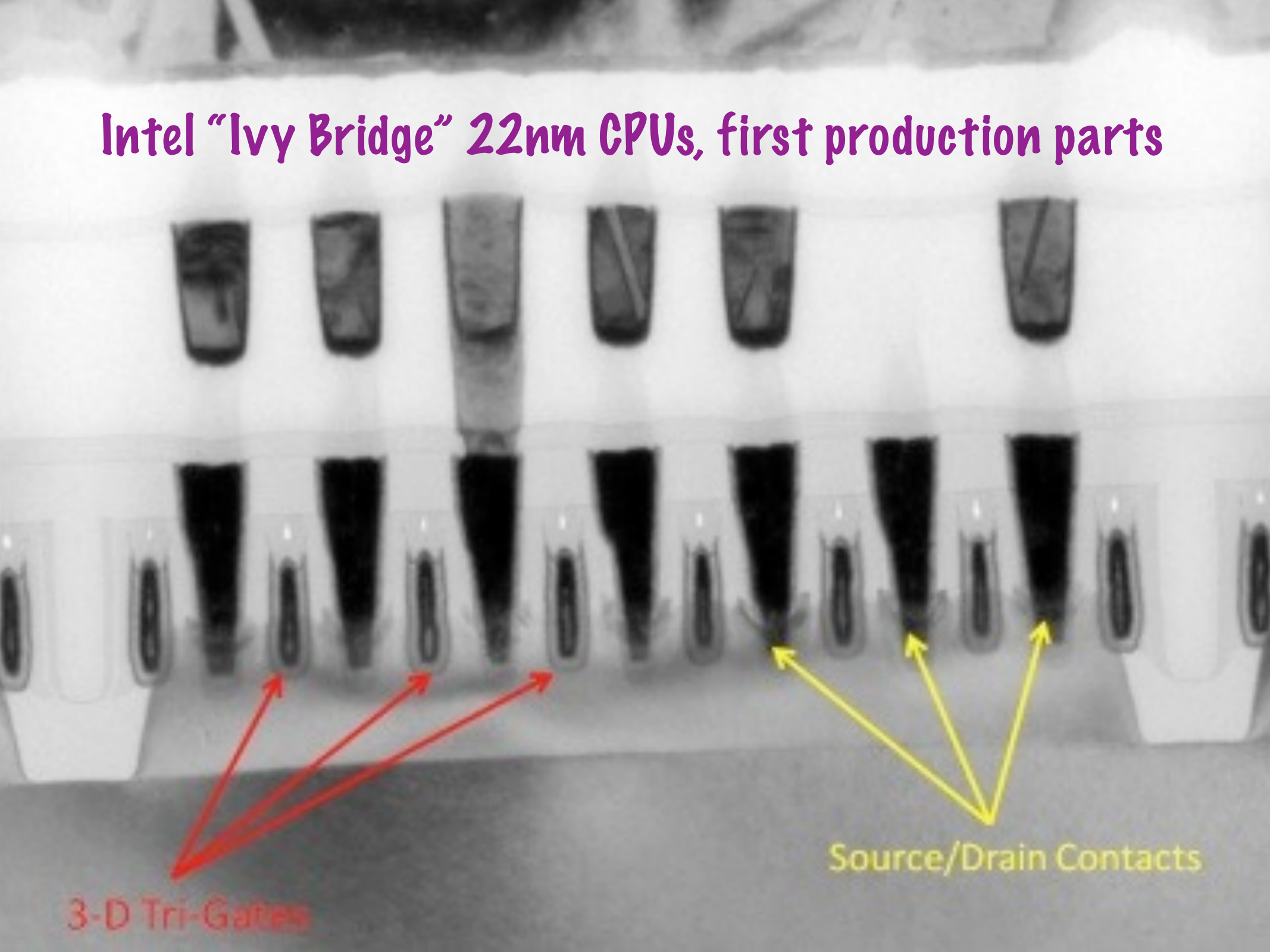



(12) **United States Patent**
**Hu et al.** Filed: **Oct. 23, 2000**

(54) **FINFET TRANSISTOR STRUCTURES HAVING A DOUBLE GATE CHANNEL EXTENDING VERTICALLY FROM A SUBSTRATE AND METHODS OF MANUFACTURE**

(75) Inventors: **Chenming Hu**, Alamo; **Tsu-Jae King**, Fremont; **Vivek Subramanian**, Redwood City; **Leland Chang**, Berkeley; **Xuejue Huang**; **Yang-Kyu Choi**, both of Albany; **Jakub Tadeusz Kedzierski**, Hayward; **Nick Lindert**, Berkeley; **Jeffrey Bokor**, Oakland, all of CA (US); **Wen-Chin Lee**, Beaverton, OR (US)

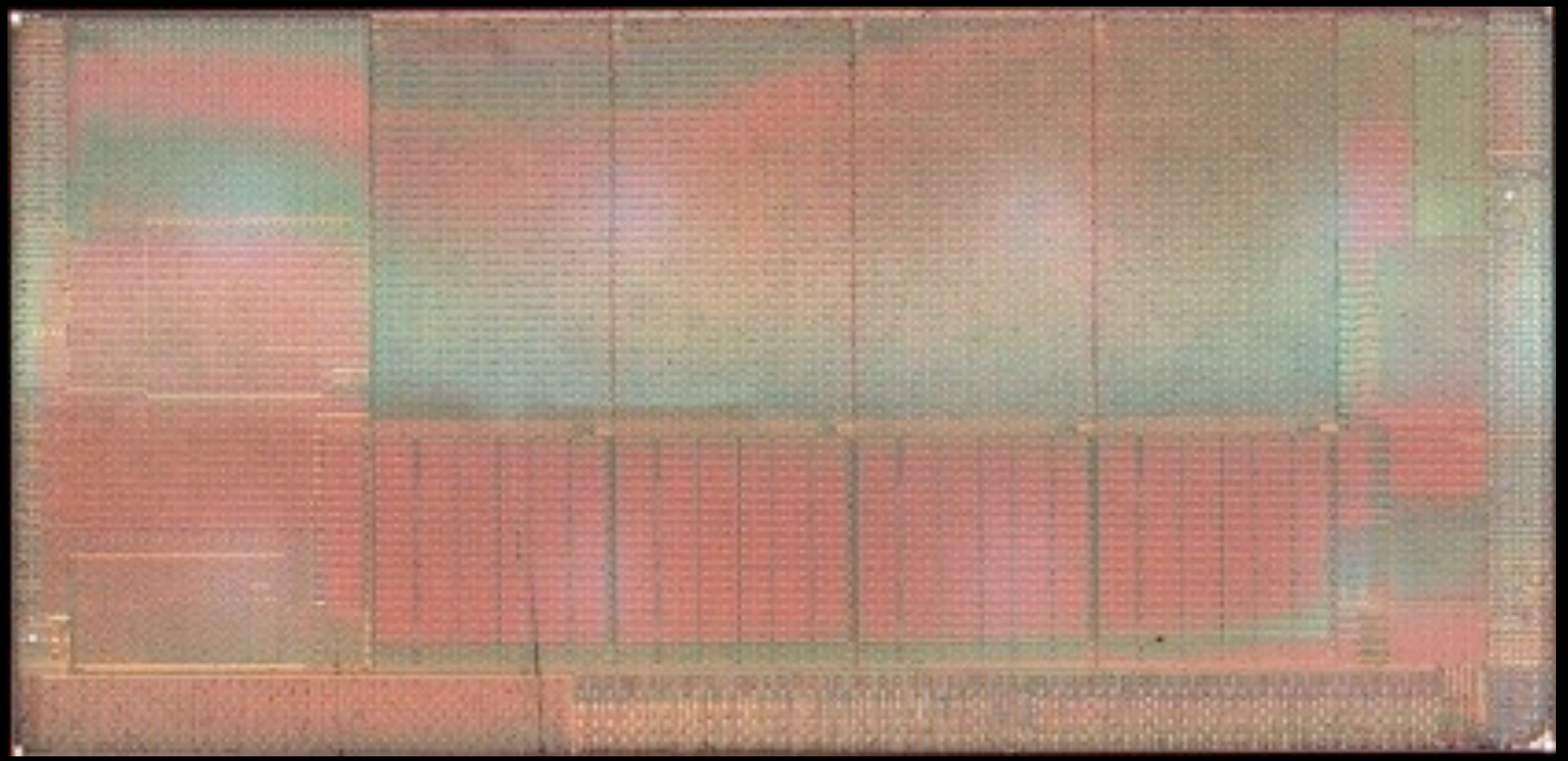
# Intel "Ivy Bridge" 22nm CPUs, first production parts



Sandy Bridge

32nm planar

1.16B transistors

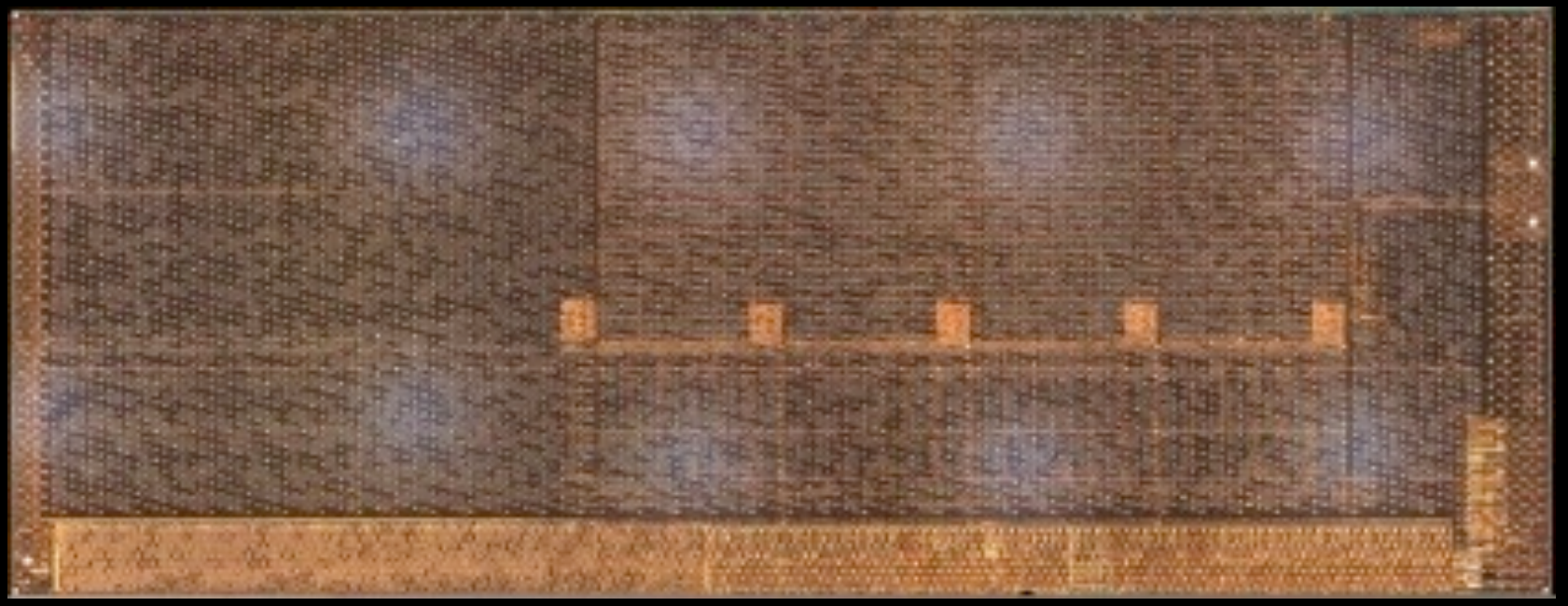


"Less than half the power @ same performance"

Ivy Bridge

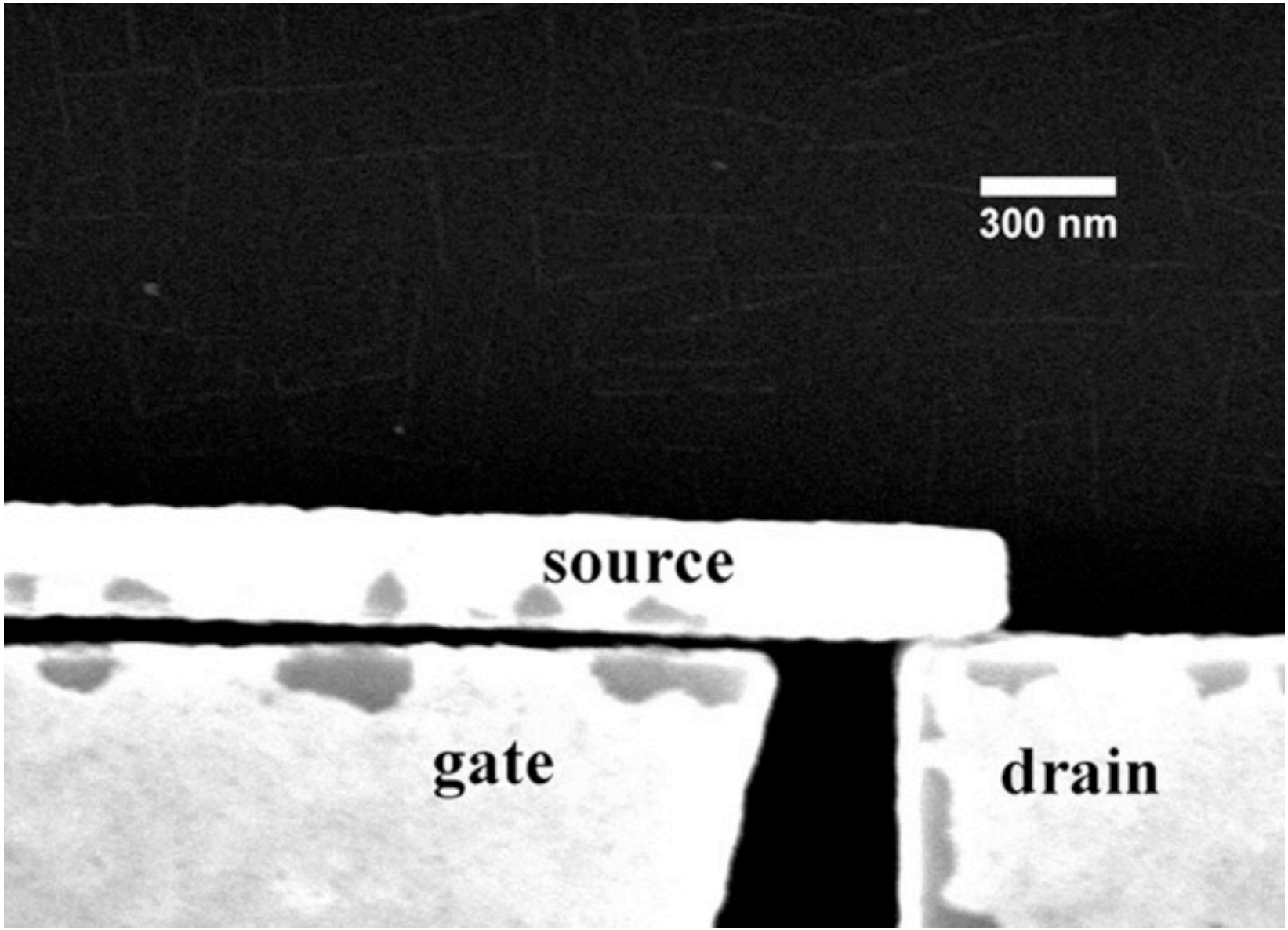
22nm FinFet

1.4B transistors



# Long-term possibility: New devices

## Electrostatic mechanical relays at the nanoscale

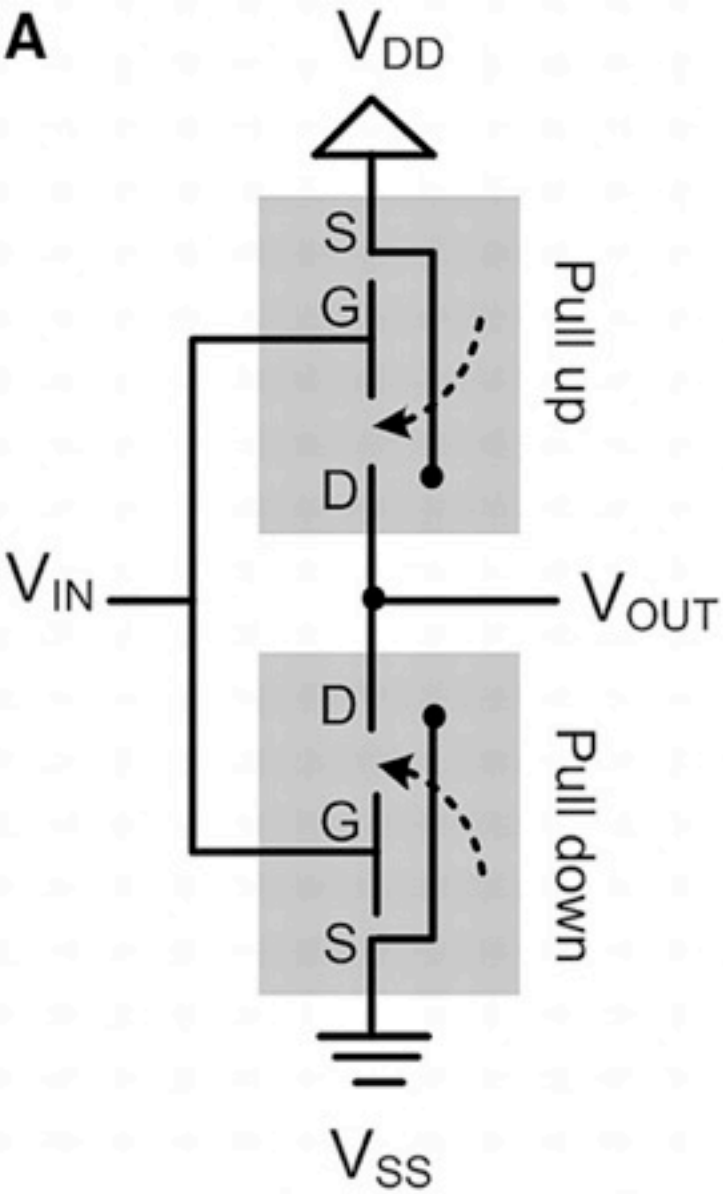


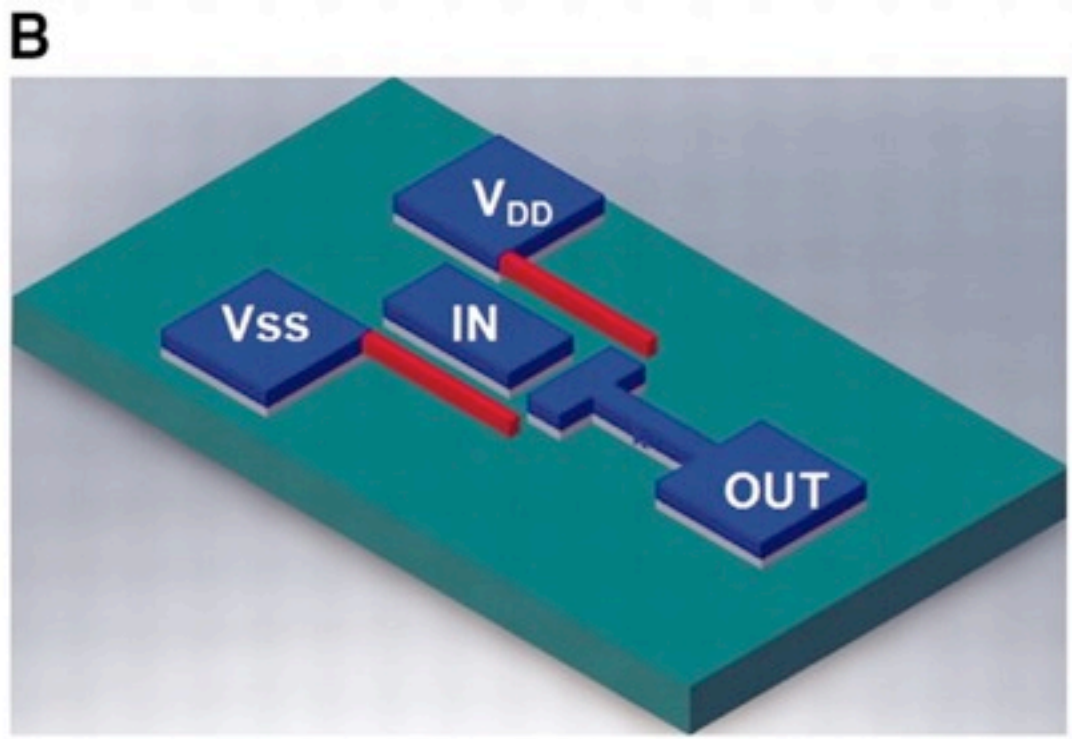

Electromechanical Computing at 500°C with Silicon Carbide. Te-Hao Lee, Swarup Bhunia, Mehran Mehregany



UC Regents Spring 2012 © UCB

# Working inverter at 500 kHz ... for a while.




+ 10 fA leakage current
+ Works at 500 degrees C

- Fails after 1-10 days of 500 kHz toggles.
- Switching requires 6V $V_{dd}$

Electromechanical Computing at 500°C with Silicon Carbide. Te-Hao Lee, Swarup Bhunia, Mehran Mehregany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# Five low-power design techniques

- Parallelism and pipelining
- Power-down idle transistors
- Slow down non-critical paths
- Clock gating
- Thermal management

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# Trading Hardware for Power

via Parallelism and Pipelining ...

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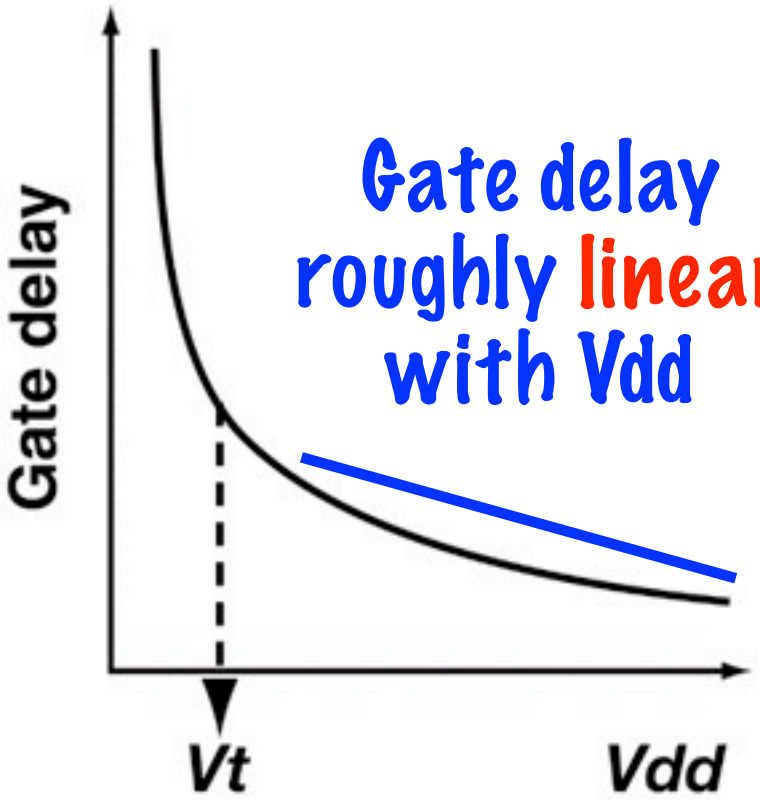



Gate delay roughly linear with Vdd

## And so, we can transform this:

Vdd

Logic Block →

$P \sim F \times V_{dd}^2$

$P \sim 1 \times 1^2$

Freq = 1
Vdd = 1
Throughput = 1
Power = 1
Area = 1
Pwr Den = 1

Block processes stereo audio. 1/2 of clocks for "left", 1/2 for "right".

## Into this:

Top block processes "left", bottom "right".

Vdd/2

Logic Block →

Logic Block →

Freq = 0.5
Vdd = 0.5
Throughput = 1
Power = 0.25
Area = 2
Pwr Den = 0.125

$P \sim \#blks \times F \times V_{dd}^2$

$P \sim 2 \times 1/2 \times 1/4 = 1/4$

$CV^2$ power only

THIS MAGIC TRICK BROUGHT TO YOU BY CORY HALL ...

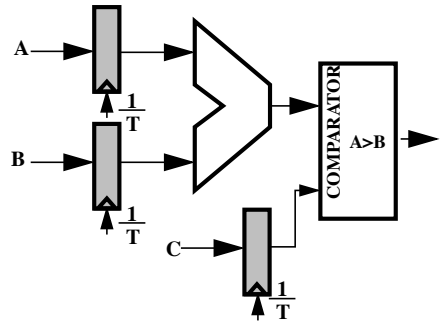

UC Regents Spring 2012 © UCB

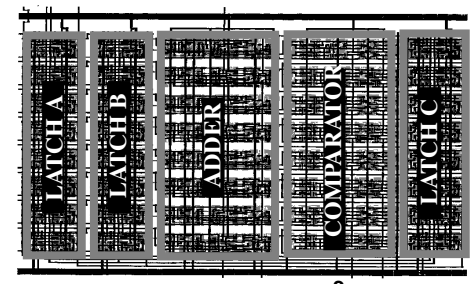
# Chandrakasan & Brodersen (UCB, 1992)

| Architecture | Power (normalized) |
|---|---|
| Simple | 1 |
| Parallel | 0.36 |
| Pipelined | 0.39 |
| Pipelined-Parallel | 0.2 |

| Architecture | Area (normalized) |
|---|---|
| Simple | 1 |
| Parallel | 3.4 |
| Pipelined | 1.3 |
| Pipelined-Parallel | 3.7 |

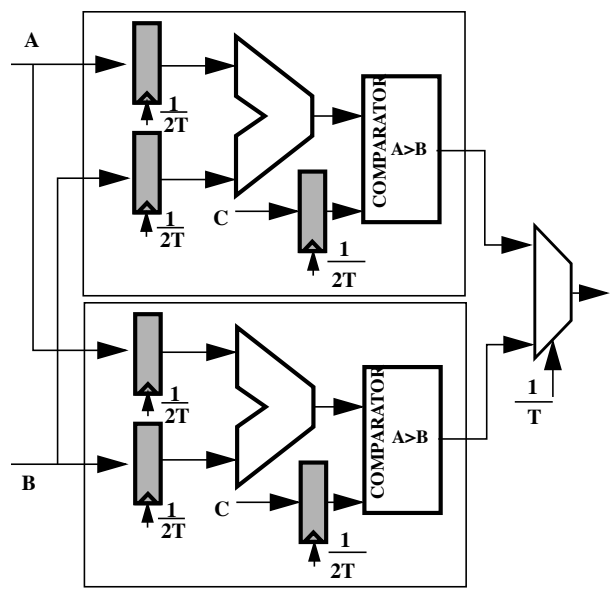
| Architecture | Voltage |
|---|---|
| Simple | 5V |
| Parallel | 2.9V |
| Pipelined | 2.9V |
| Pipelined-Parallel | 2.0 |

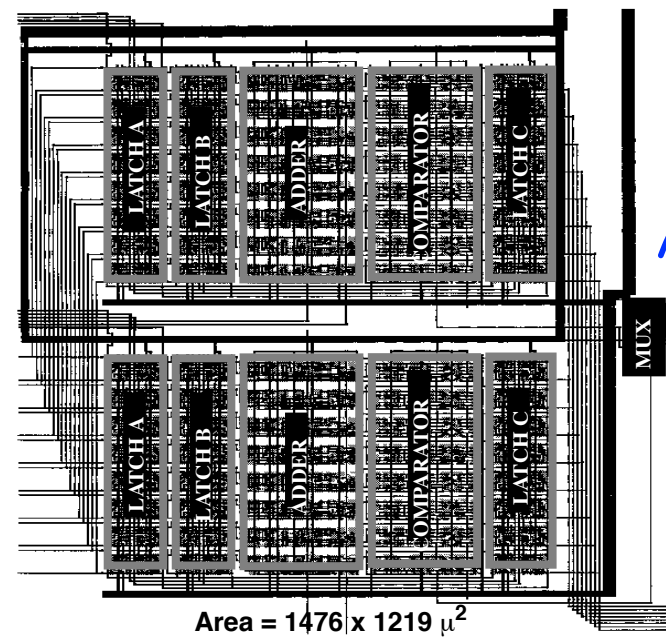



Area = 636 x 833 $\mu^2$

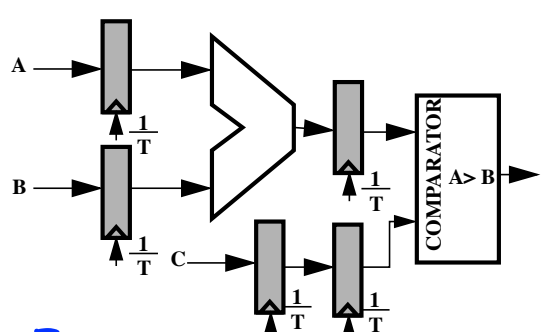
Simple

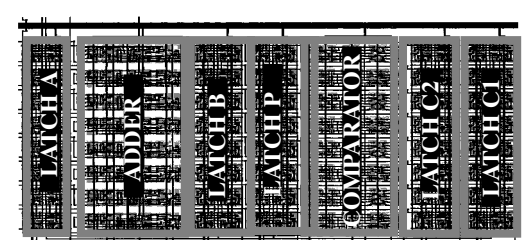



Area = 1476 x 1219 $\mu^2$

Parallel




Area = 640 x 1081 $\mu^2$

Pipelined

From:

**Minimizing Power Consumption in CMOS Circuits** Anantha P. Chandrakasan, Robert W. Brodersen



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# Multiple Cores for Low Power

Trade hardware for power,
on a large scale ...

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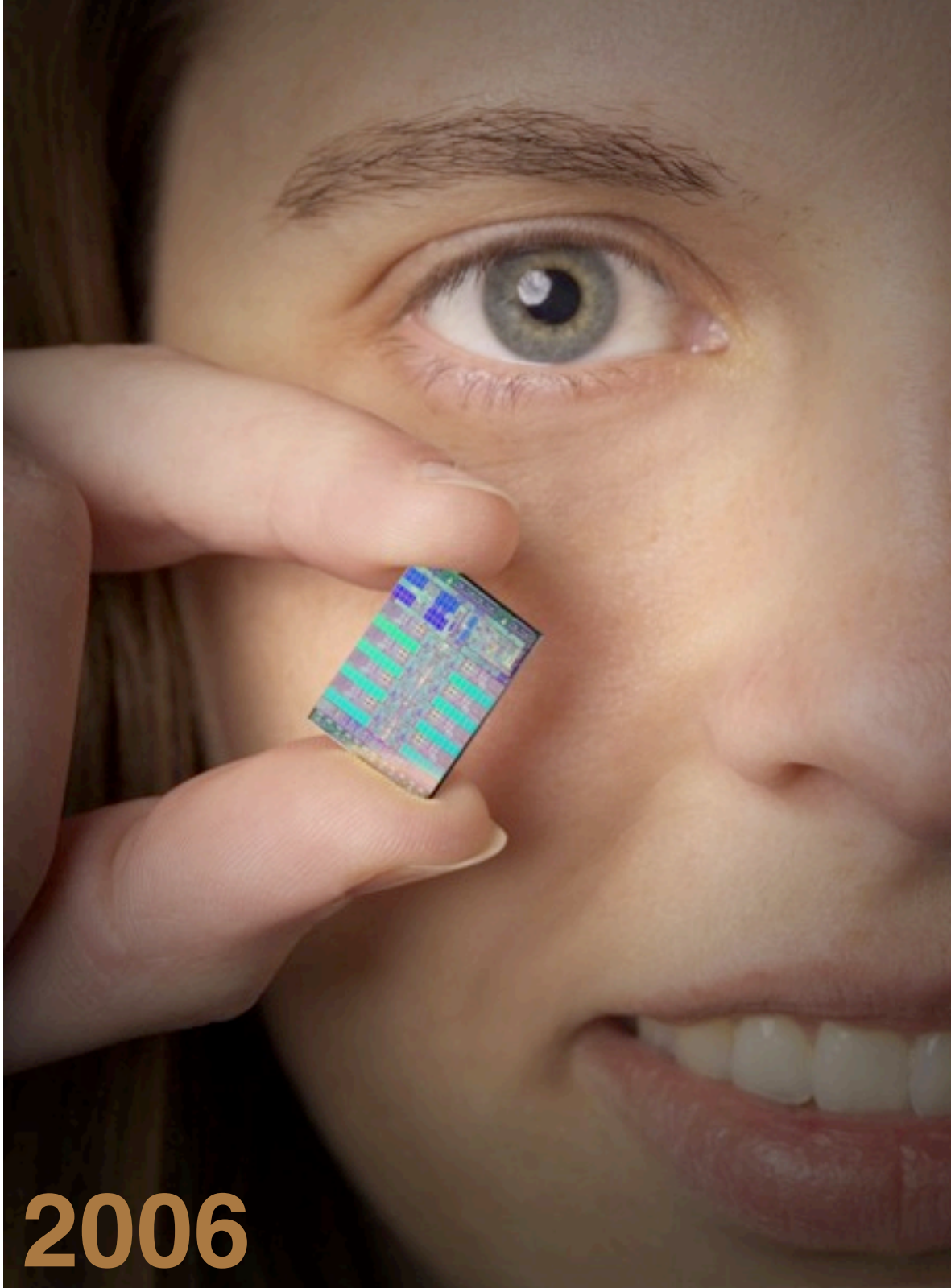
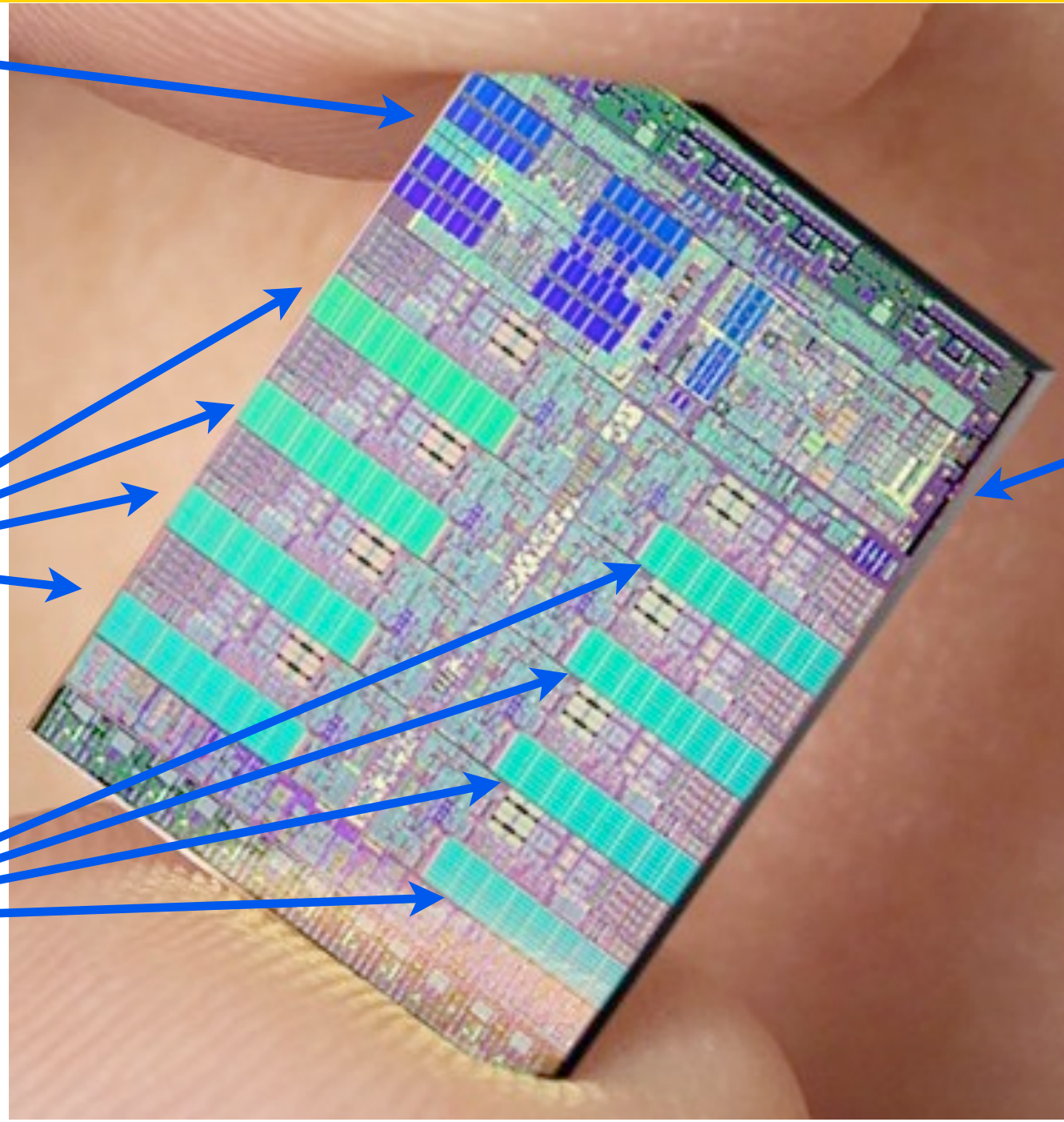
# Cell: The PS3 chip



# Cell (PS3 Chip): 1 CPU + 8 "SPUs"



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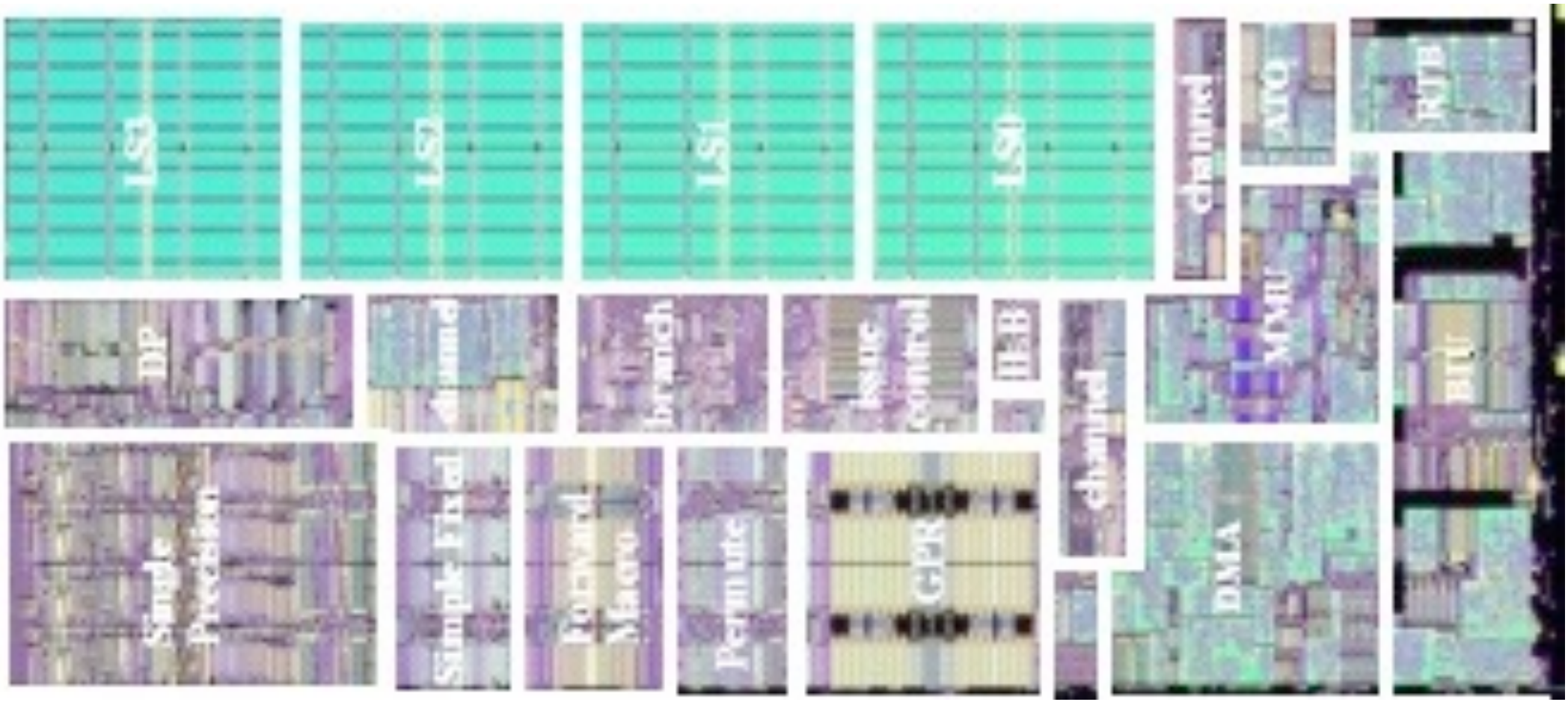
# One Synergistic Processing Unit (SPU)




SPU issues 2 inst/cycle (in order) to 7 execution units

256 KB Local Store, 128 128-bit Registers

SPU fills Local Store using DMA to DRAM and network



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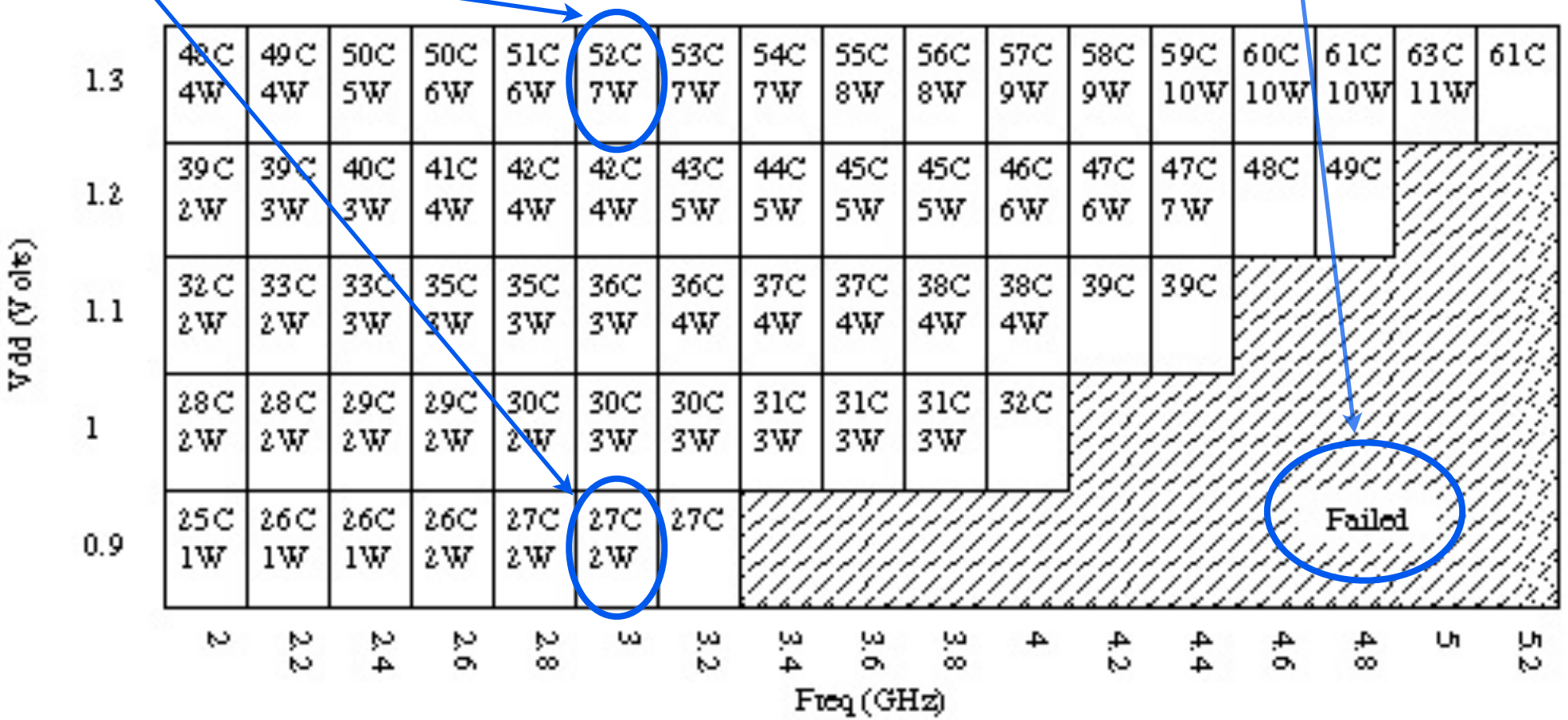
# A "Schmoo" plot for a Cell SPU ...

The lower Vdd, the less dynamic energy consumption.

$$E_{0\to1} = \frac{1}{2} C V_{dd}^2 \qquad E_{1\to0} = \frac{1}{2} C V_{dd}^2$$

The lower Vdd, the longer the maximum clock period, the slower the clock frequency.



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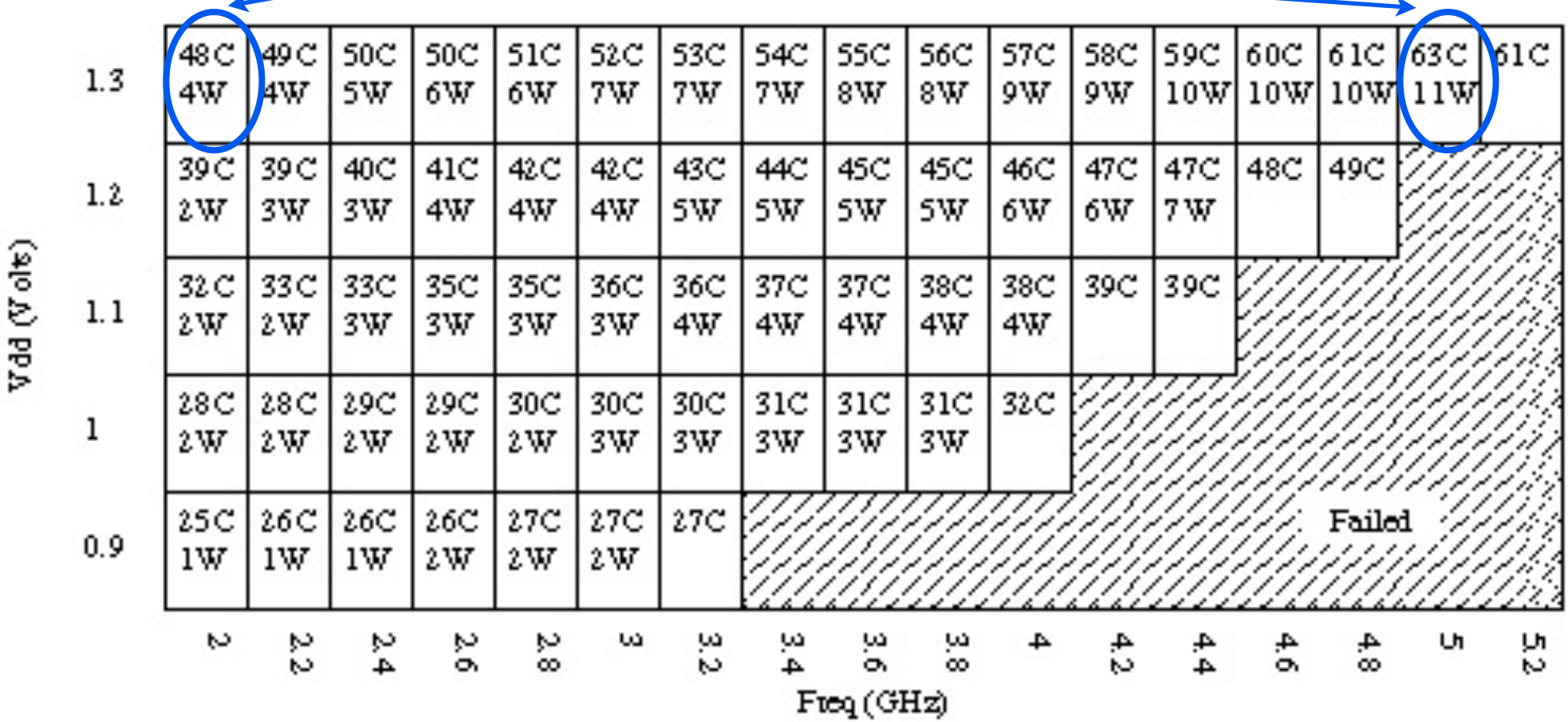
# Clock speed alone doesn't help E/op ...

But, lowering clock frequency while keeping voltage constant spreads the same amount of work over a longer time, so chip stays cooler ...

$$E_{0->1} = \frac{1}{2} C V_{dd}^2 \qquad E_{1->0} = \frac{1}{2} C V_{dd}^2$$



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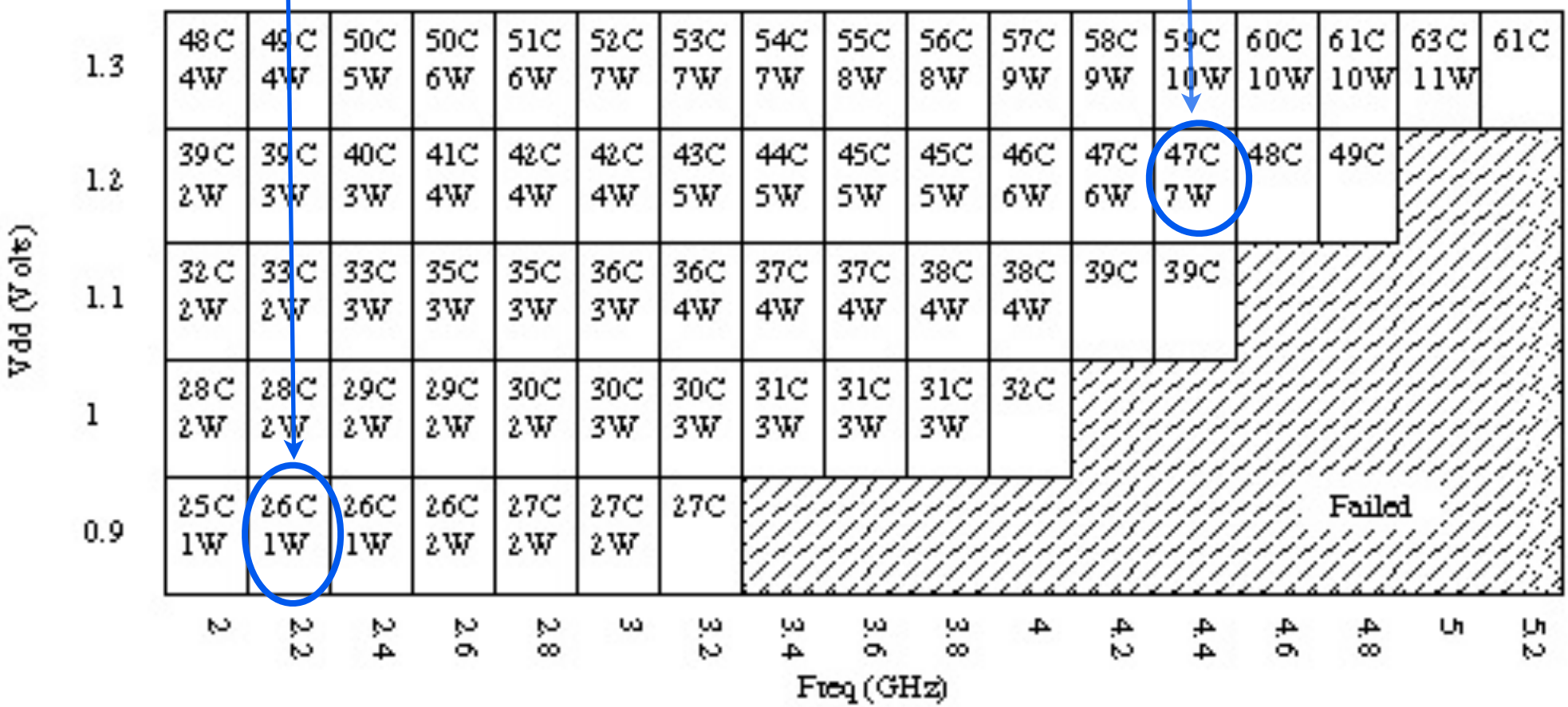
# Scaling V and f *does* lower energy/op

1 W to get 2.2 GHz performance. 26 C die temp.

7W to reliably get 4.4 GHz performance. 47C die temp.

If a program that needs a 4.4 Ghz CPU can be recoded to use two 2.2 Ghz CPUs ... big win.



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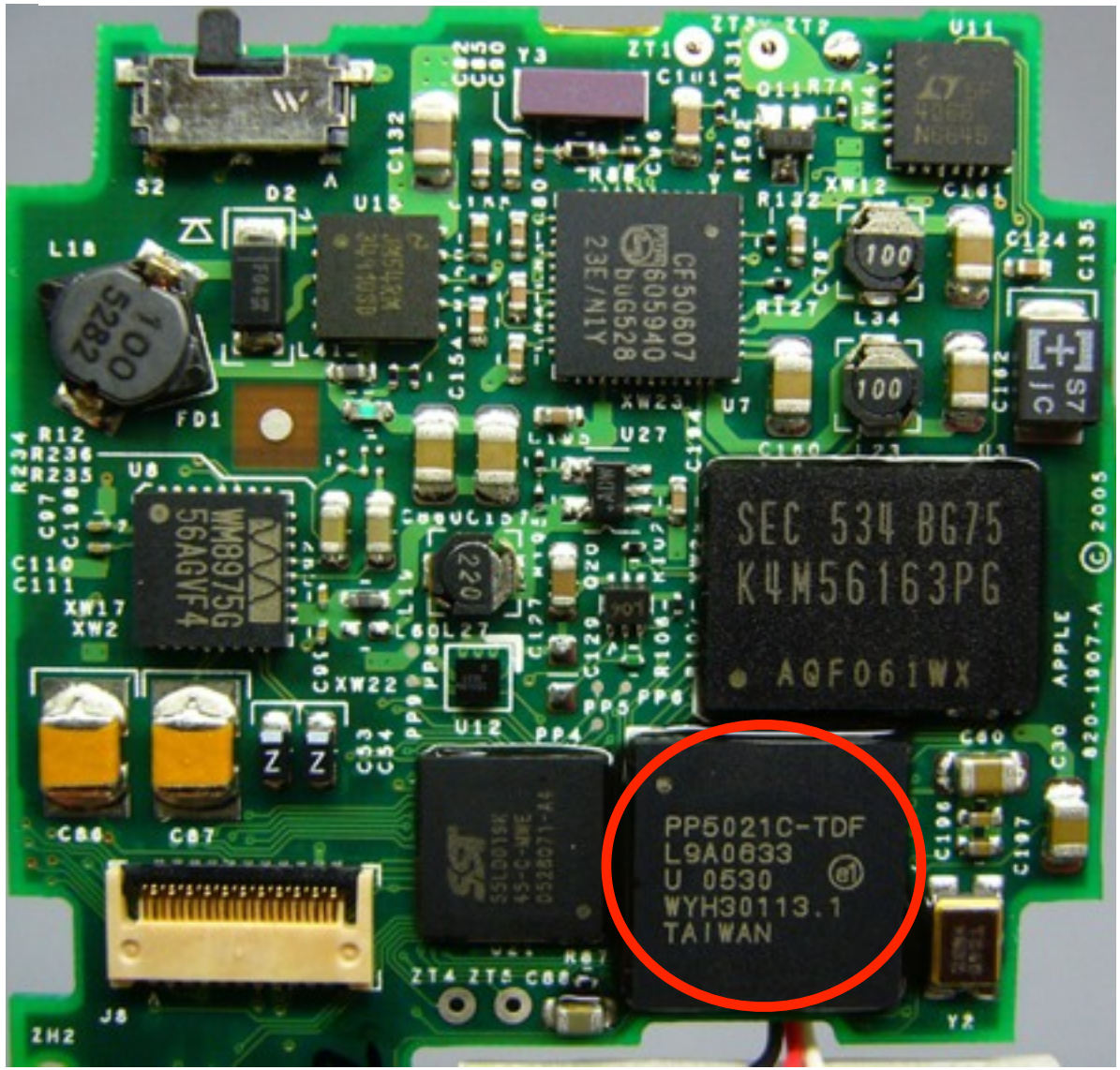
# How iPod nano 2005 puts its 2 cores to use ...

portalplayer™

**PP5020**

digital media management system-on-chip




## Dual ARM Processors

- Dual 32-bit ARM7TDMI processors
- Up to 80 MHz processor operation per core with independent clock-skipping feature on COP
- Efficient cross-bar implementation providing zero wait state access to internal RAM
- Integrated 96KB of SRAM
- 8KB of unified cache per processor
- Six DMA channels

Two 80 MHz CPUs. Was used in several nano generations, with one CPU doing audio decoding, the other doing photos, etc.



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# Powering down idle circuits

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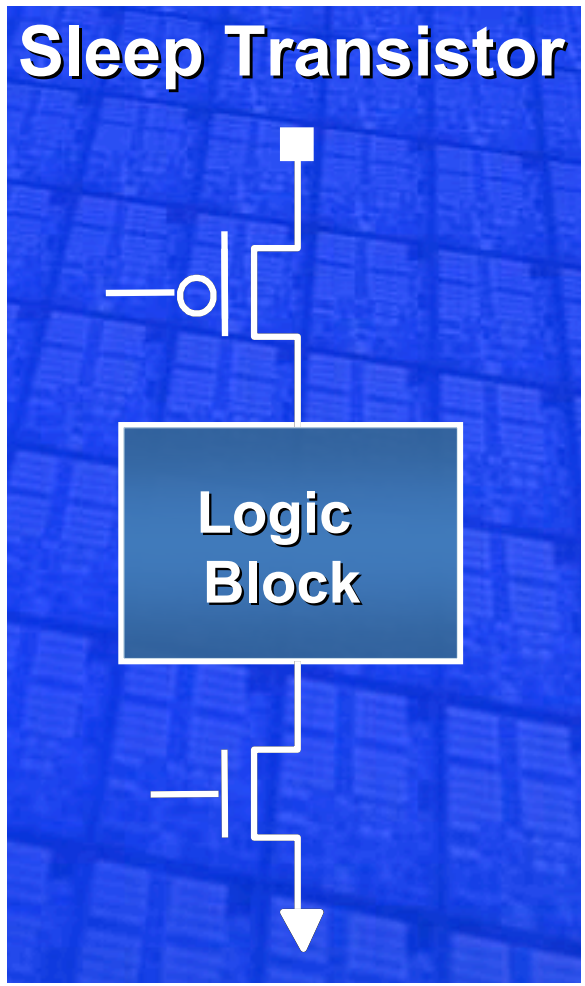
# Add “sleep” transistors to logic ...




Example: Floating point unit logic.

When running fixed-point instructions, put logic “to sleep”.

+++ When “asleep”, leakage power is dramatically reduced.

--- Presence of sleep transistors slows down the clock rate when the logic block is in use.



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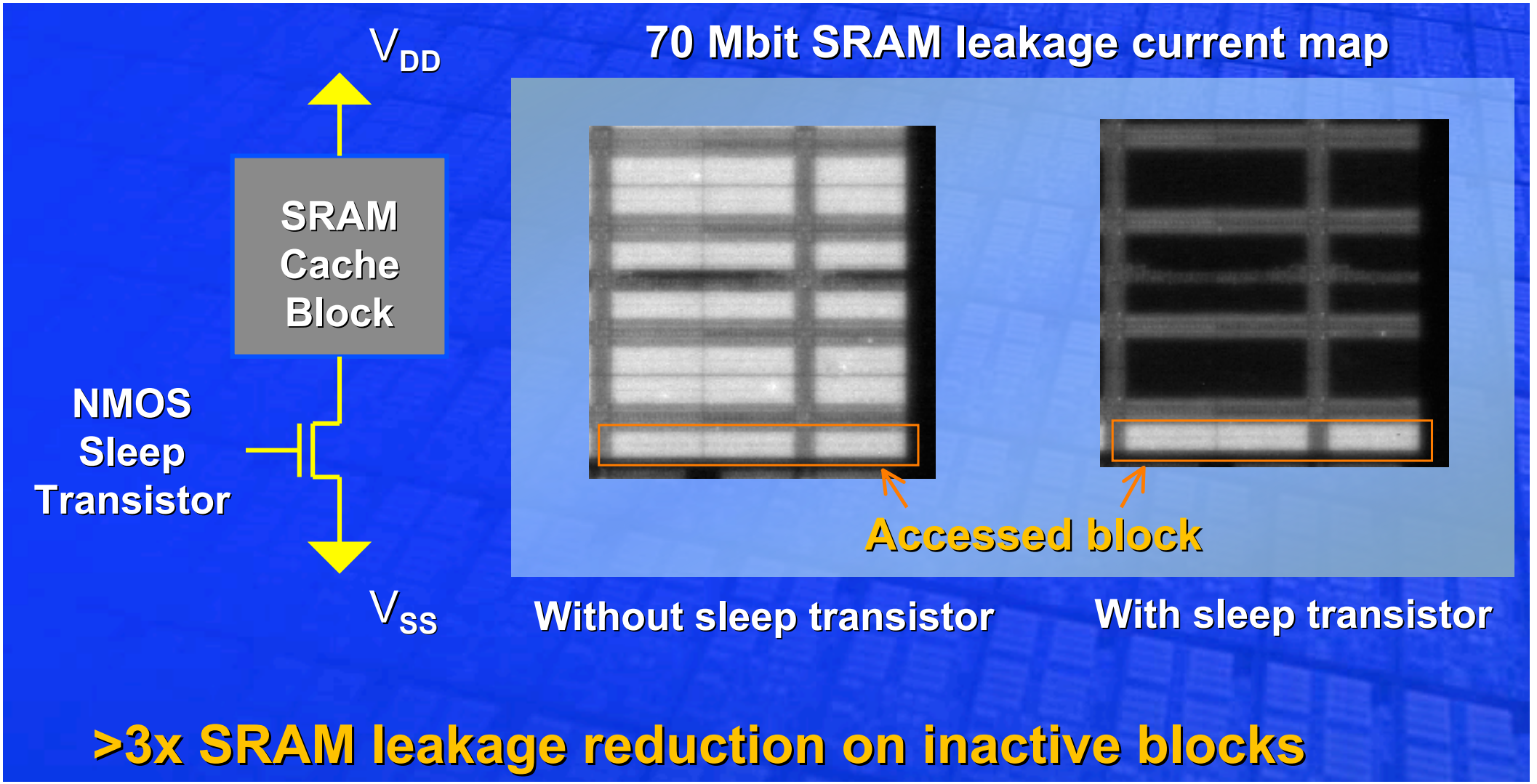
# Intel example: Sleeping cache blocks




From: "Facing the Hot Chips Challenge Again", Bill Holt, Intel, presented at Hot Chips 17, 2005.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# Slow down "slack paths"

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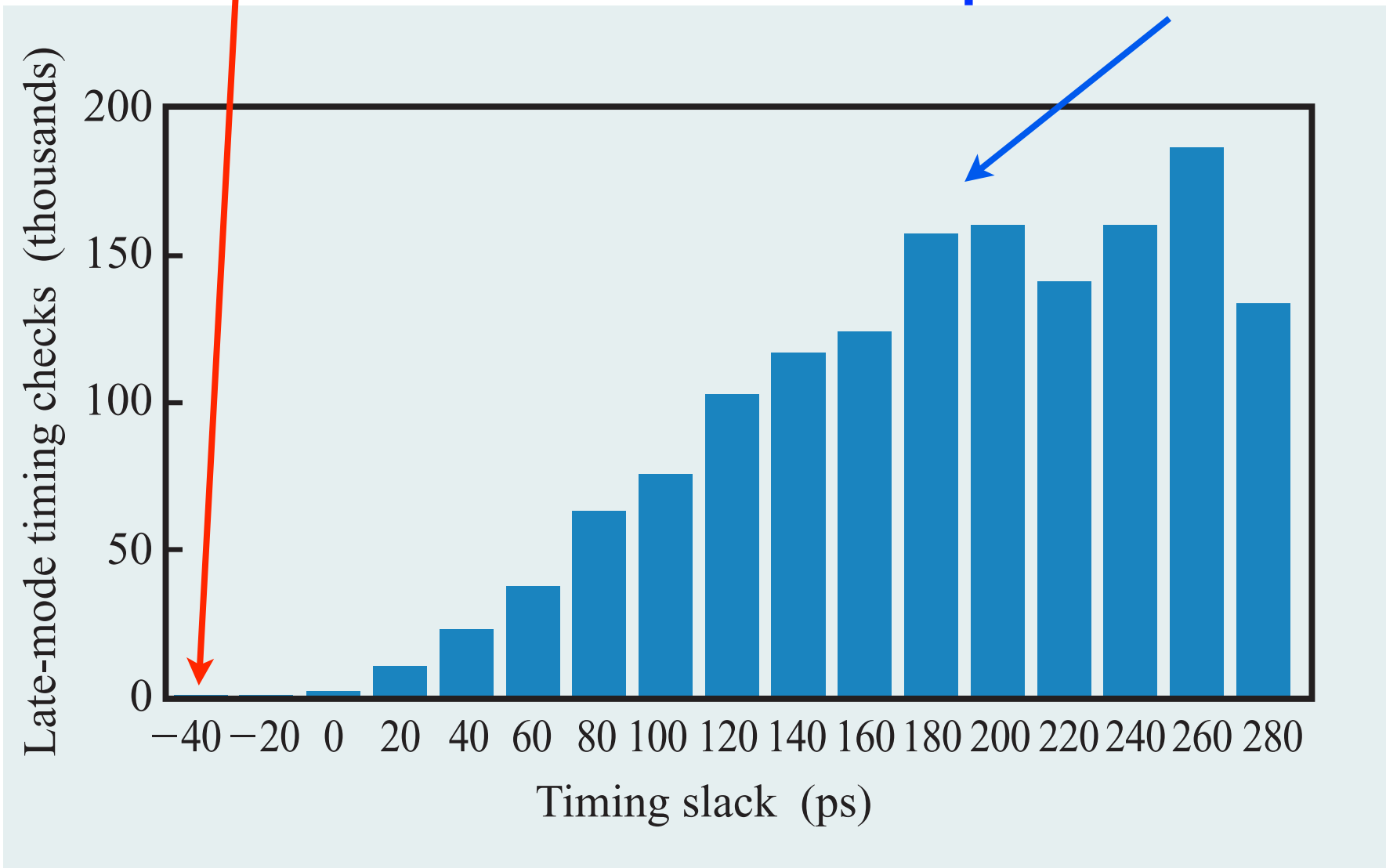
# Fact: Most logic on a chip is "too fast"

The critical path

Most wires have hundreds of picoseconds to spare.




*From "The circuit and physical design of the POWER4 microprocessor", IBM J Res and Dev, 46:1, Jan 2002, J.D. Warnock et al.*



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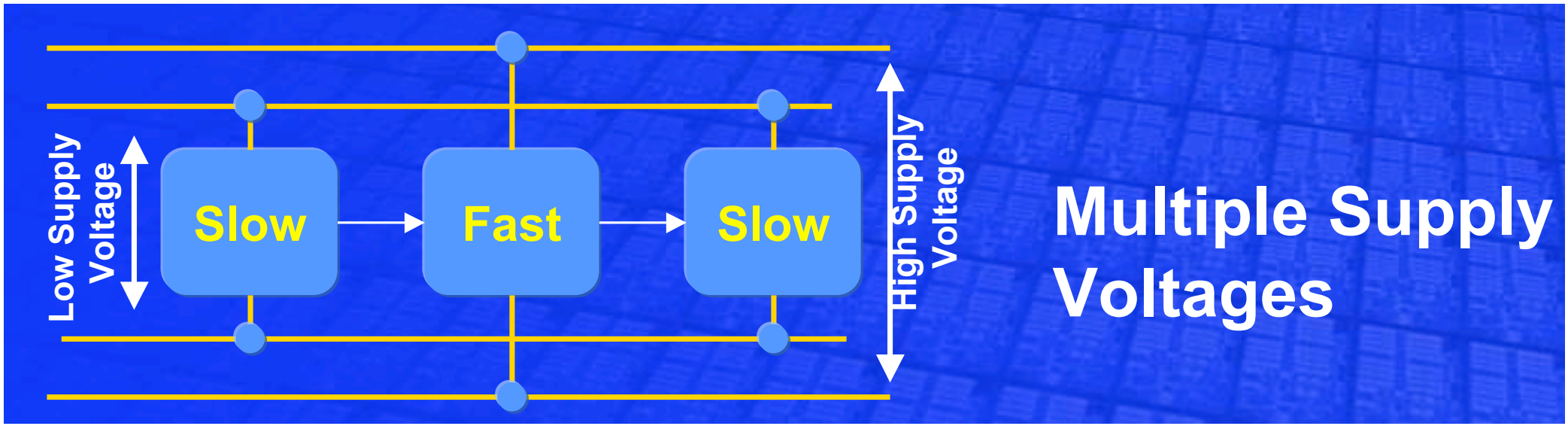
# Use several supply voltages on a chip …




Why use multi-Vdd? We can reduce dynamic power by using low-power Vdd for logic off the critical path.

What if we can't do a multi-Vdd design?
In a multi-Vt process, we can reduce leakage power on the slow logic by using high-Vth transistors.

From: "Facing the Hot Chips Challenge Again", Bill Holt, Intel, presented at Hot Chips 17, 2005.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# LOW POWER ARM 1136JF-S™ DESIGN

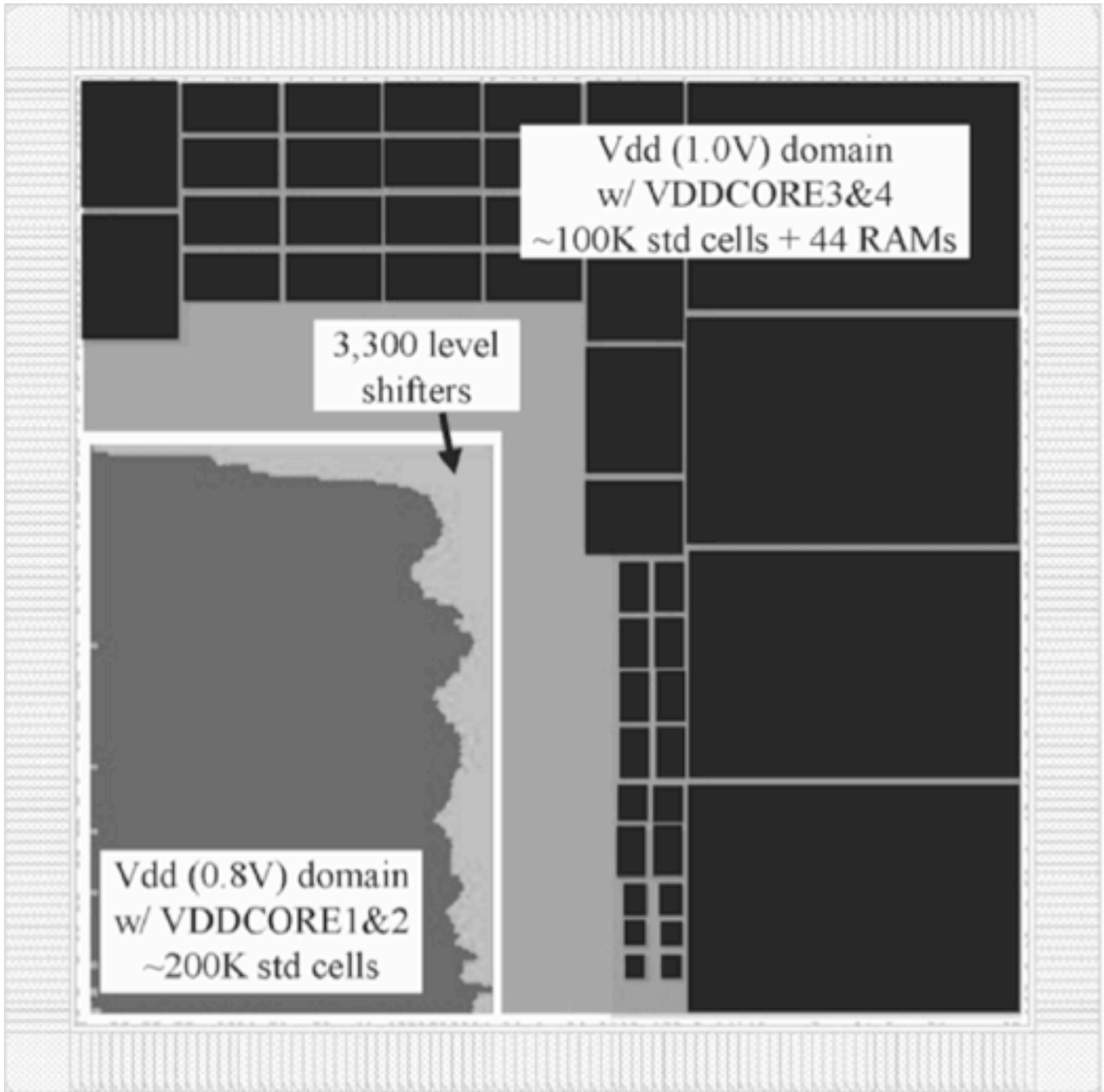
George Kuo, Anand Iyer
*Cadence Design Systems, Inc.*
*San Jose, CA 95134, USA*

Logical partition into 0.8V and 1.0V nets done manually to meet 350 MHz spec (90nm).

Level-shifter insertion and placement done automatically.

Dynamic power in 0.8V section cut 50% below baseline.

Leakage power in 1.0V section cut 70% below baseline.




From a chapter from new book on ASIC design by Chinnery and Keutzer (UCB).



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# Gating clocks to save power

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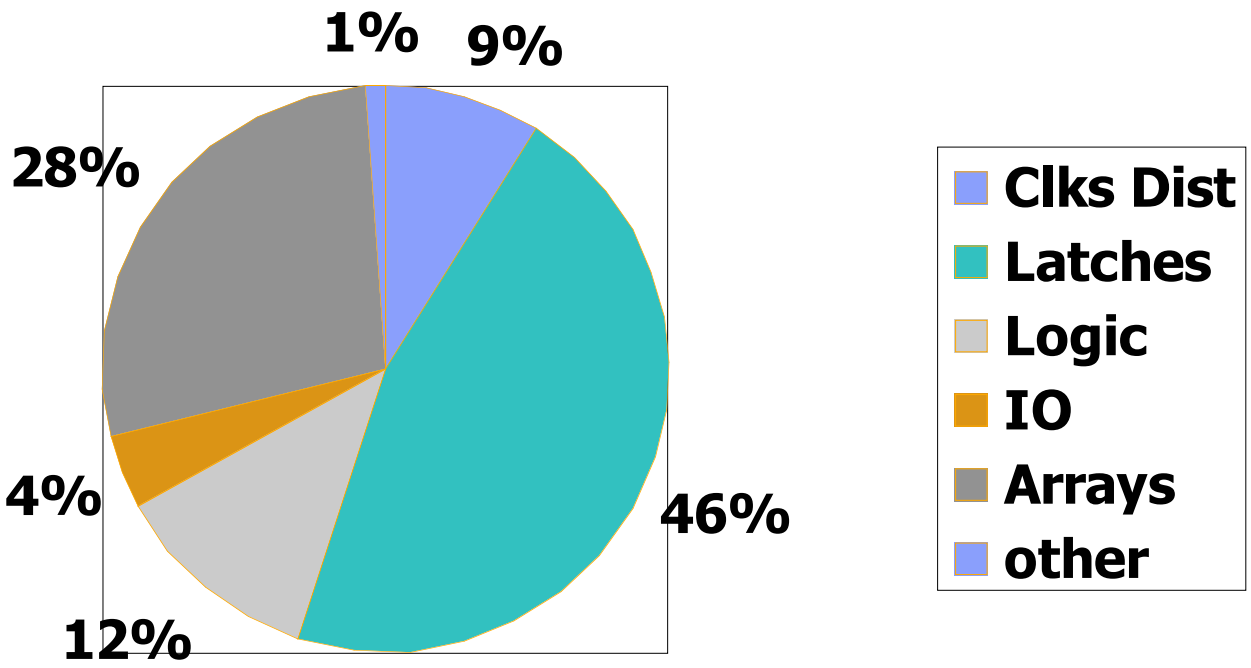
# On a CPU, where does the power go?




Half of the power goes to latches (Flip-Flops).

Most of the time, the latches don't change state.

So (gasp) gated clocks are a big win.
But, done with CAD tools in a disciplined way.

From: Bose, Martonosi, Brooks: Sigmetrics-2001 Tutorial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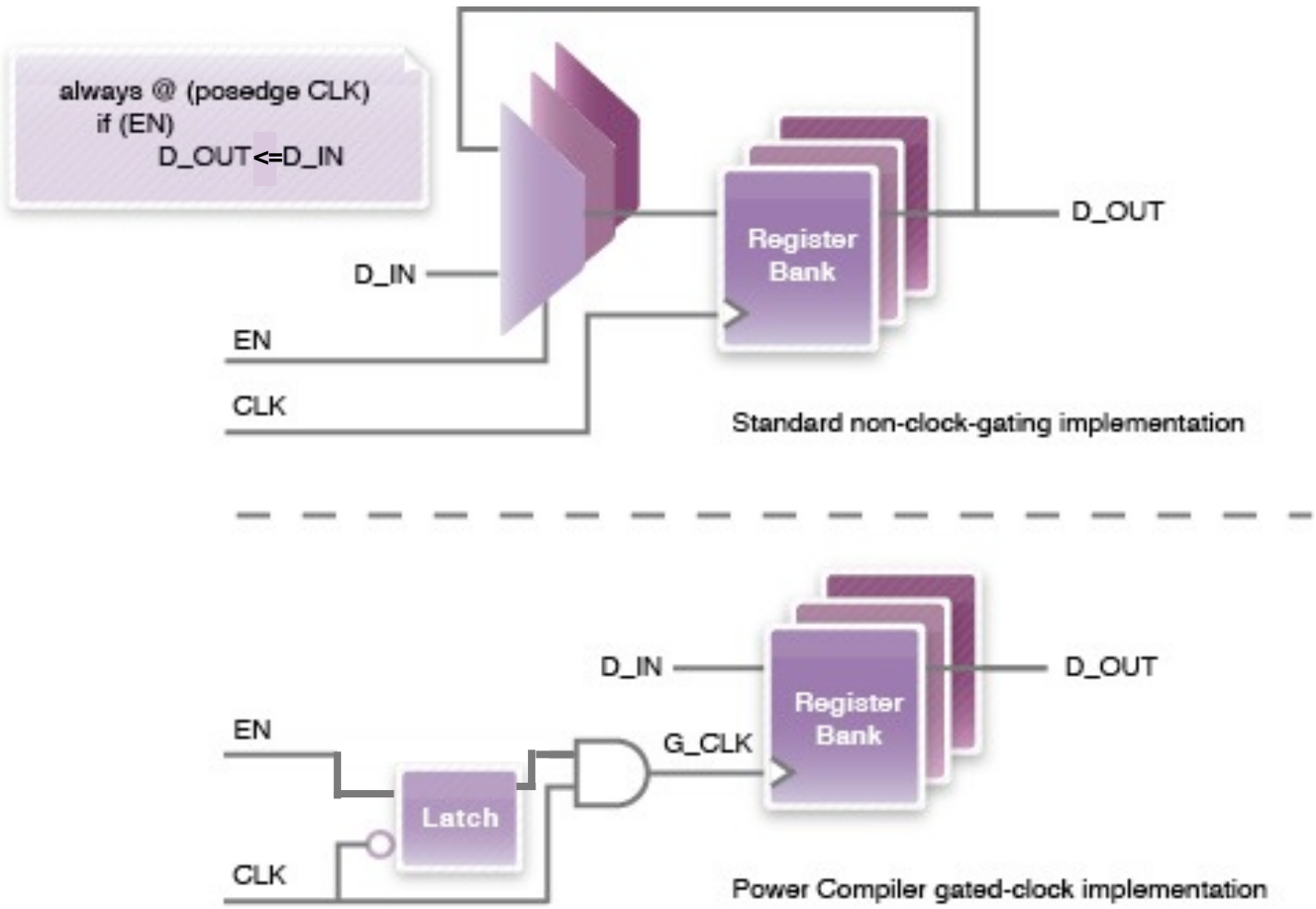
# Synopsis Power Compiler can do this ...




"Up to 70% power savings at the block level, for applicable circuits" Synopsis Data Sheet

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# Thermal Management

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# Keep chip cool to minimize leakage power

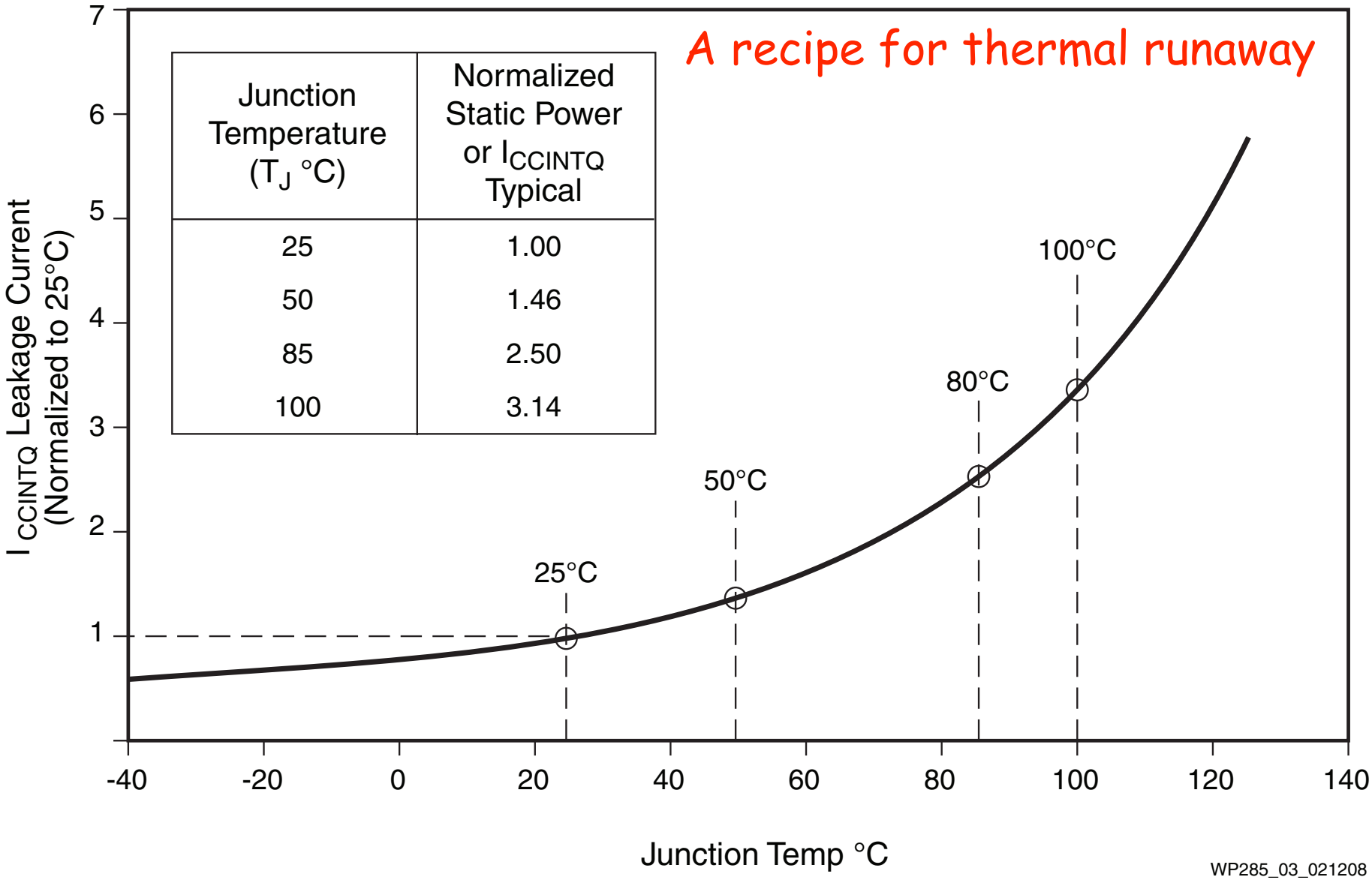
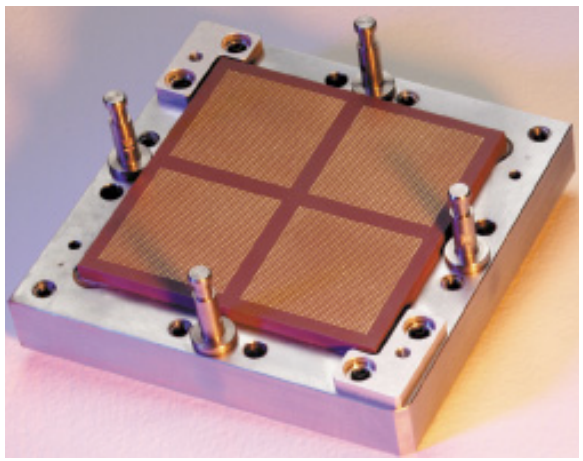


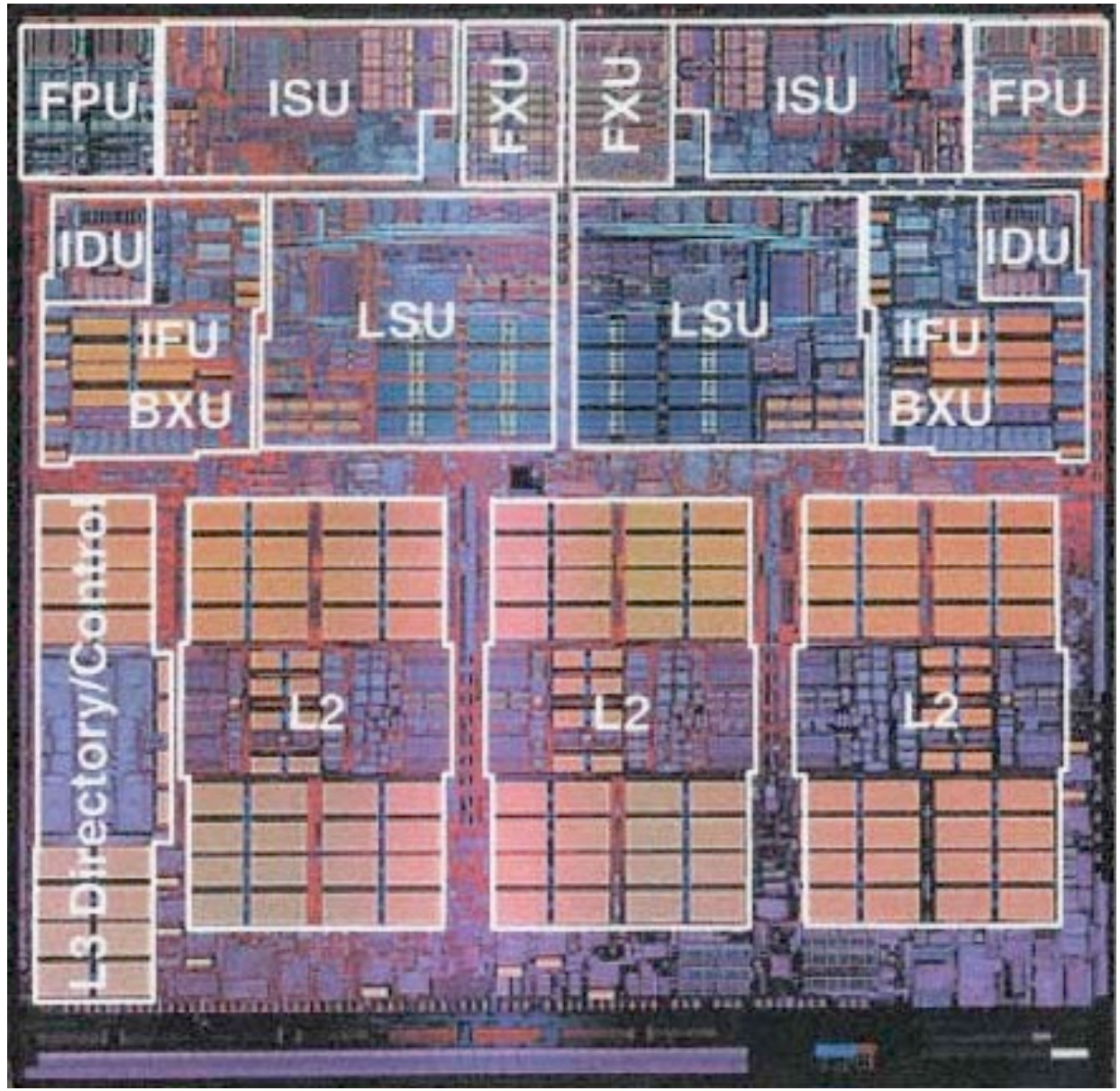

*Figure 3:* **$I_{CCINTQ}$ vs. Junction Temperature with Increase Relative to 25°C**

# IBM Power 4: How does die heat up?



4 dies on a multi-chip module

2 CPUs per die



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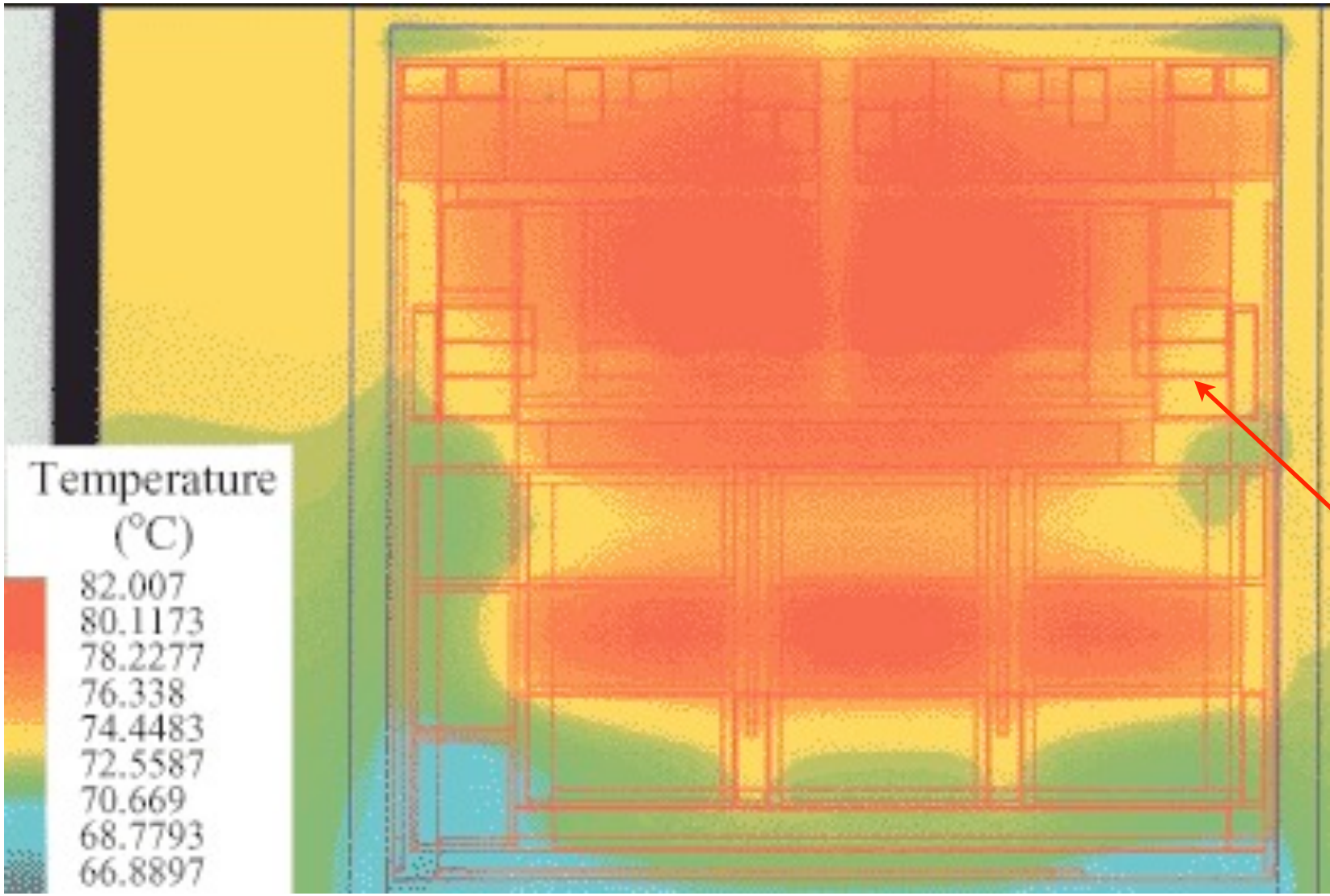
# 115 Watts: Concentrated in "hot spots"




Hot spots

Fixed point units

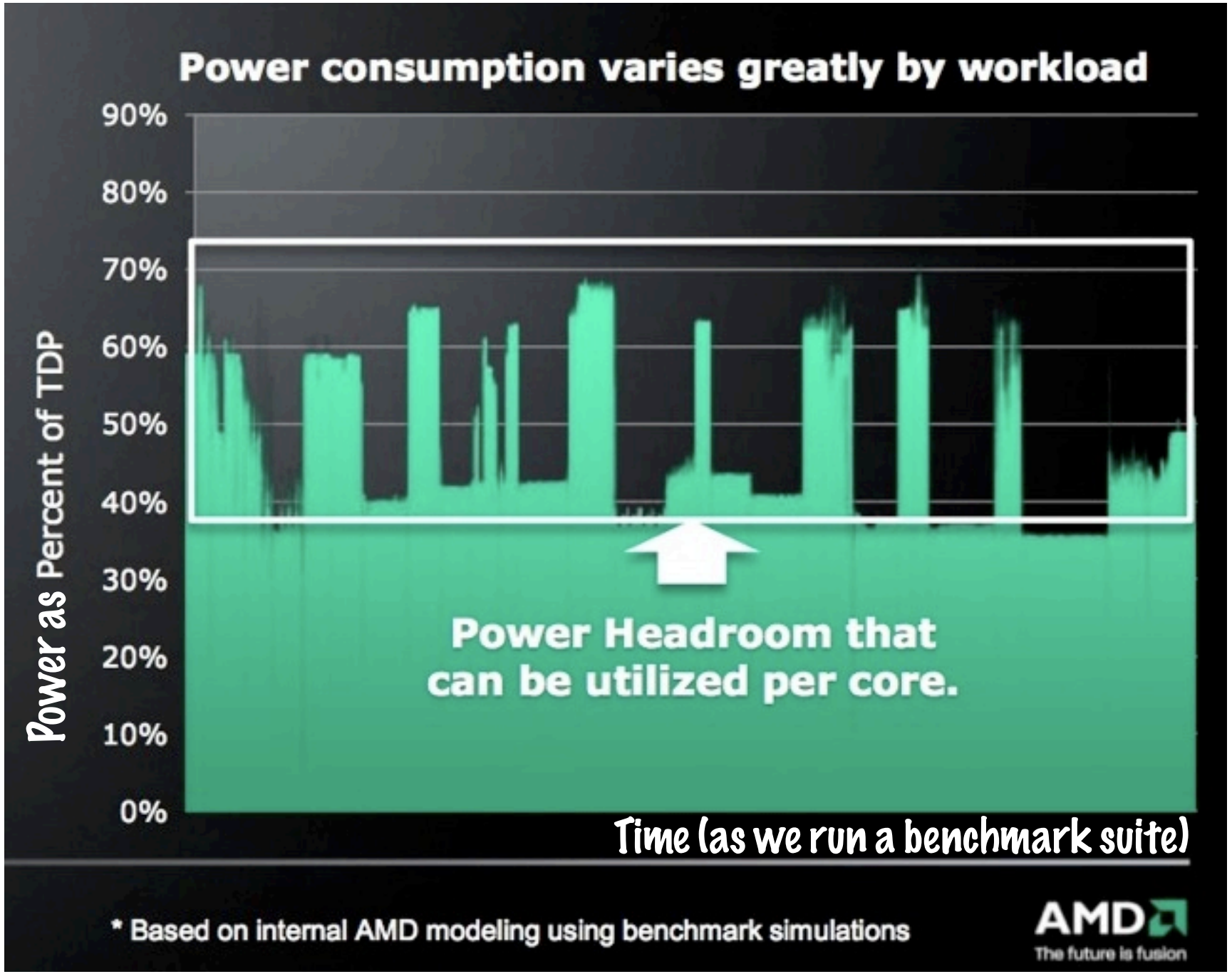
Cache logic

66.8 C == 152 F  82 C == 179.6



UC Regents Spring 2012 © UCB

# Idea: Monitor temperature, servo clock speed




TDP = Thermal Design Point



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# Thursday's lecture: Graphics ...

| | |
|---|---|
| Thu 4/19 | Lec #26: Graphics Processing Chips (Slides) |

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