Technology	Area	Timing
Atmel 0.18 CMOS std-cell	35K gates + RAM	165 MHz (pre-layout)
Atmel 0.25 CMOS std-cell	33K gates + RAM	140 MHz (pre-layout, log file)
UMC 0.25 CMOS std-cell	35K gates + RAM	130 MHz (pre-layout)
Atmel 0.35 CMOS std-cell	2 mm2 + RAM	65 MHz (pre-layout, log file)
Xilinx XC2V3000-6	5,000 LUT + block RAM	80 MHz (post-layout, log1, log2)
Altera 20K200C-7	5,700 LCELLs + EAB RAM	49 MHz (post-layout) log file
Actel AX1000-3	7,600 cells + RAM	48 MHz (post-layout) log file