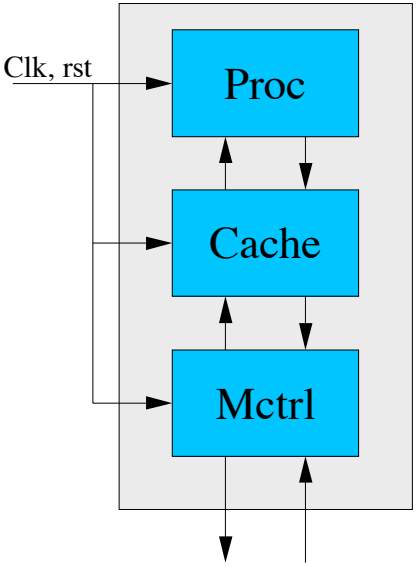
- Grouping of signals makes code readable and shows the direction of the dataflow




```
use work.interface.all;

entity cpu is port (
  clk      : in std_logic;
  rst      : in std_logic;
  mem_in   : in mem_in_type;
  mem_out  : out mem_out_type);
end;

architecture rtl of cpu is
  signal cache_out  : cache_type;
  signal proc_out   : proc_type;
  signal mctrl_out  : mctrl_type;
begin

  u0 : proc port map
    (clk, rst, cache_out, proc_out);

  u1 : cache port map
    (clk, rst, proc_out, mem_out cache_out);

  u2 : mctrl port map
    (clk, rst, cache_out, mem_in, mctrl_out,
     mem_out);

end architecture;
```