# CS 152
# Computer Architecture and Engineering

# Lecture 12 – VLSI II

**2005-2-24**

**John Lazzaro**

**(www.cs.berkeley.edu/~lazzaro)**

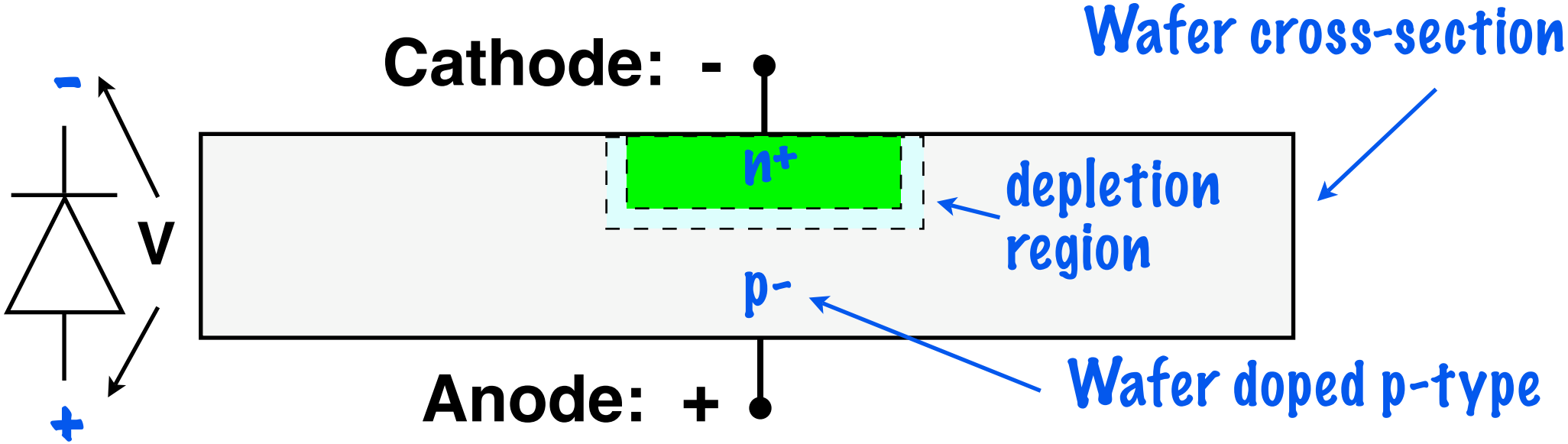
TAs: Ted Hong and David Marquardt

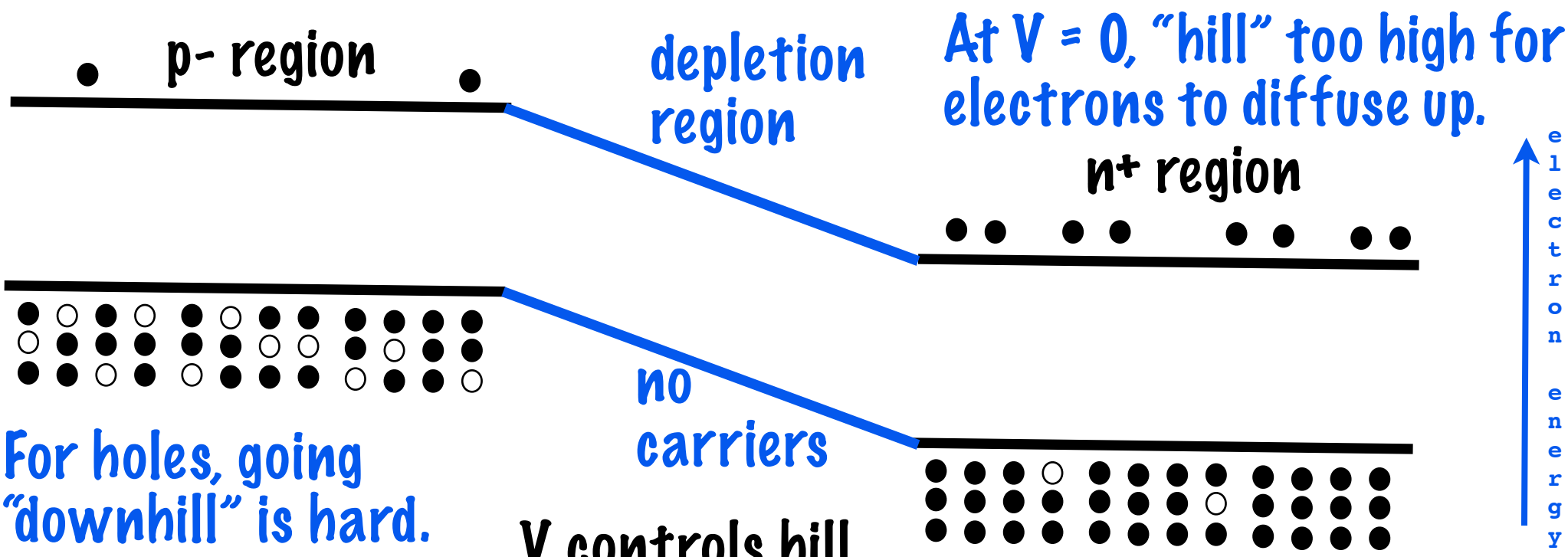
**www-inst.eecs.berkeley.edu/~cs152/**



UC Regents Spring 2005 © UCB

# Last Time: Device Physics Introduction





UC Regents Spring 2005 © UCB

# Today: Memory Core Cells ...

- **Transistor wrap-up:** Fabrication, p-FETs, device model equations.
- **DRAM:** 1 Transistor + 1 Capacitor

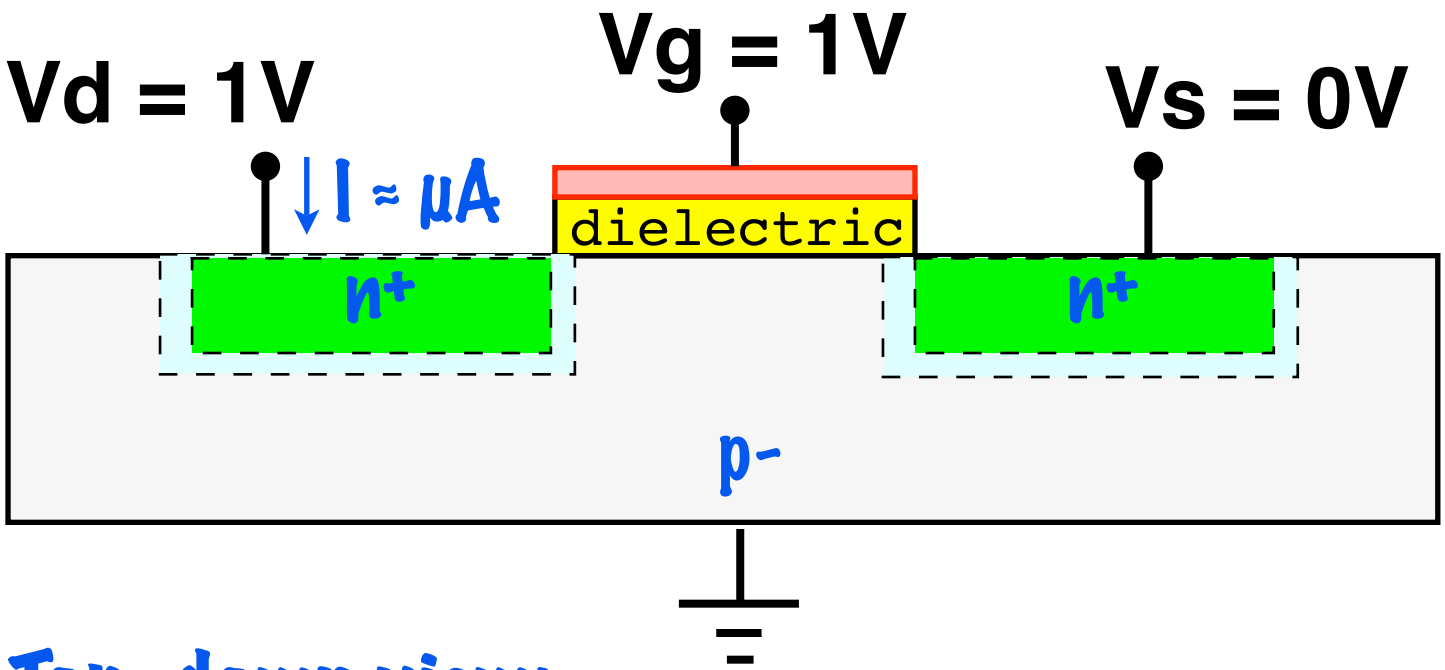

UC Regents Spring 2005 © UCB

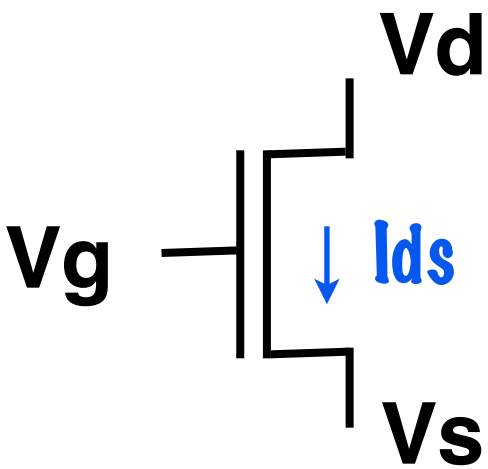
# Fabrication



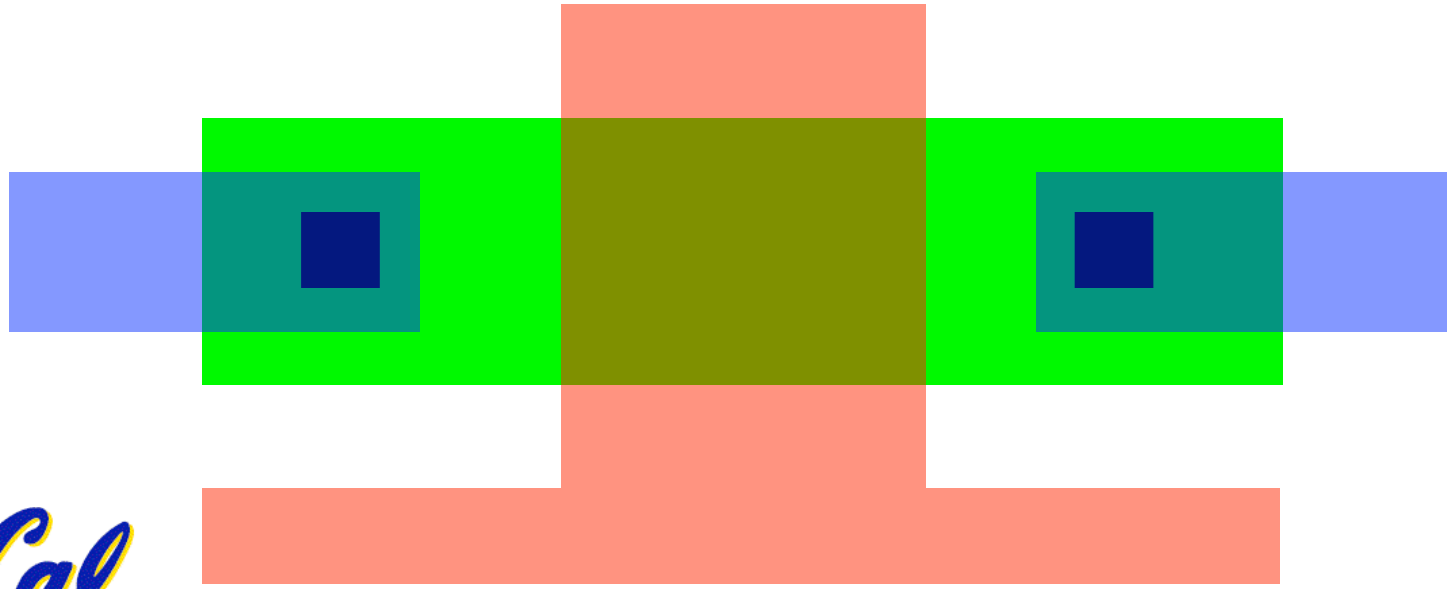
UC Regents Spring 2005 © UCB

# Mask set for an n-Fet ...




Top-down view:



Masks

#1: n+ diffusion

#2: poly (gate)

#3: diff contact

#4: metal

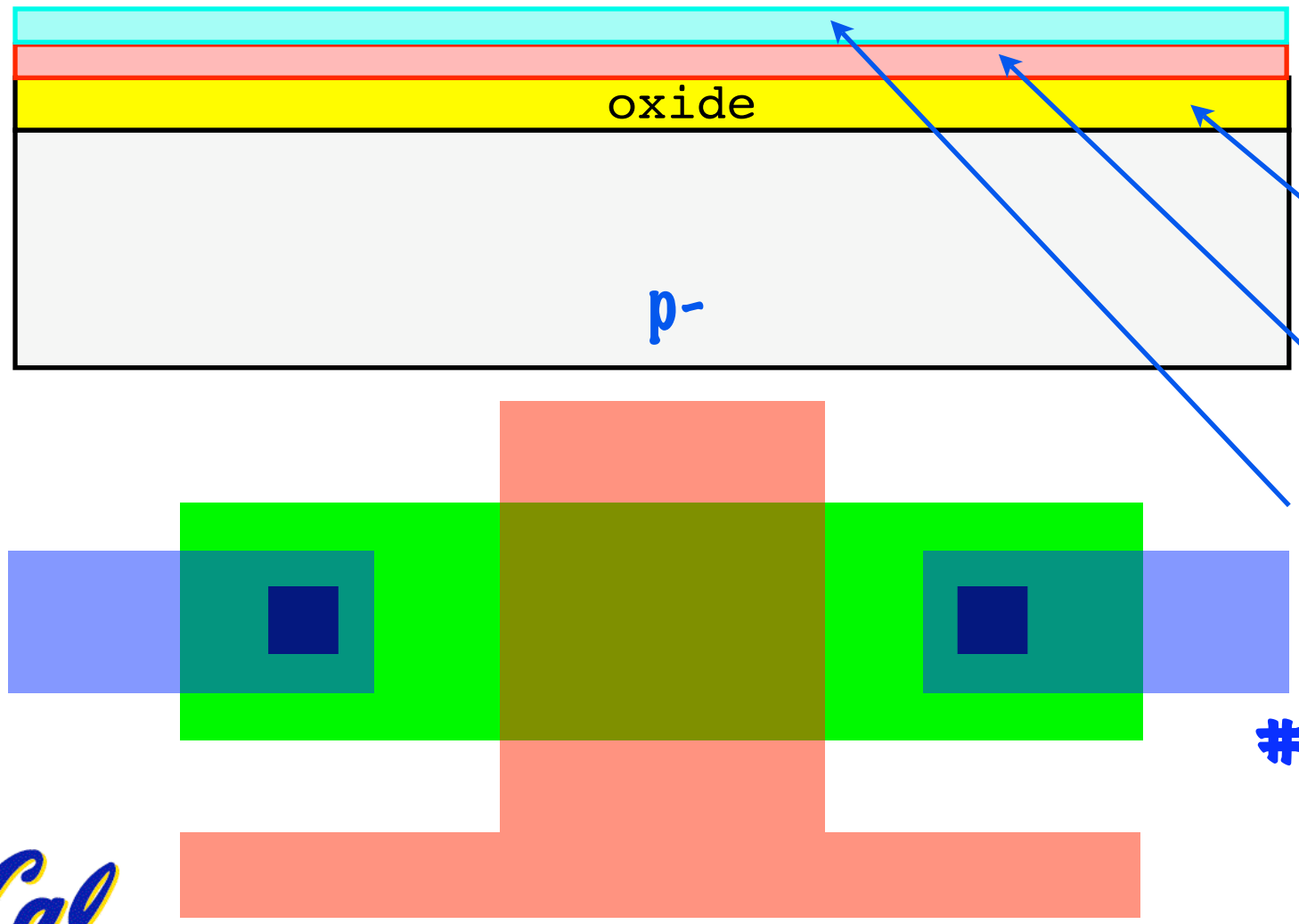
How does a fab use a mask set to make an IC?



UC Regents Spring 2005 © UCB

# Start with an un-doped wafer ...

UV hardens exposed resist. A wafer wash leaves only hard resist.




Steps

#1: dope wafer p-

#2: grow gate oxide

#3: grow undoped polysilicon

#4: spin on photoresist

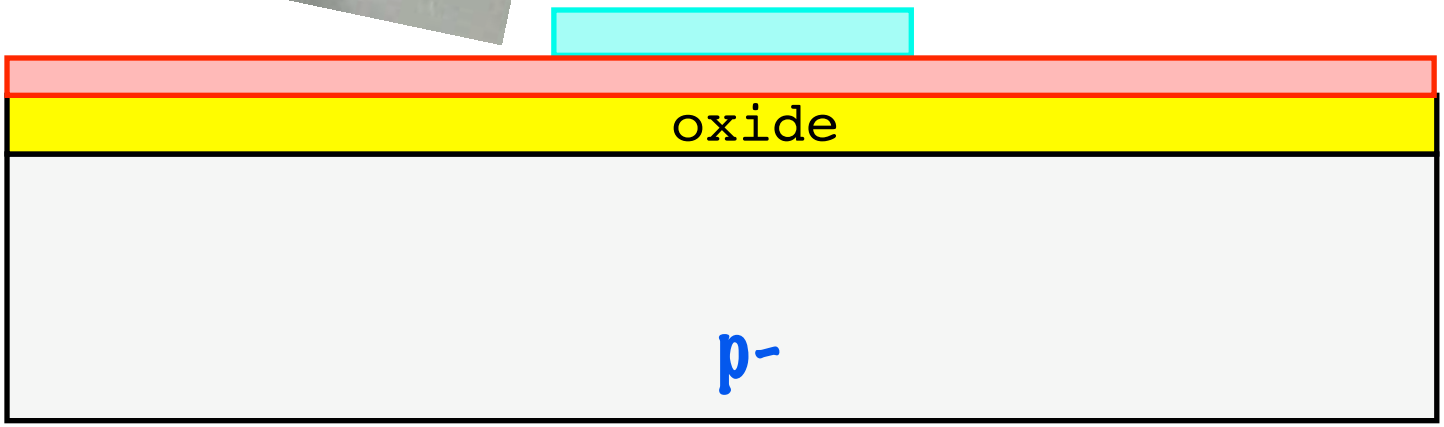
#5: place positive poly mask and expose with UV.

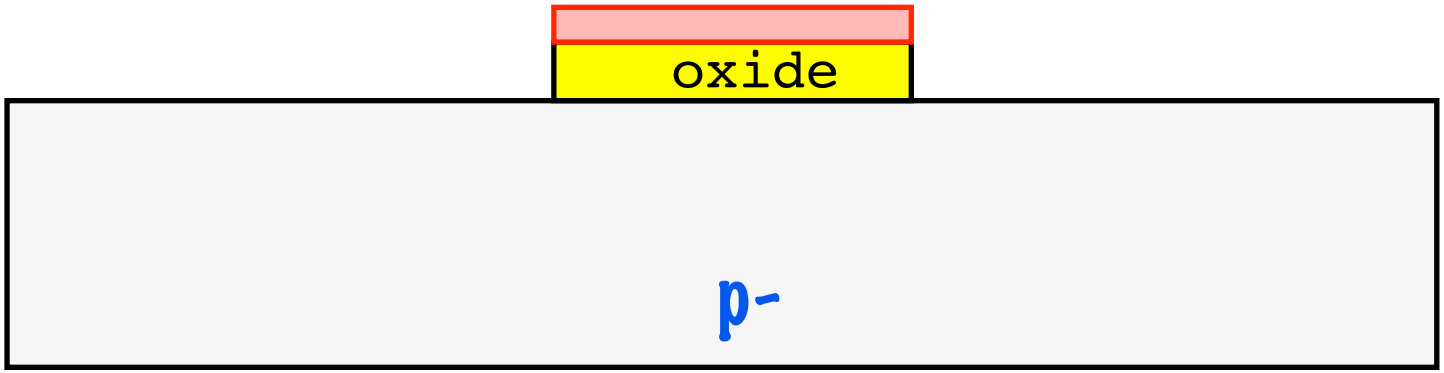


UC Regents Spring 2005 © UCB

# Wet etch to remove unmasked ...

HF acid etches through poly and oxide, but not hardened resist.



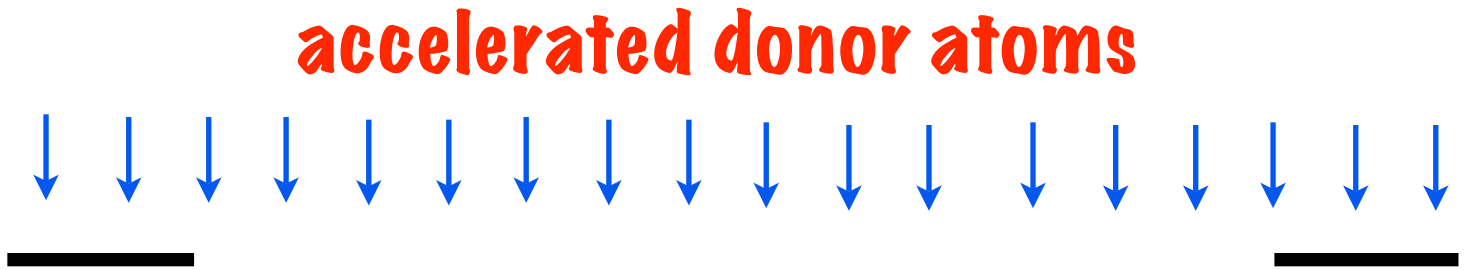



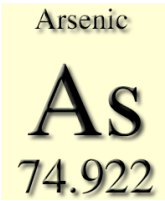

After etch and resist removal

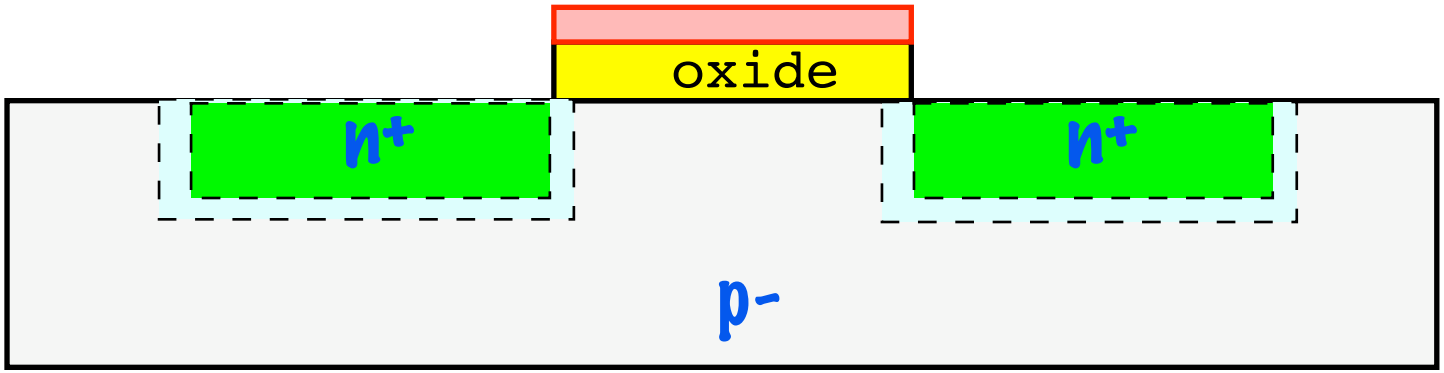


UC Regents Spring 2005 © UCB

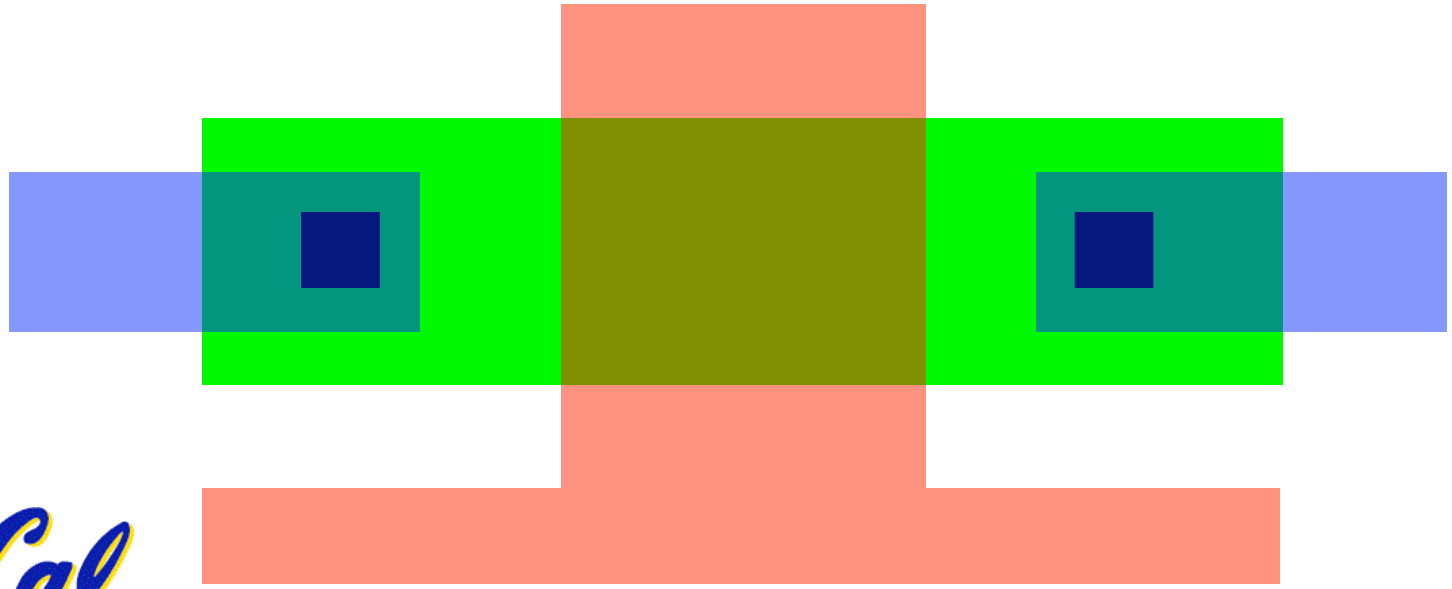
# Use diffusion mask to implant n-type




Notice how donor atoms are blocked by gate and do not enter channel.

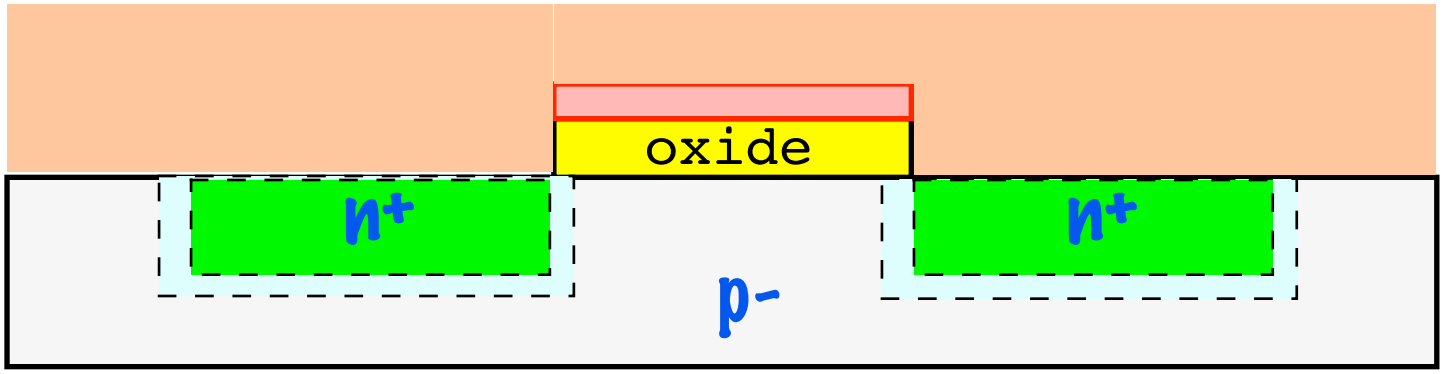


Thus, the channel is "self-aligned", precise mask alignment is not needed!

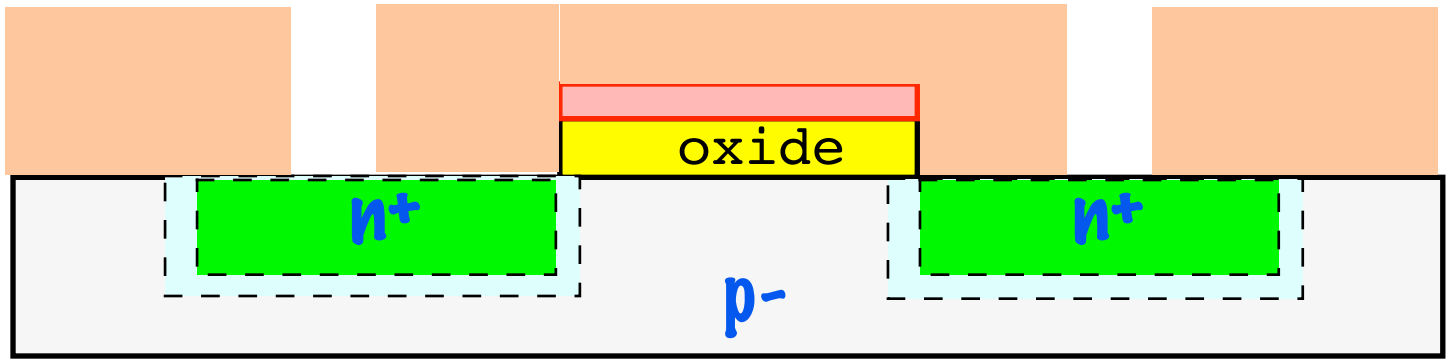


UC Regents Spring 2005 © UCB

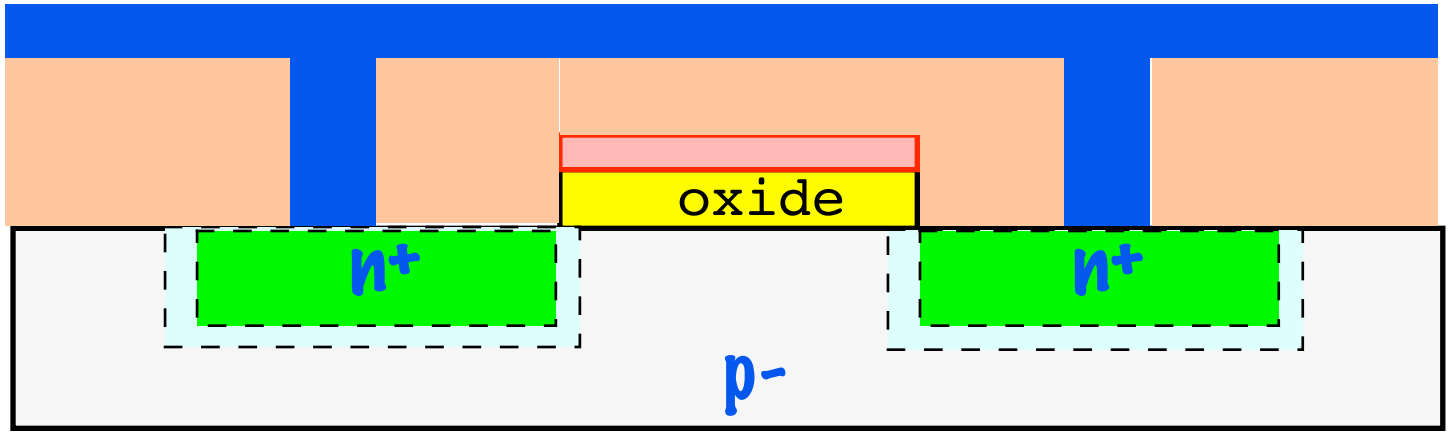
# Metallization completes device




Grow a thick oxide on top of the wafer.




Mask and etch to make contact holes

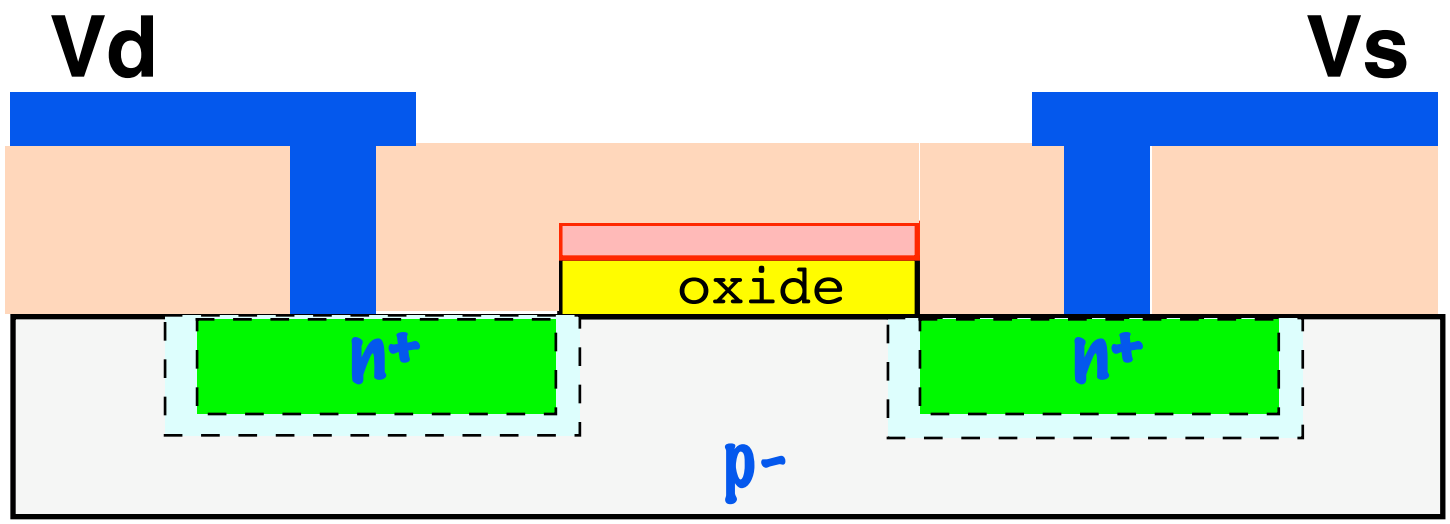



Put a layer of metal on chip. Be sure to fill in the holes!



UC Regents Spring 2005 © UCB

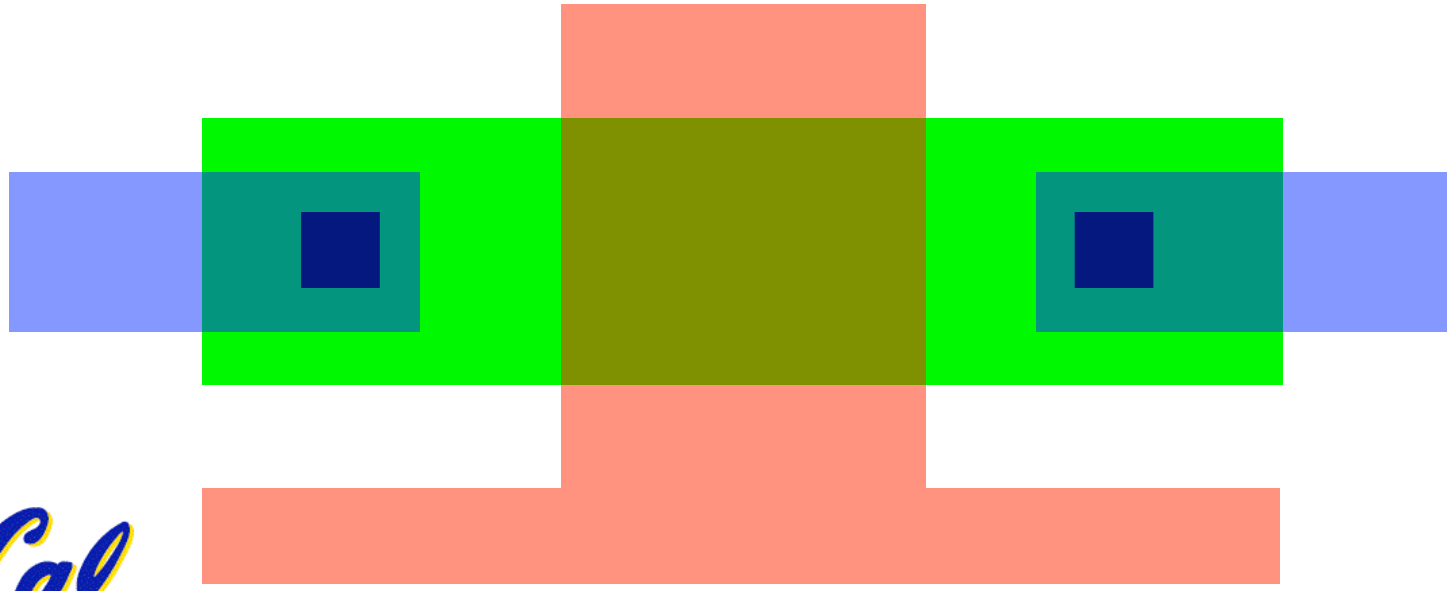
# Final product ...




"The planar process"

Jean Hoerni, Fairchild Semiconductor 1958

Top-down view:





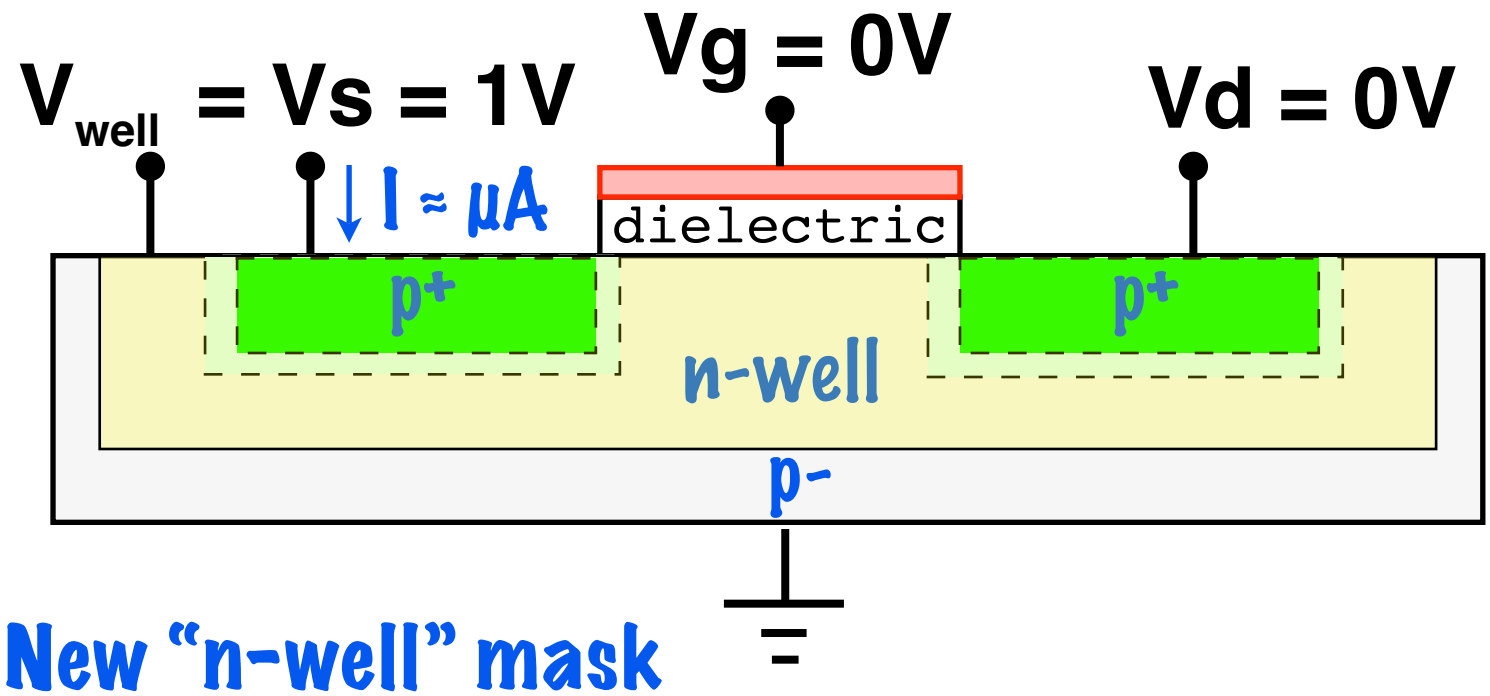
UC Regents Spring 2005 © UCB

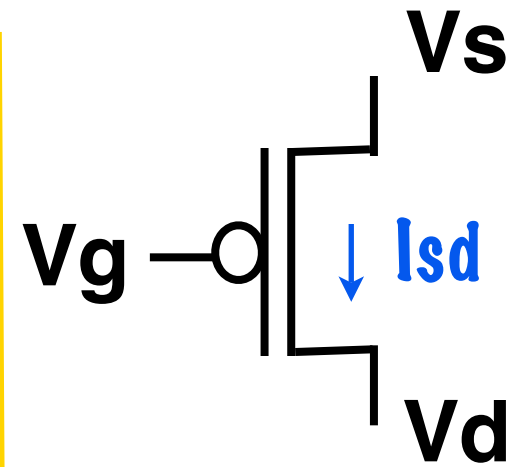
# p-channel Transistors



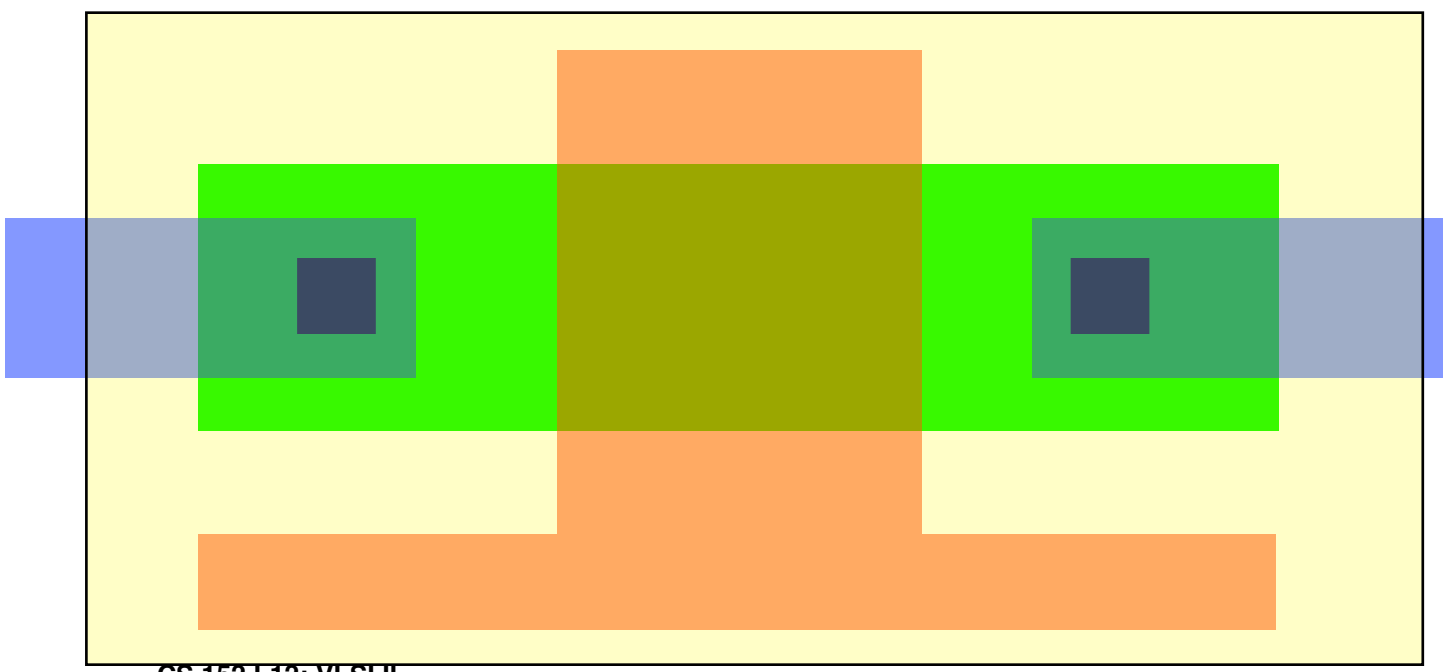
UC Regents Spring 2005 © UCB

# p-Fet: Change polarity of everything




New "n-well" mask



"Mobility" of holes is slower than electrons.

p-Fets drive less current than n-Fets, all else being equal



UC Regents Spring 2005 © UCB

# Device Equations

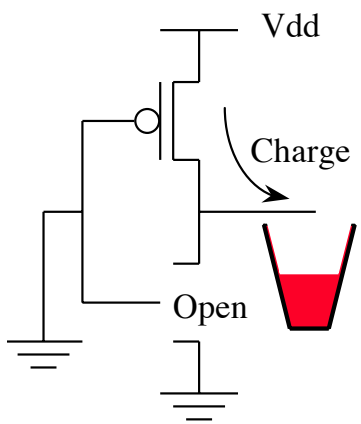


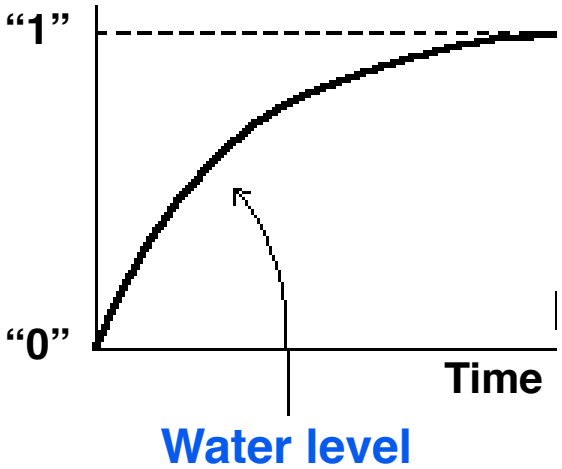
UC Regents Spring 2005 © UCB

# Recall: Our old "switch" model ...

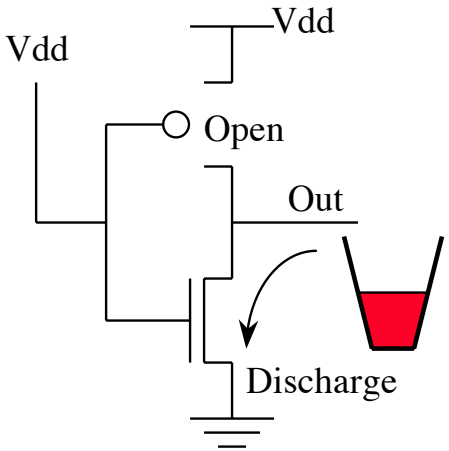
## We begin by modeling transistors that are "off"

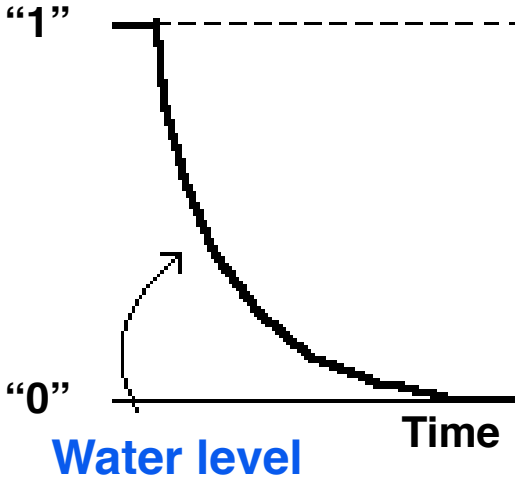
A "on" p-FET fills up the capacitor with charge.




A "on" n-FET empties the bucket.

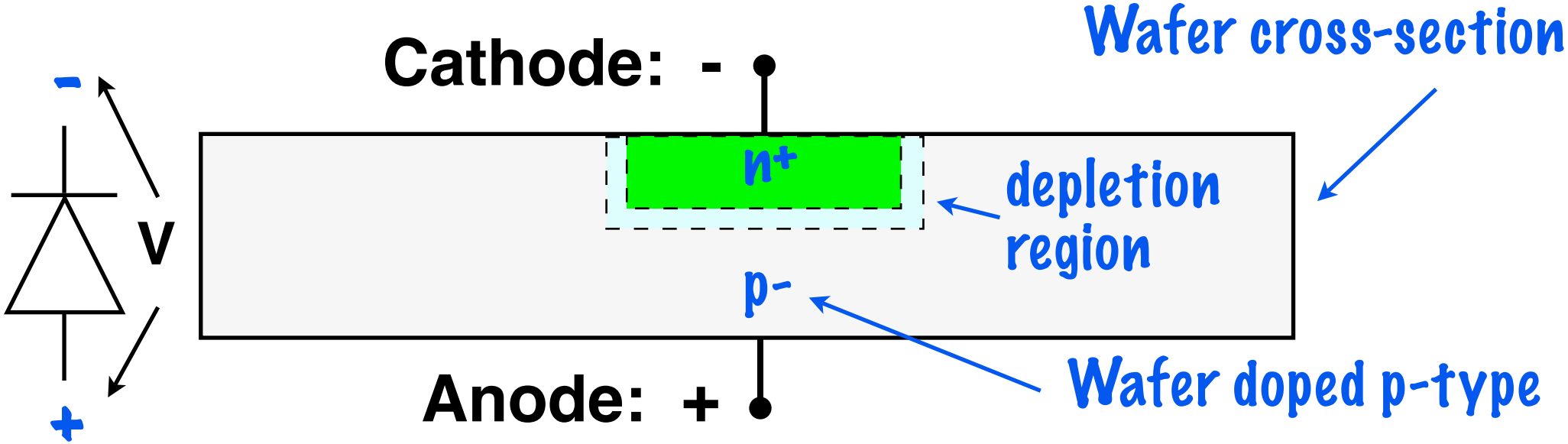


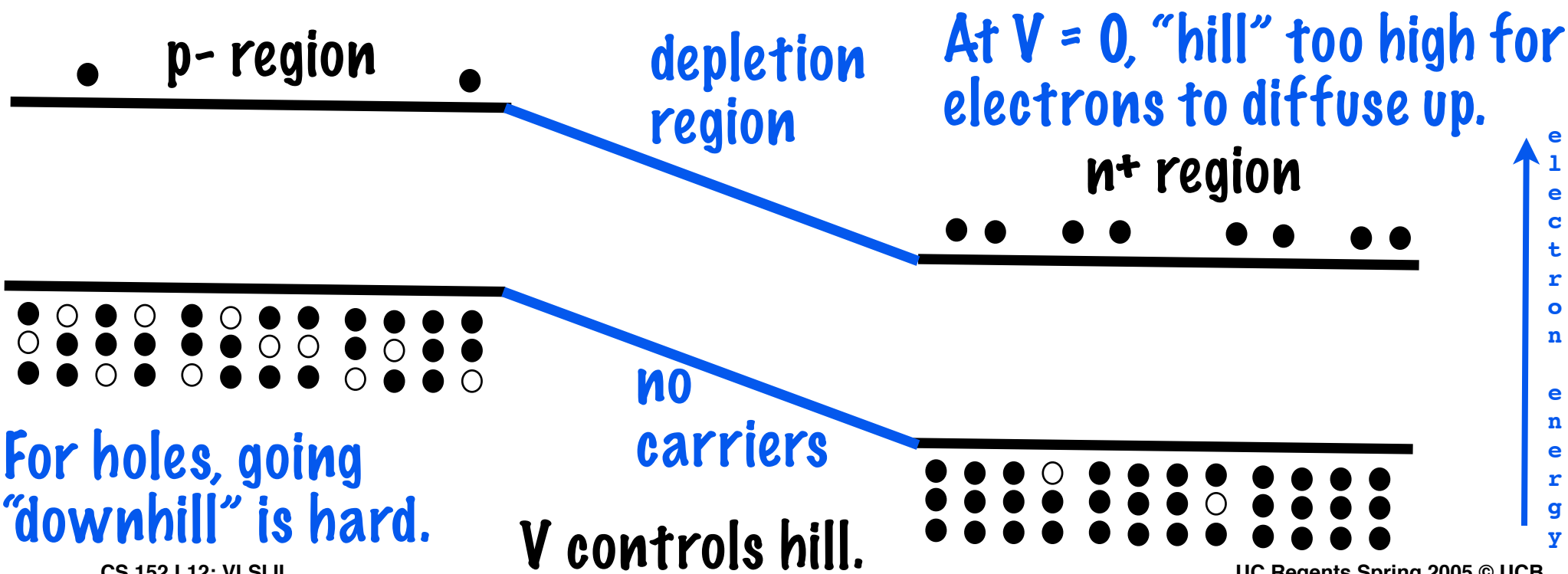






UC Regents Spring 2005 © UCB

# Recall: Why diode current is I = exp(V) ...

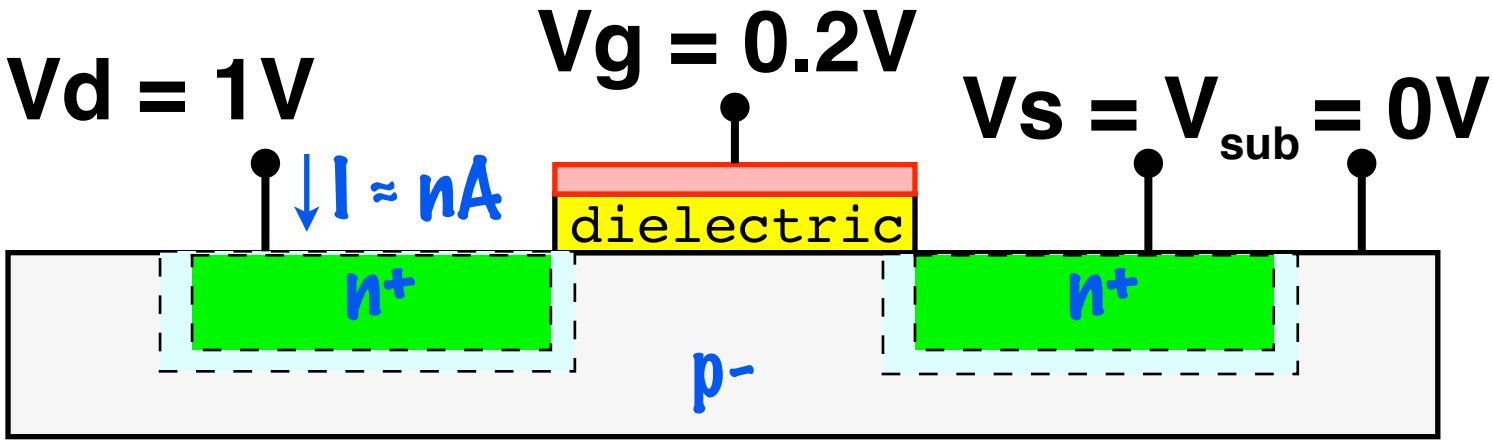


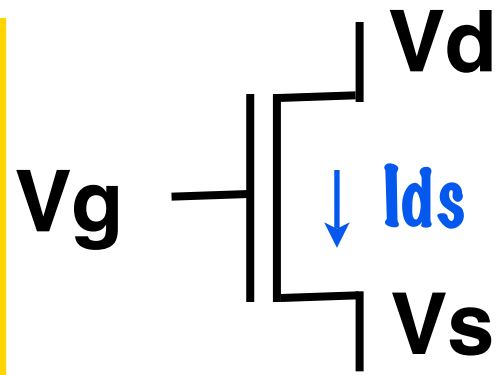





UC Regents Spring 2005 © UCB

# A simple model for "off" transistor ...

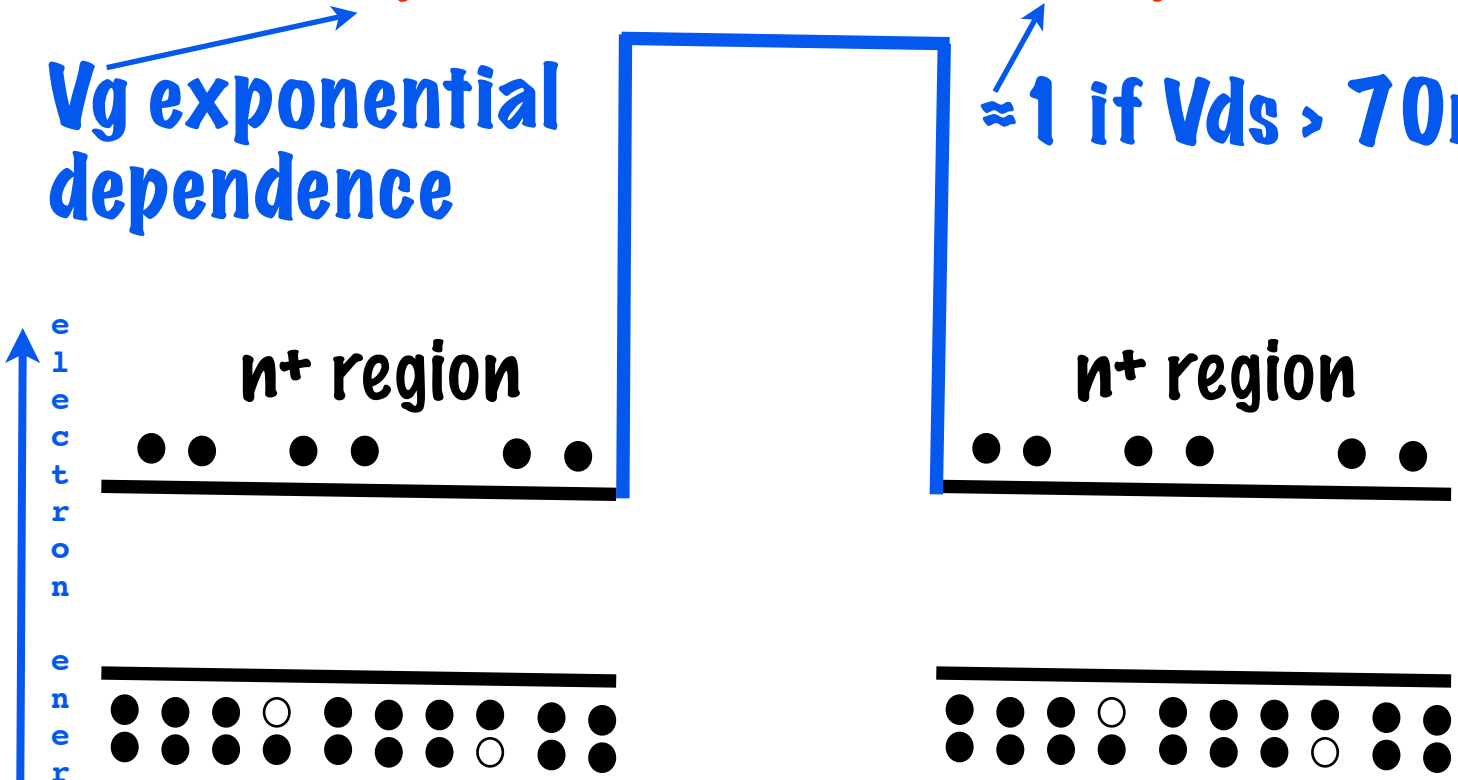



$$I_{ds} = I_o\,[\exp((\kappa V_g - V_s)/V_o)]\;[1 - \exp(-V_{ds}/V_o)]$$

Vg exponential dependence

≈1 if Vds > 70mV




Current flows when electrons diffuse to the "gate wall" top

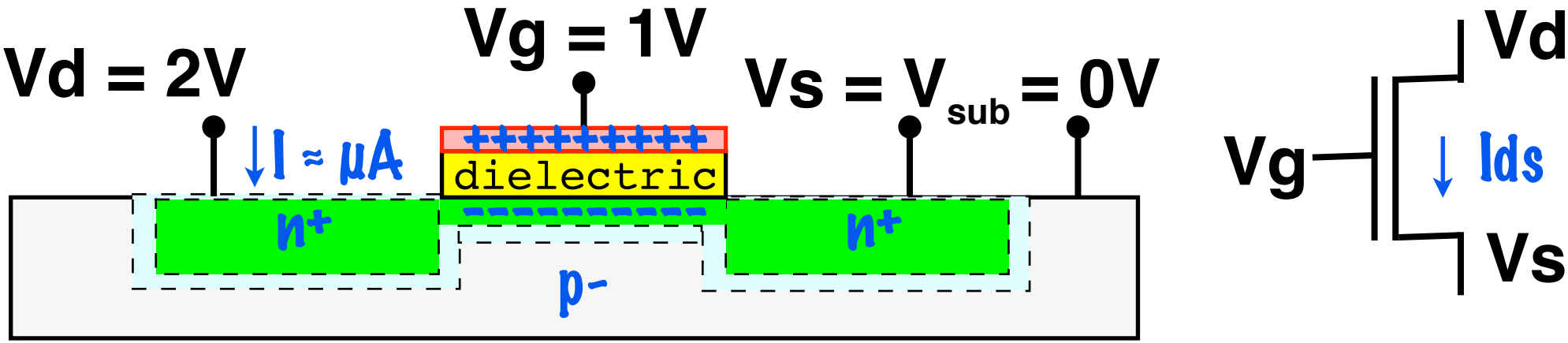
# electrons that reach top goes up as wall comes down, implies Ids ~ exp(Vg)

$I_o$ ~100fA, $V_o = kT/q = 25mV$, $\kappa = 0.7$



UC Regents Spring 2005 © UCB

# A simple model for "on" transistor ...




Ids = (carriers in channel) / (transit time)

Q = CV

f(length, velocity)

$$I_{ds} = [(\mu \epsilon W)/(LD)]\ [V_{gs} - V_{th}]\ [V_{ds}]$$

If Vds > Vgs - Vth, channel physics change :

$$I_{ds} = [(\mu \epsilon W)/(2LD)]\ [V_{gs} - V_{th}]^2$$

W = transistor width, L = length,
D = capacitor plate distance
μ is velocity, ∈ is C dilectric constant


UC Regents Spring 2005 © UCB

# Admin: Testing and Interfaces on Friday

| | | | | |
|---|---|---|---|---|
| F 2/25 | | | | Lab 3: Final Design Document Review (Interfaces and Test Benches), 12-2PM, 119 Cory |

1. **Detailed specifications** of the processor: timing diagrams and pinouts for every module, signal names and timing diagrams for every global wire in the datapath and the controller, and a few schematics to communicate the design to your TAs (datapath schematic, etc). These specifications should be sufficiently detailed that the TAs would be able to design one of your modules from the specification, and the Verilog would work when you added it to your design.
2. **Completed test benches**. For each module, you will show a **unit test bench**, written in Verilog, with a complete set of test vectors. To show the test benches work, you should prepare a "dummy" module of the device under test, that also knows the test input vectors, and will respond with either the correct output vector or an incorrect output vector (so that we can see during section that your test bench code works). In addition to unit tests, you should have a set of **multi-unit test benches**, written in Verilog and ready to demo, to ensure that the specifications for each module are consistent. Finally, you should prepare and a machine language code suite for **full processor testing** that tests the edge cases of a pipelined design, and be prepared to show programs from the suite working in SPIM to your TAs.

**Homework 1: due Friday 3/4**

**Midterm 1: Thurs 3/17, 6PM to 9PM**



UC Regents Spring 2005 © UCB

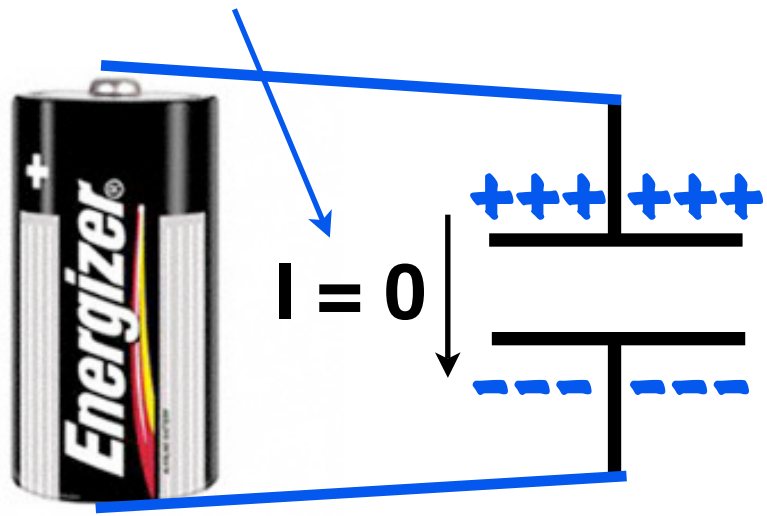
# Dynamic Memory (DRAM)



UC Regents Spring 2005 © UCB

# Recall: Capacitors in action

Because the dielectric is an insulator, and does not conduct.




After circuit "settles" ...

Q = C V = C * 1.5 Volts (D cell)

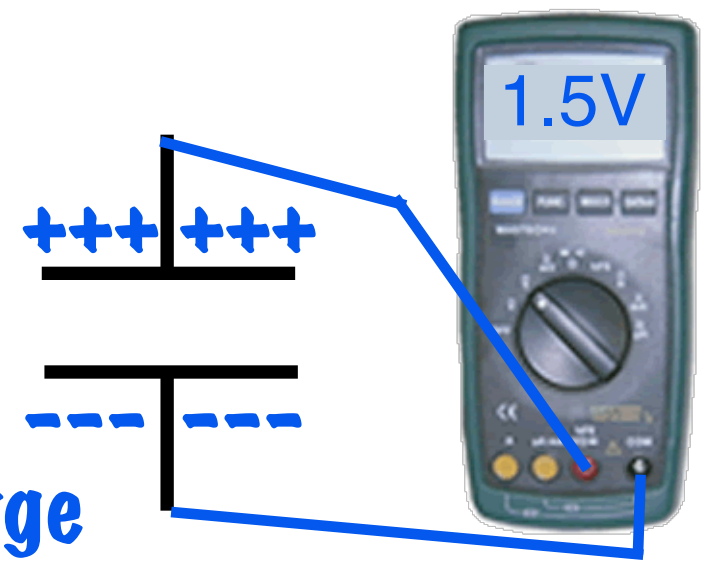
Q: Charge stored on capacitor

C: The capacitance of the device: function of device shape and type of dielectric.

After battery is removed:

Still, Q = C * 1.5 Volts

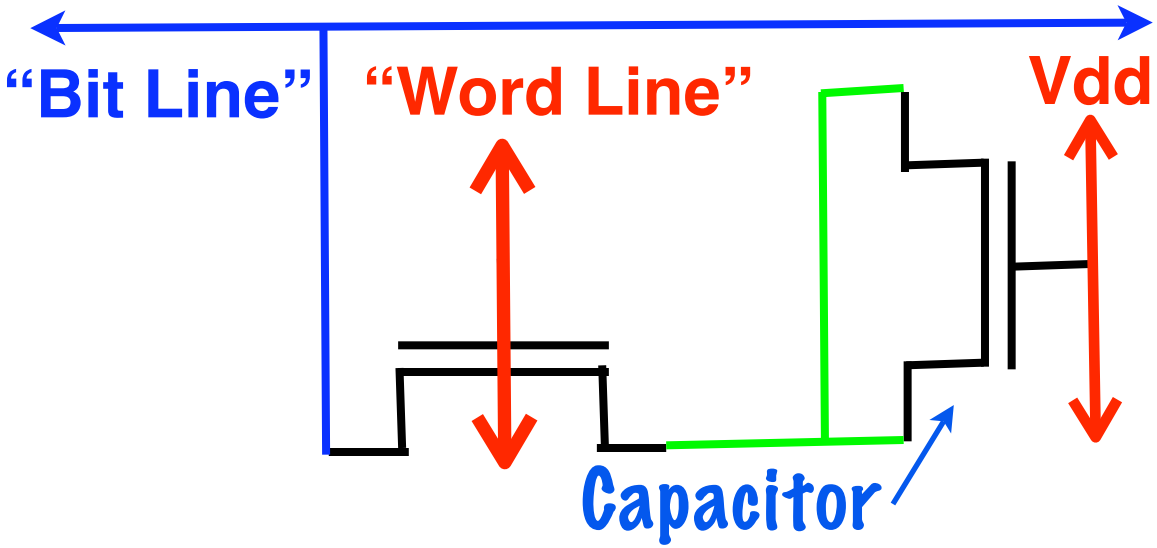
Capacitor "remembers" charge

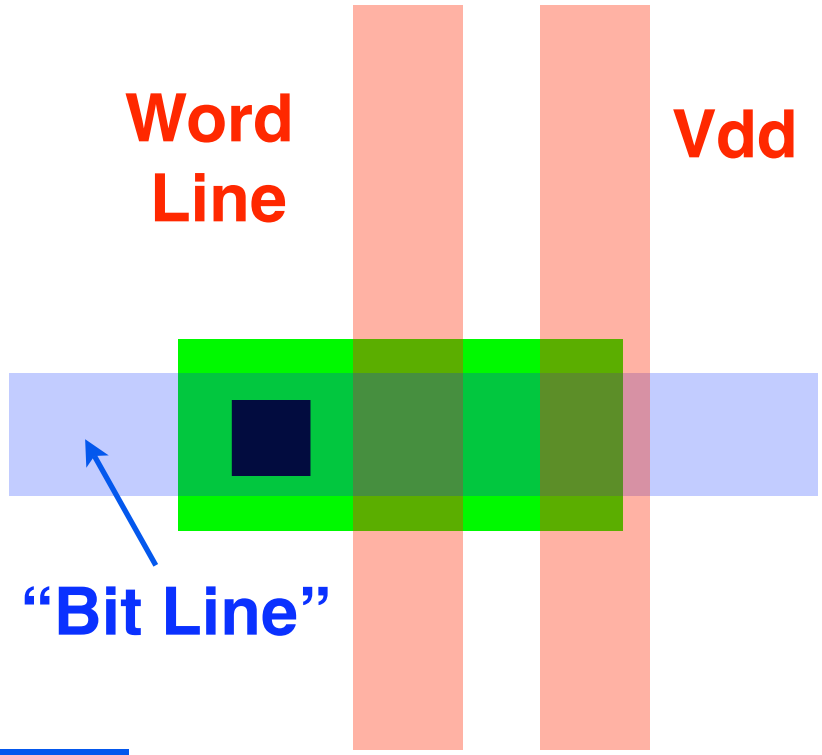


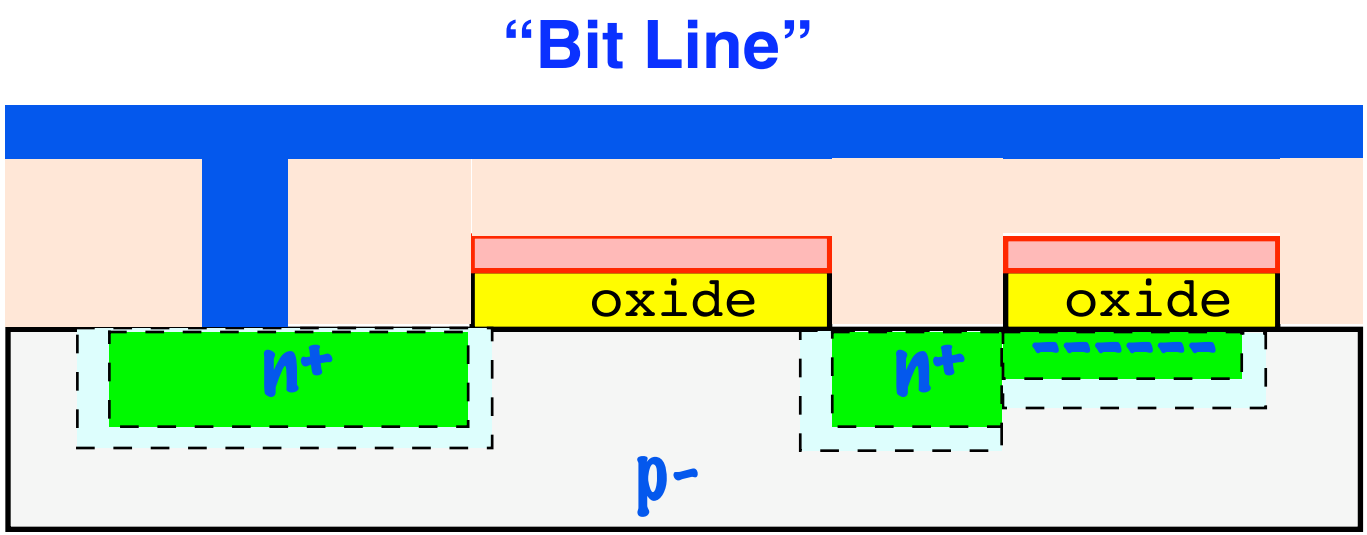



UC Regents Spring 2005 © UCB

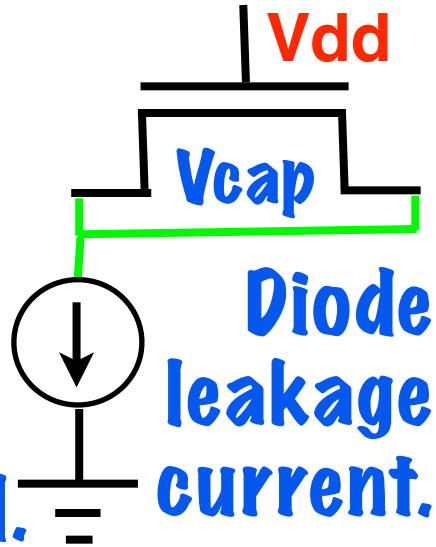
# DRAM cell: 1 transistor, 1 capacitor




Why Vcap values start out at ground.



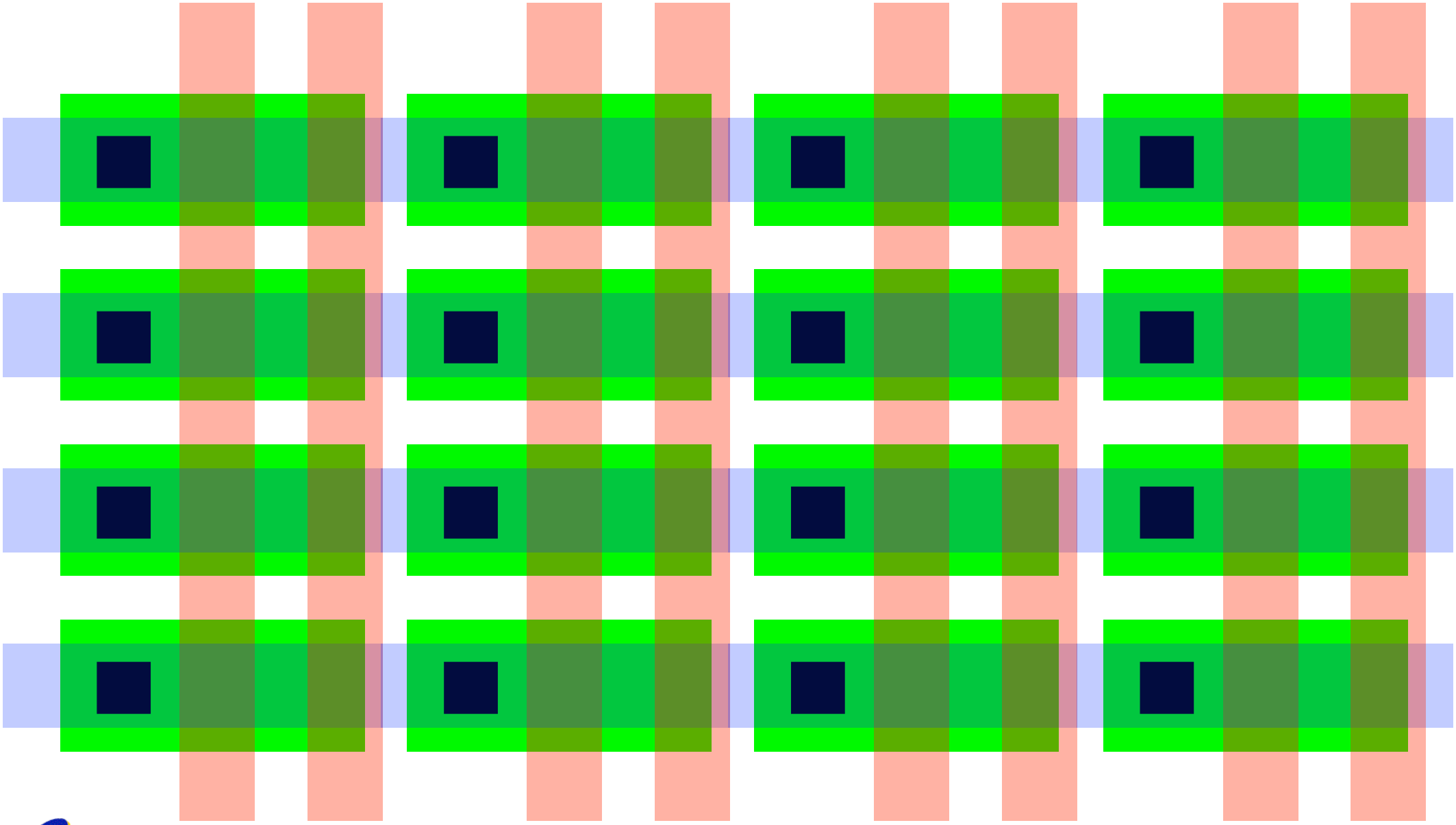

Diode leakage current.

Word Line and Vdd run on "z-axis"



UC Regents Spring 2005 © UCB

# A 4 x 4 DRAM array (16 bits) ....



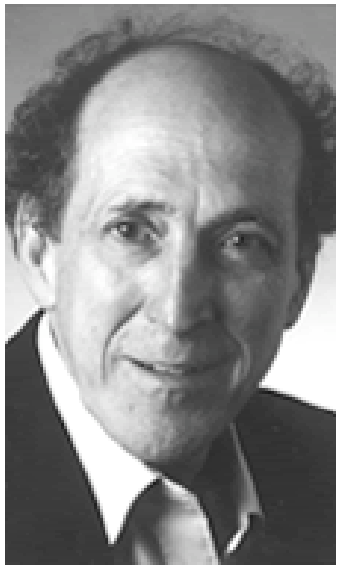


UC Regents Spring 2005 © UCB

# Invented after SRAM, by Robert Dennard

## United States Patent Office

3,387,286
Patented June 4, 1968



1

3,387,286
FIELD-EFFECT TRANSISTOR MEMORY
Robert H. Dennard, Croton-on-Hudson, N.Y., assignor to International Business Machines Corporation, Armonk, N.Y., a corporation of New York
Filed July 14, 1967, Ser. No. 653,415
21 Claims. (Cl. 340—173)

2

tinent in disclosing various concepts and structures which have been developed in the application of field-effect transistors to different types of memory applications, the primary thrust up to this time in conventional read-write random access memories has been to connect a plurality of field-effect transistors in each cell in a latch configuration. Memories of this type require a large number of active devices in each cell and therefore each cell re-

FIG. 1

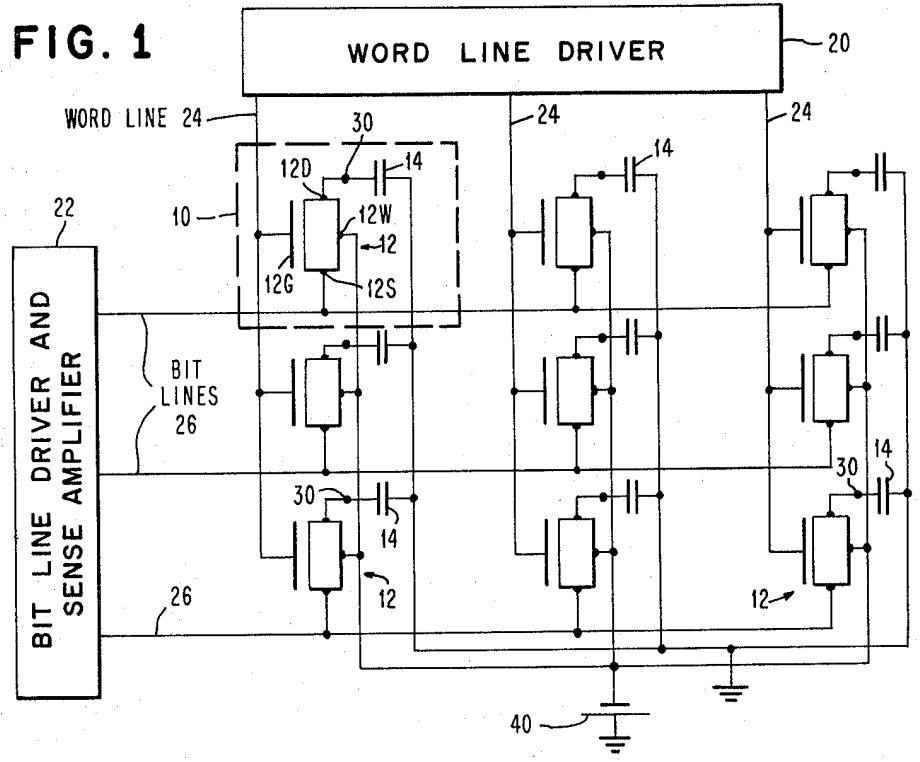
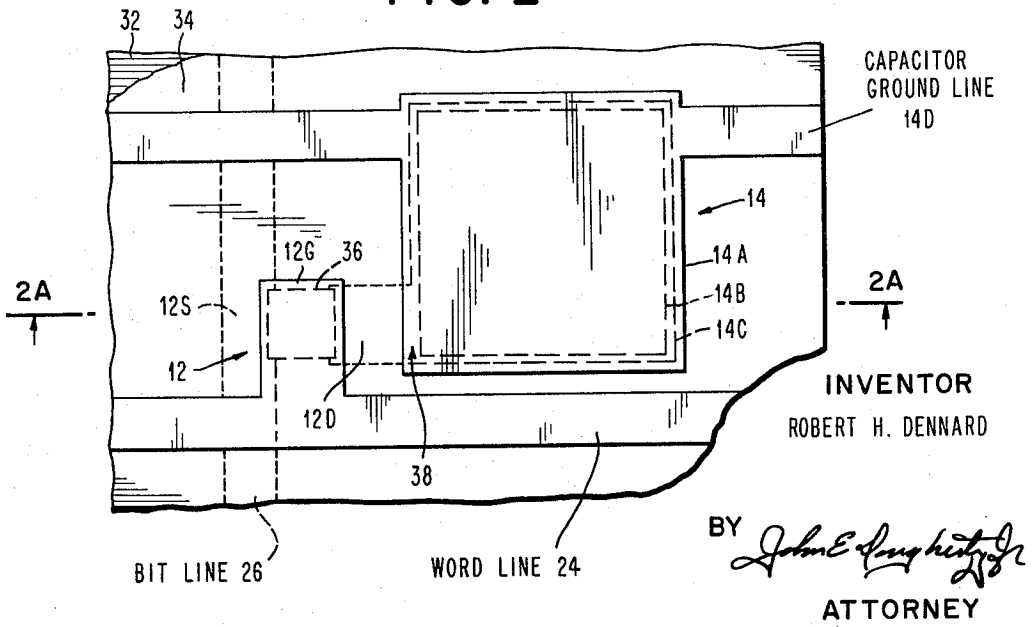


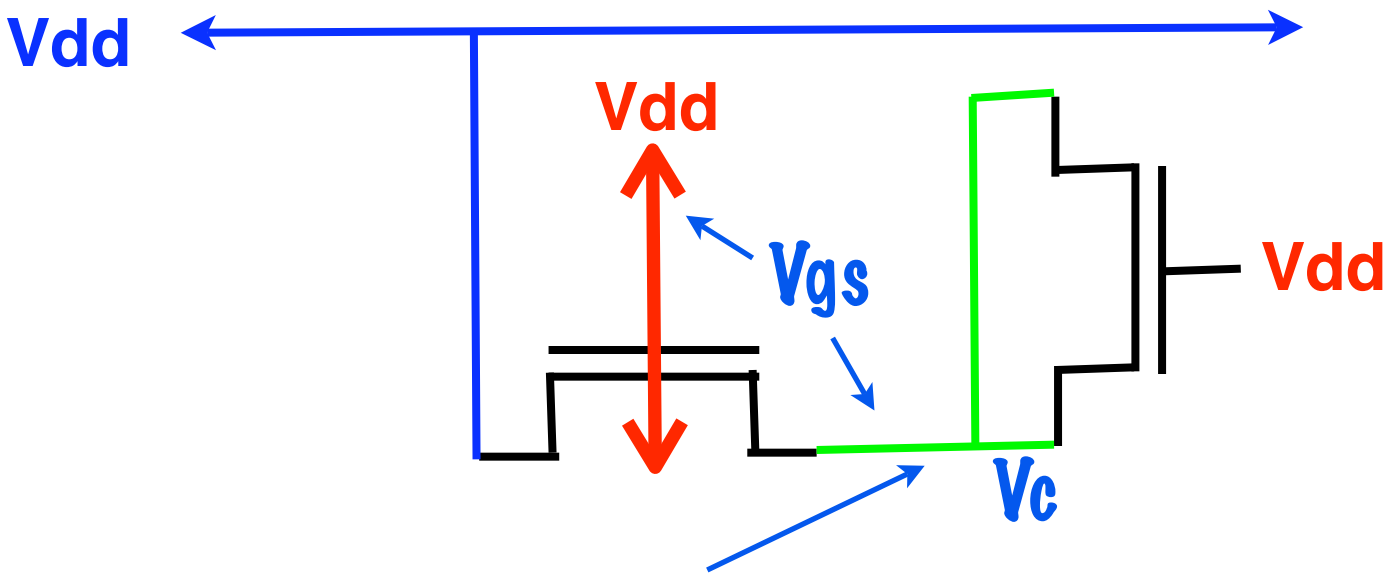

FIG. 2






UC Regents Spring 2005 © UCB

# DRAM Circuit Challenge #1: Writing




Vdd - Vth. Bad, we store less charge. Why do we not get Vdd?

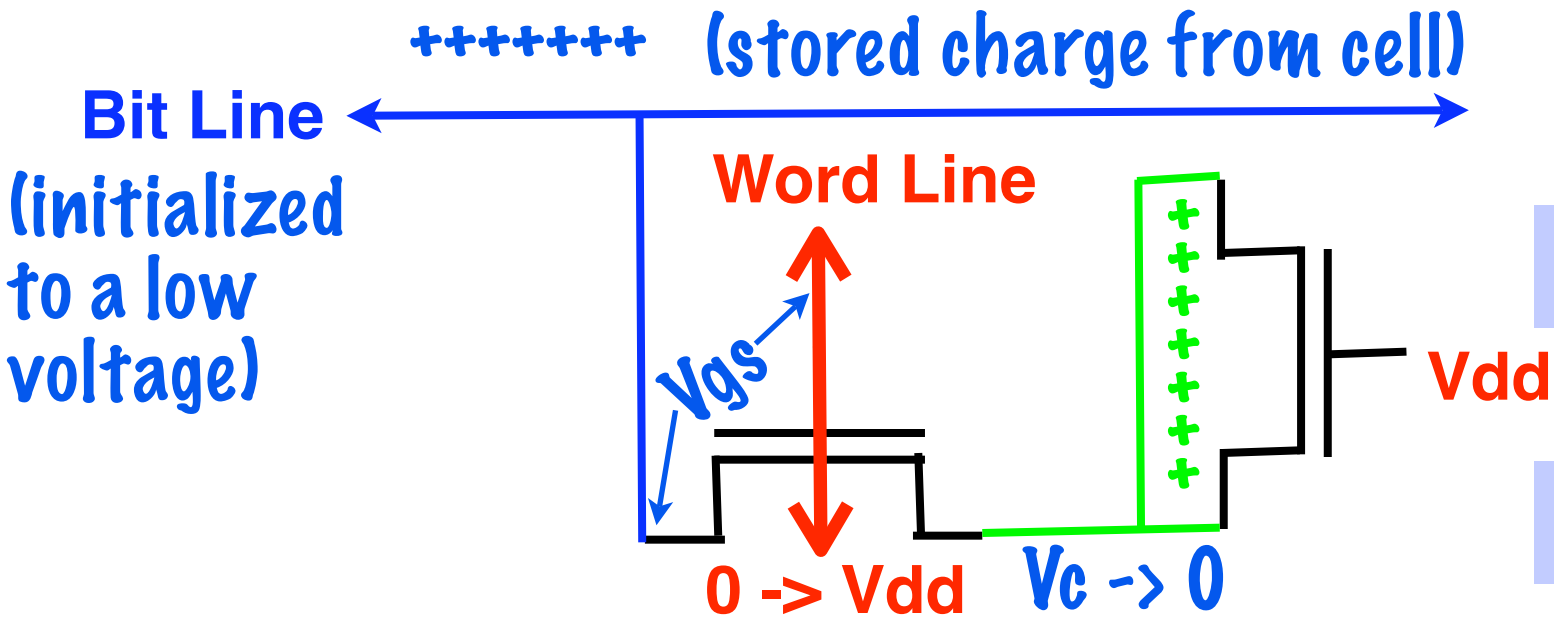
Ids = [(μεW)/(2LD)] [Vgs -Vth]^2 , but "turns off" when Vgs <= Vth!

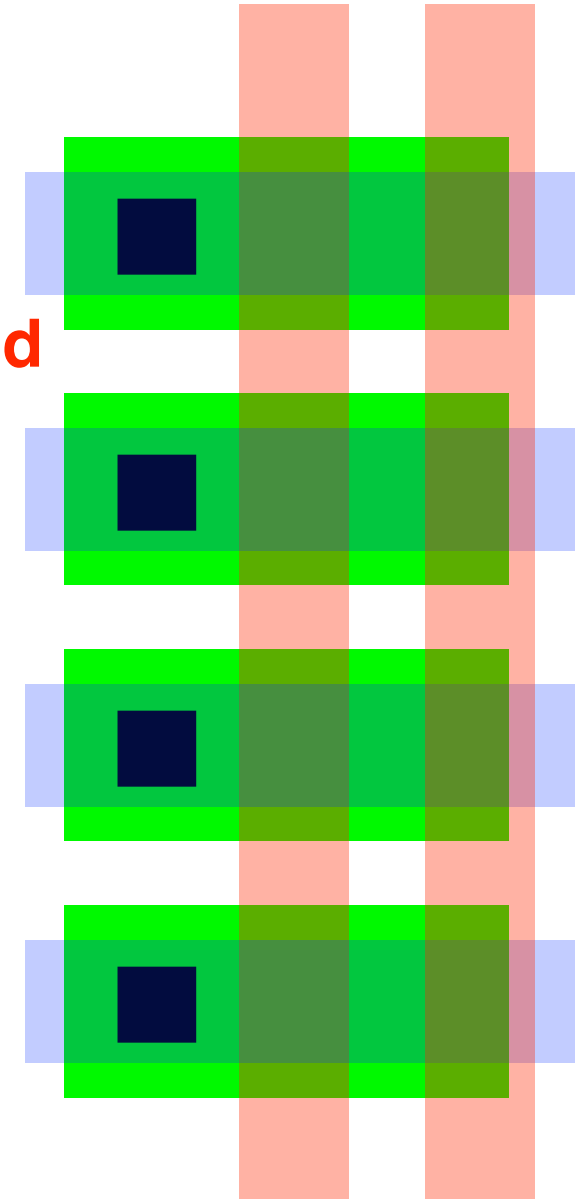
Vgs = Vdd - Vc. When Vdd - Vc == Vth, charging effectively stops!



UC Regents Spring 2005 © UCB

# DRAM Challenge #2: Destructive Reads



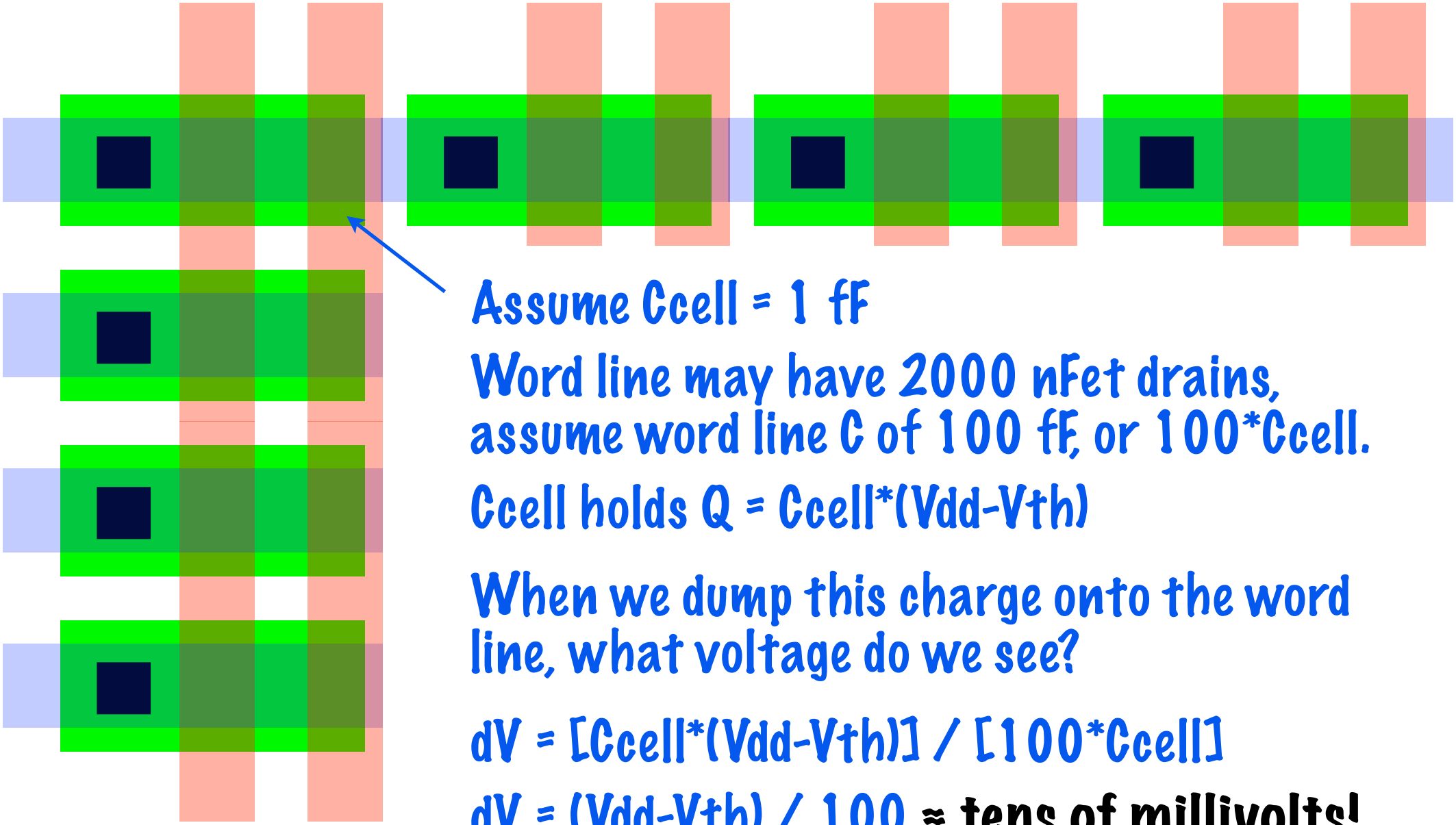
Raising the word line removes the charge from every cell it connects too!

Must write back after each read.



UC Regents Spring 2005 © UCB

# DRAM Circuit Challenge #3a: Sensing



Assume Ccell = 1 fF

Word line may have 2000 nFet drains, assume word line C of 100 fF, or 100*Ccell.

Ccell holds Q = Ccell*(Vdd-Vth)

When we dump this charge onto the word line, what voltage do we see?

dV = [Ccell*(Vdd-Vth)] / [100*Ccell]

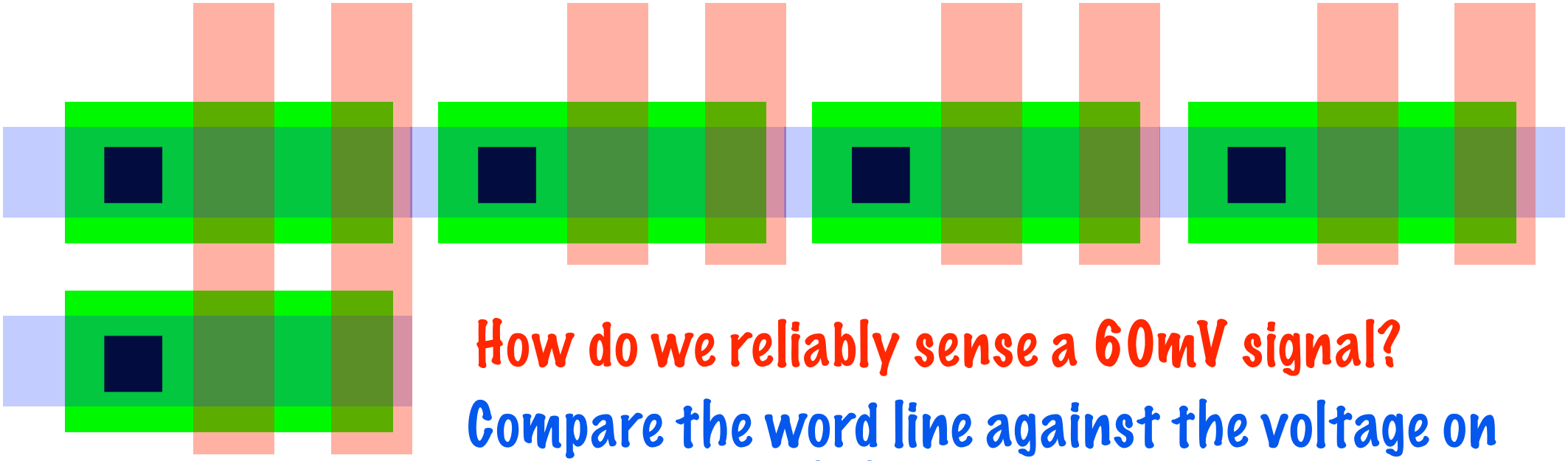
dV = (Vdd-Vth) / 100 ≈ **tens of millivolts!**

In practice, scale array to get a 60mV signal.



UC Regents Spring 2005 © UCB

# DRAM Circuit Challenge #3b: Sensing



How do we reliably sense a 60mV signal?

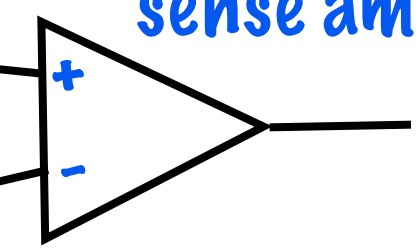
Compare the word line against the voltage on a "dummy" world line.

[...]

"sense amp"

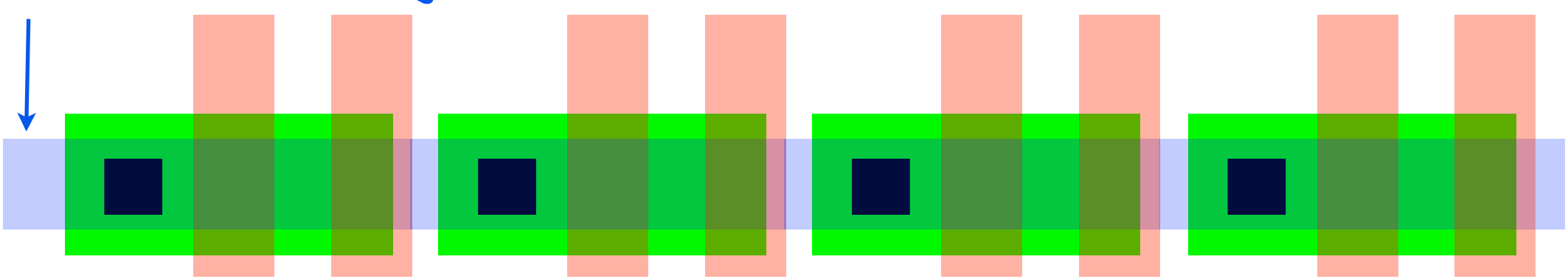
Word line to sense

Dummy word line




?

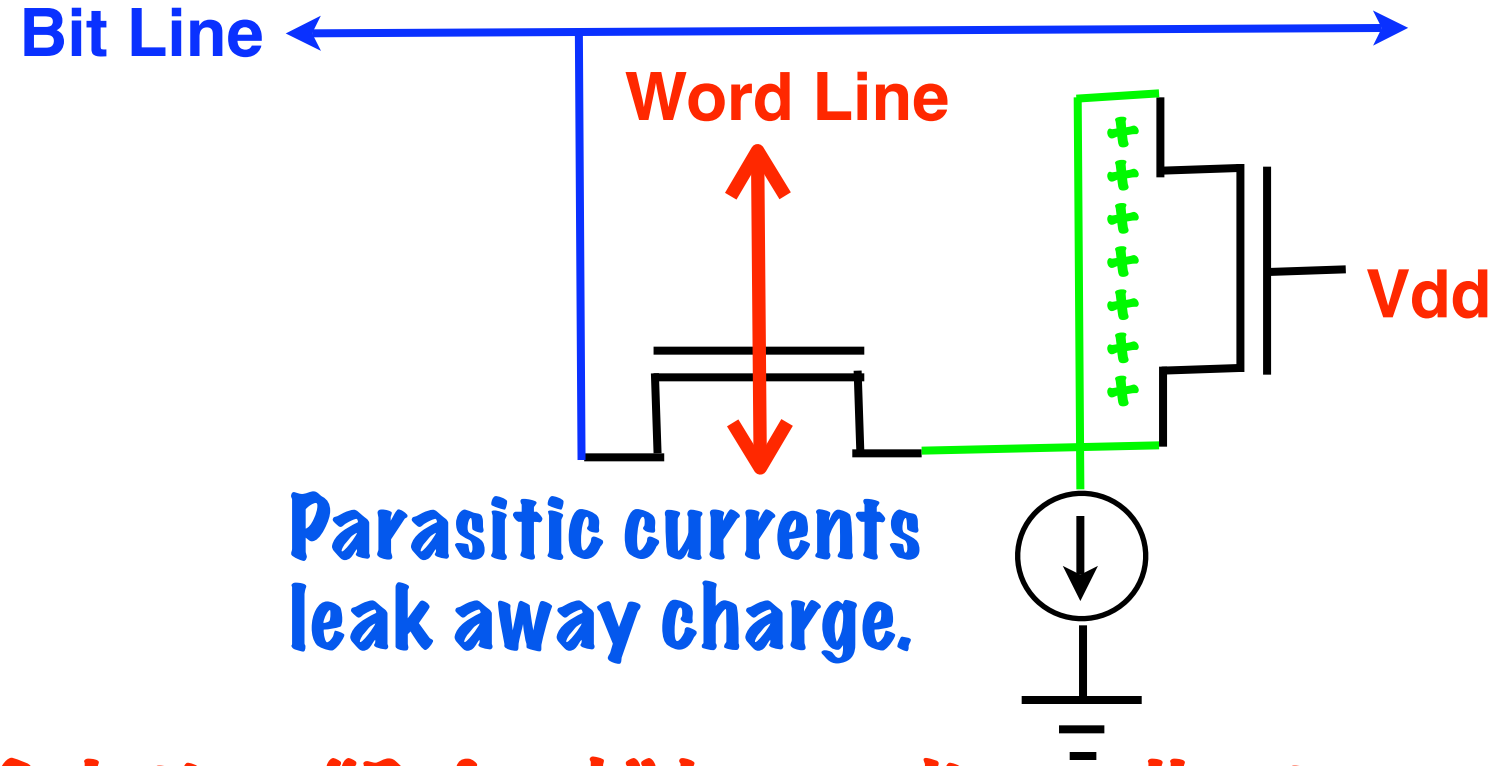
"Dummy" word line.
Cells hold no charge.



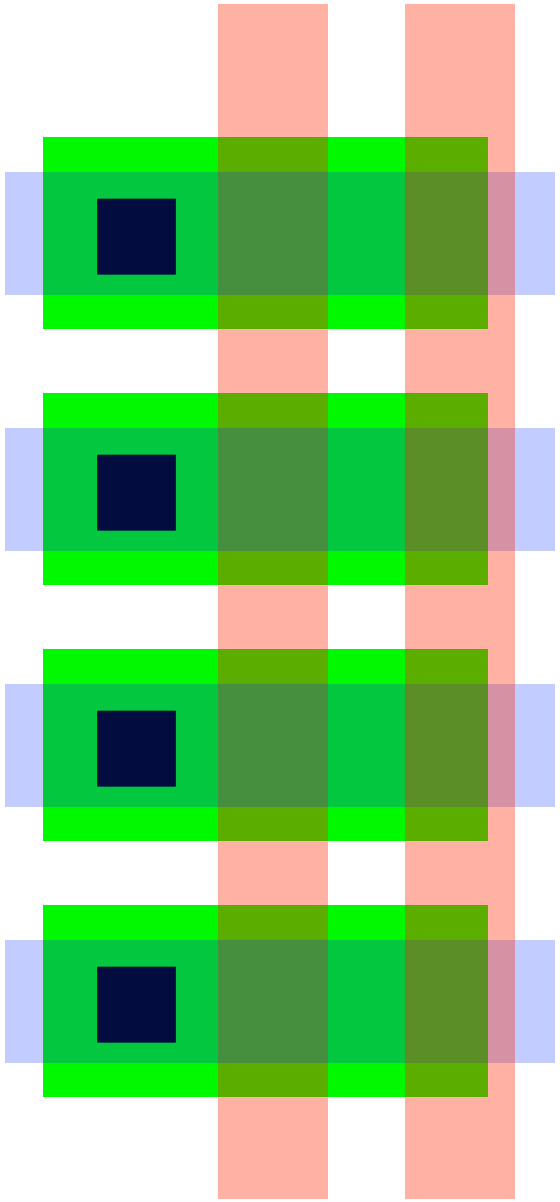


UC Regents Spring 2005 © UCB

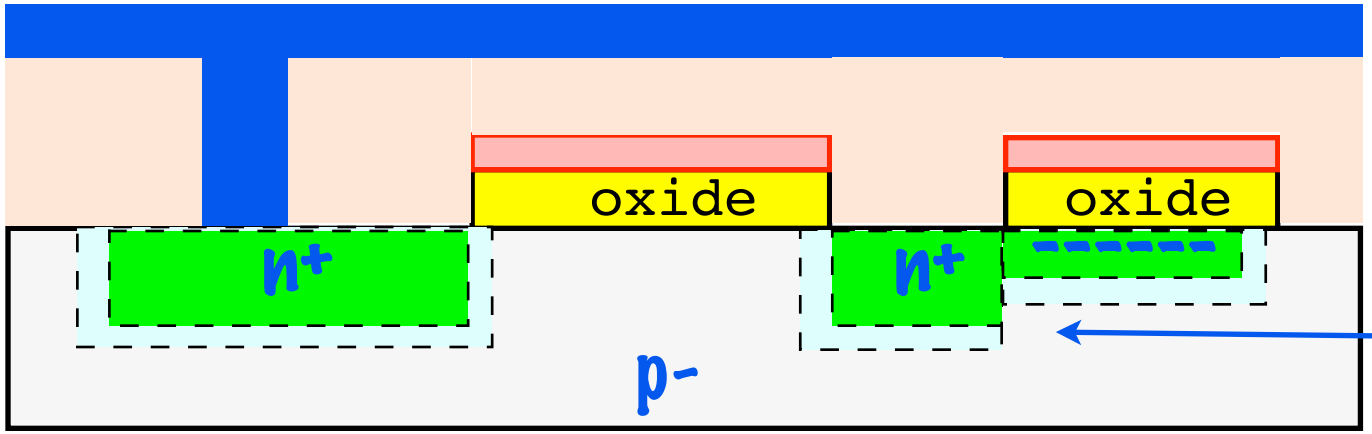
# DRAM Challenge #4: Leakage ...




Parasitic currents leak away charge.



Solution: "Refresh", by reading cells at regular intervals (tens of milliseconds)

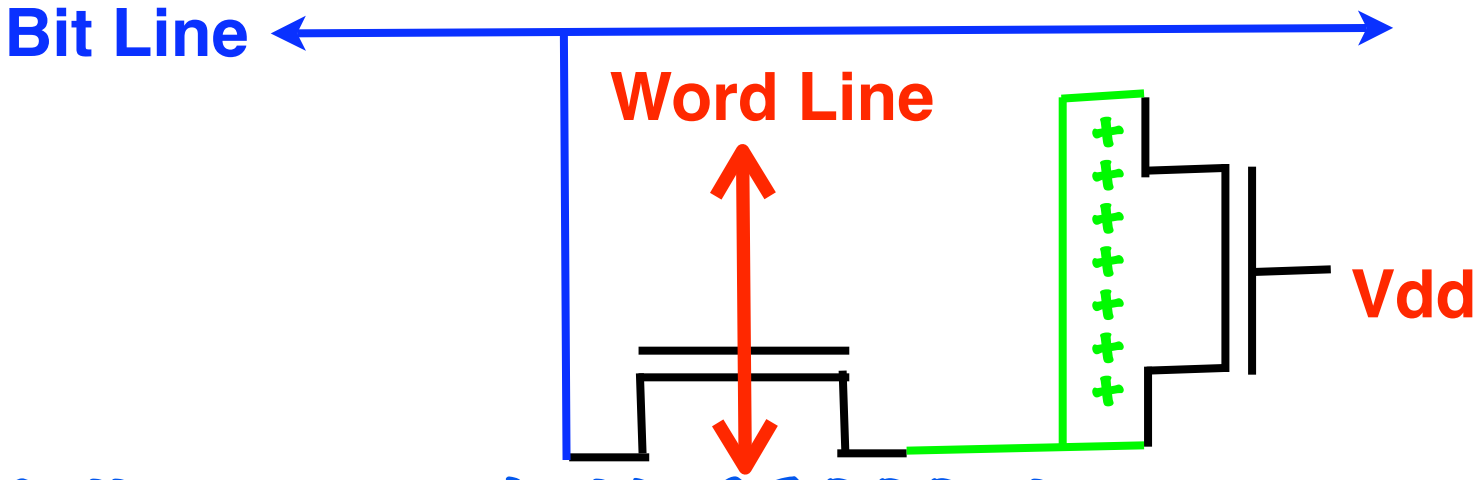


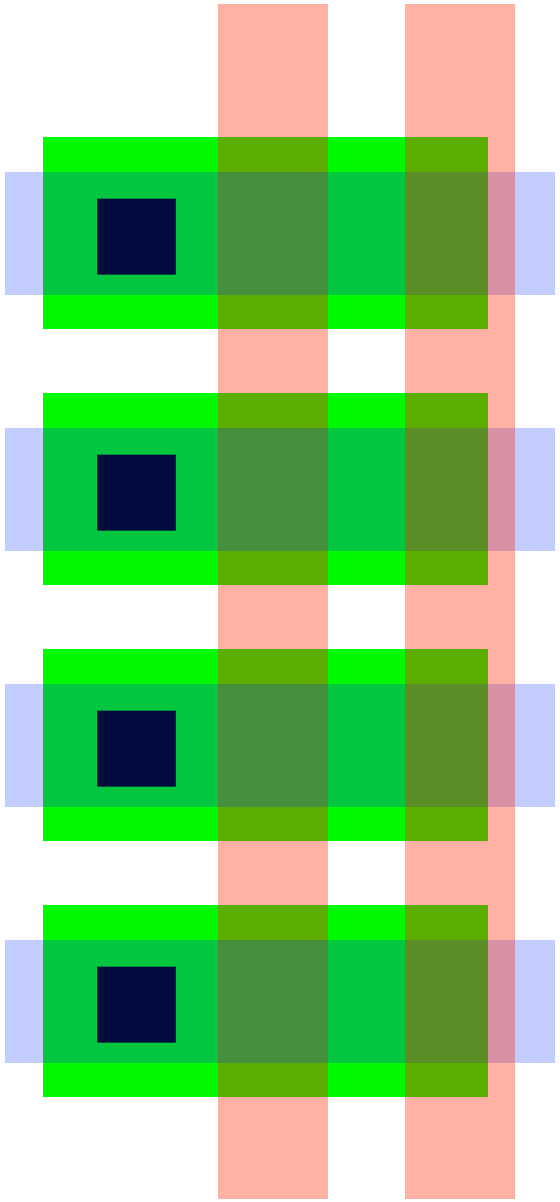

Diode leakage ...



UC Regents Spring 2005 © UCB

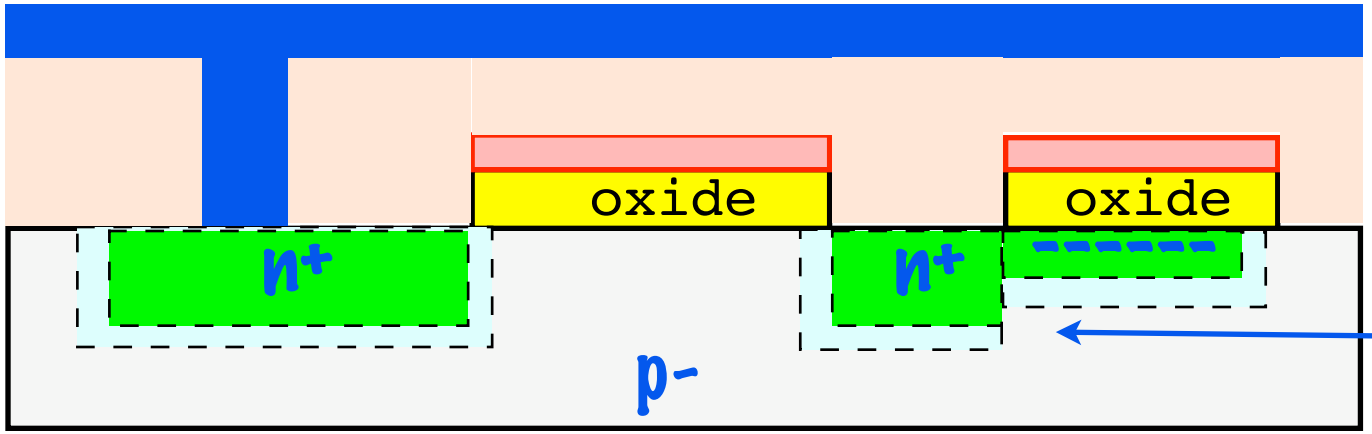
# DRAM Challenge #5: Cosmic Rays ...



Cell capacitor holds 25,000 electrons (or less). Cosmic rays that constantly bombard us can release the charge!

Solution: Store extra bits to detect and correct random bit flips (ECC).




Cosmic ray hit.



UC Regents Spring 2005 © UCB

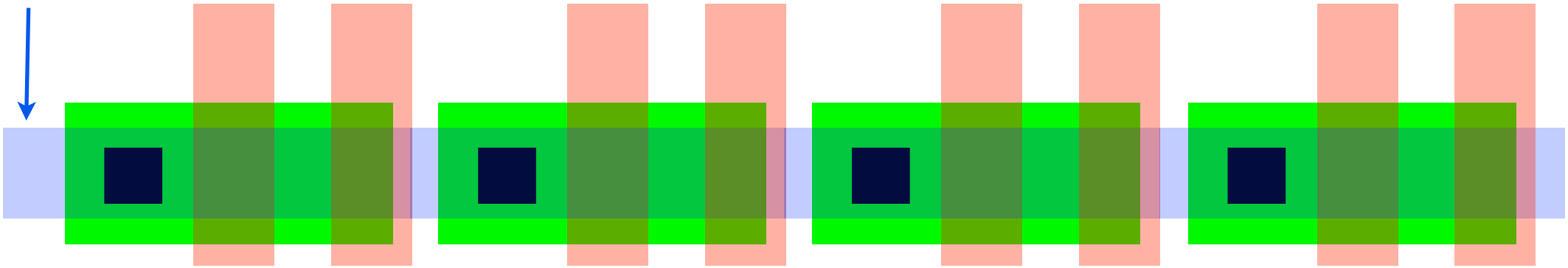
# DRAM Challenge 6: Yield

[...]

If one bit is bad, do we throw chip away?

Solution: add extra word lines (i.e. 80 when you only need 64). During testing, find the bad word lines, and use high current to burn away "fuses" put on chip to remove them.

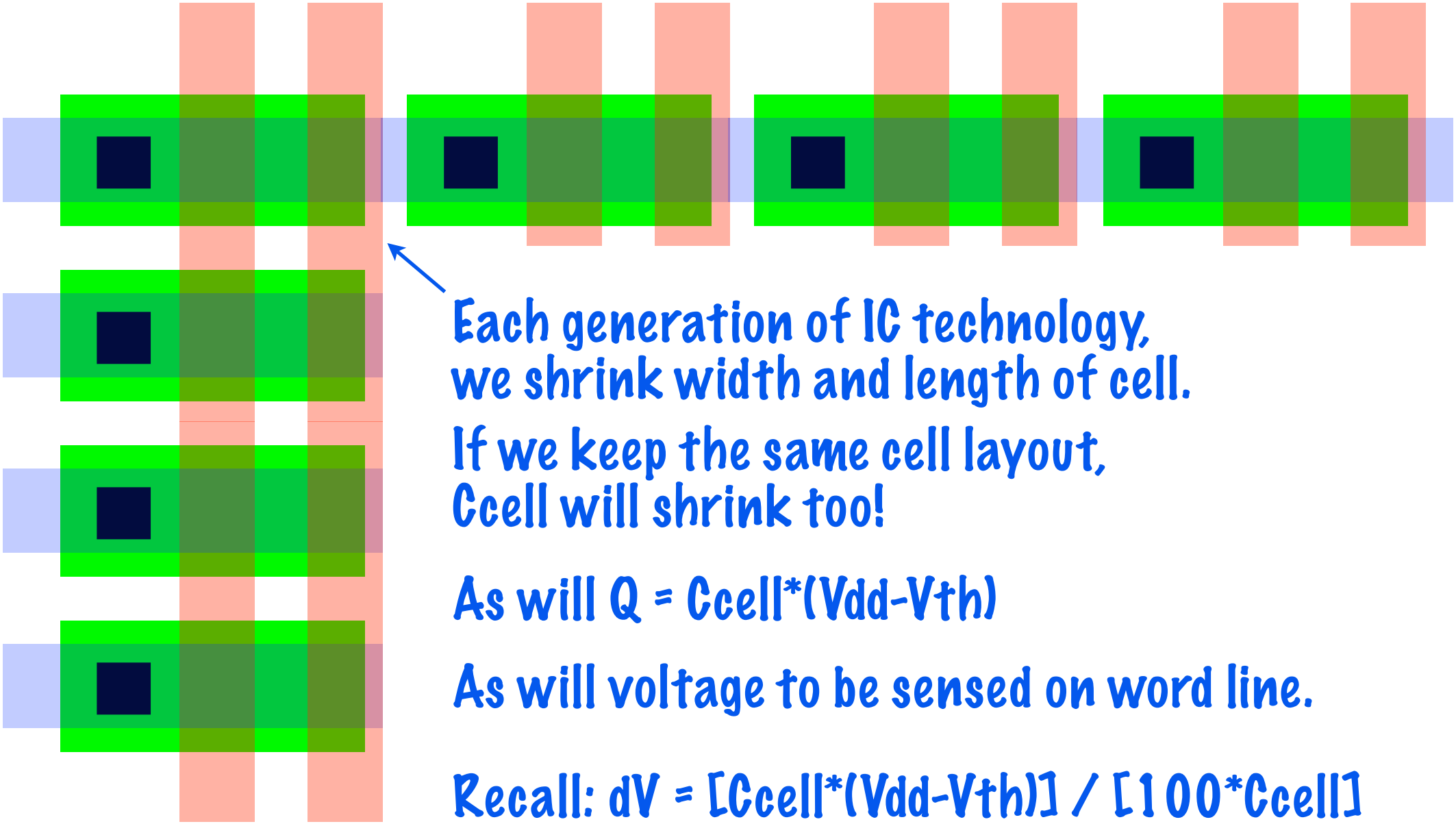
Extra word lines. Used for "sparing".





UC Regents Spring 2005 © UCB

# DRAM Challenge 7: Scaling



Each generation of IC technology, we shrink width and length of cell.

If we keep the same cell layout, Ccell will shrink too!

As will Q = Ccell*(Vdd-Vth)

As will voltage to be sensed on word line.

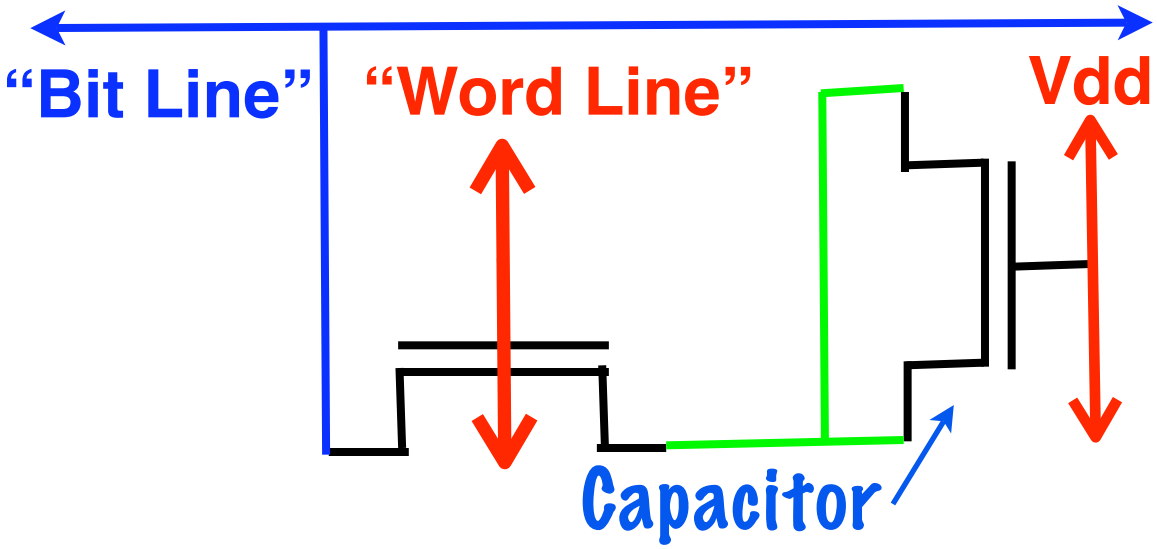
Recall: dV = [Ccell*(Vdd-Vth)] / [100*Ccell]

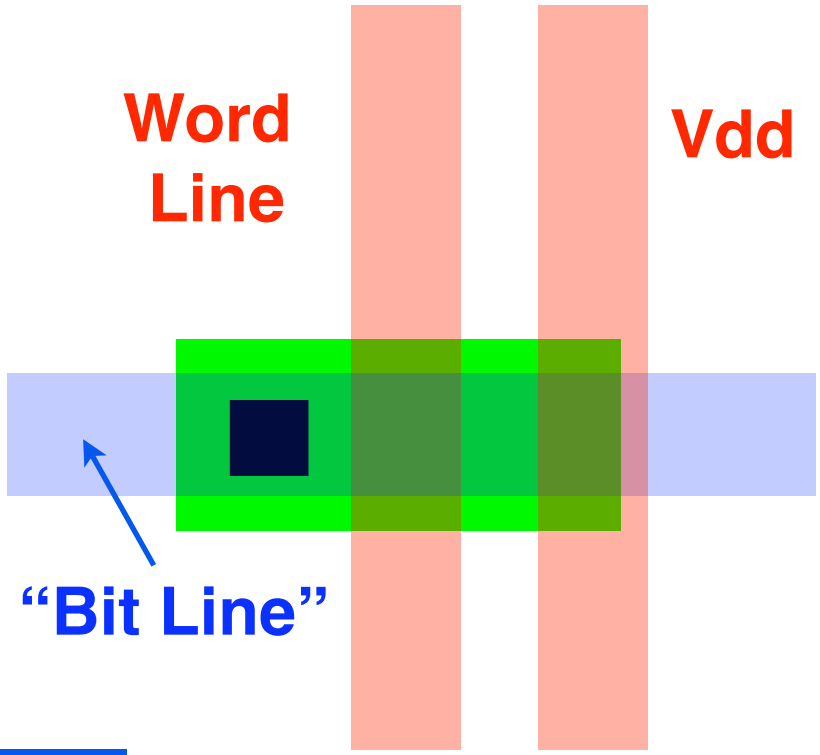
**Solution: Constant Innovation of Cell Capacitors!**

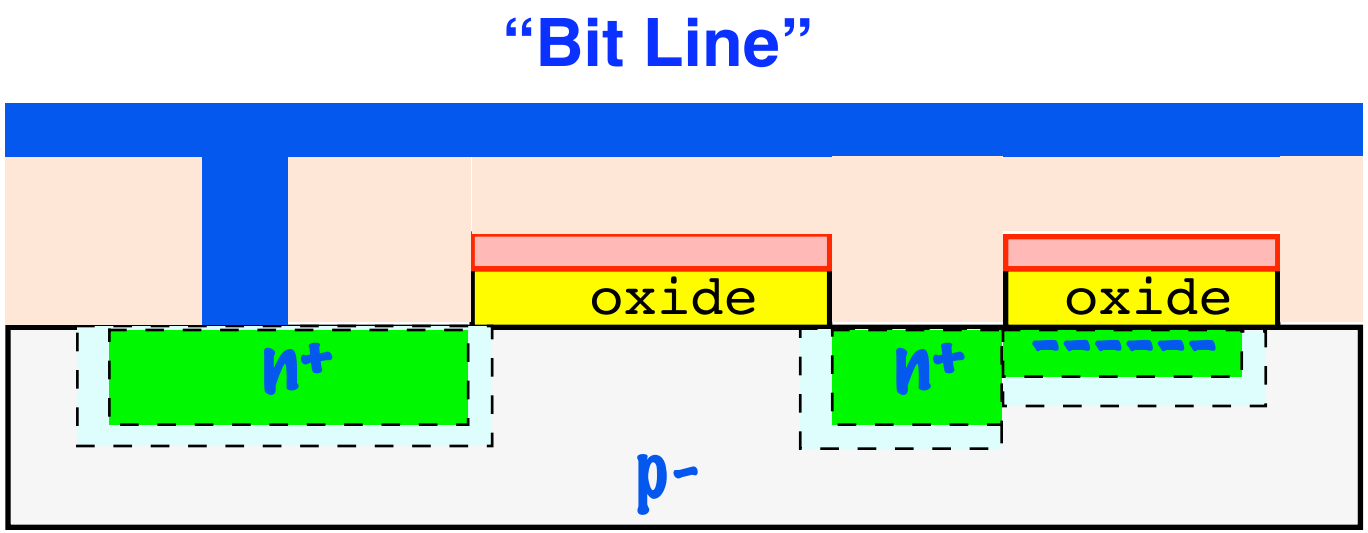


UC Regents Spring 2005 © UCB

# Poly-diffusion Ccell is ancient history




Word Line and Vdd run on "z-axis"



UC Regents Spring 2005 © UCB

# Modern cells: “trench” capacitors

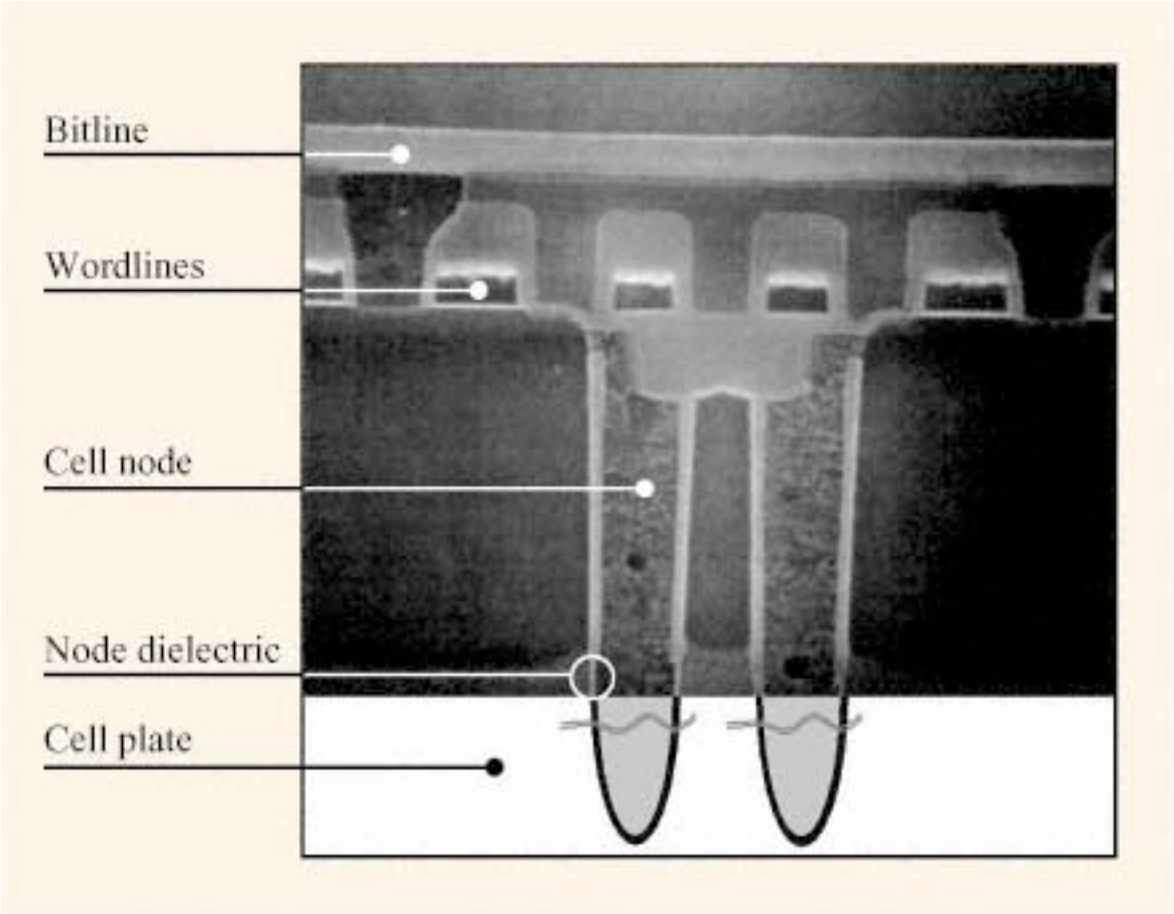



Figure 4

SEM photomicrograph of 0.25-$\mu$m trench DRAM cell suitable for scaling to 0.15$\mu$m and below. Reprinted with permission from [17]; © 1995 IEEE.



UC Regents Spring 2005 © UCB

# Modern cells: “stacked” capacitors

UC Regents Spring 2005 © UCB

# Lectures: Coming up next ...

| | | |
|---|---|---|
| | Th 2/24 | VLSI II |
| | F 2/25 | |
| | Sa 2/26 | |
| | Su 2/27 | |
| | M 2/28 | |
| | T 3/1 | DRAM |
| | W 3/2 | |
| | Th 3/3 | Cache I |

Transistor equations, basic memory circuits.

Memory array structures and interfaces.

The memory hierarchy



UC Regents Spring 2005 © UCB