## CS152: Section 2

## Q1. Iron Law

Q1.1: For each term in the Iron Law, give at least three techniques that improve that term. Instructions/program:

Cycles/instruction:

Time/cycle:

Q1.2: Explain how each term changes given the proposed modification (increase / decrease / no effect).
[Quiz 1, 2011] In a classic RISC pipeline, modify the ISA (and thus the microarchitecture) to use hardware interlocking instead of software interlocking for both branch delay slots and load-use delay slots

Instructions/program:

Cycles/instruction:

Time/cycle:
[Quiz 1, 2013] Remove hardware floating-point instructions and instead use software subroutines for floating-point arithmetic

Instructions/program:

Cycles/instruction:

Time/cycle:

## Q2. Pipelining

Q2.1: What does the following code do? How many iterations does it run?

|  | ADDI | x2, x0, $0 \times 700$ |
| :---: | :---: | :---: |
| LOOP: | ADD | x1, x2, x0 |
|  | LW | x2, 4 (x2) |
|  | BNE | x2, x0, LOOP |


| Memory | Memory |
| :--- | :--- |
| Address | Value |
| $0 \times 400$ | $0 \times 000$ |
| $0 \times 404$ | $0 \times D 40$ |
| $\ldots$ |  |
| $0 \times 700$ | $0 \times 9 F 0$ |
| $0 \times 704$ | $0 \times 400$ |
| $\ldots$ |  |
| $0 \times 9 F 0$ | $0 \times 400$ |
| $0 \times 9 F 4$ | $0 \times 000$ |
| $\ldots$ |  |
| $0 x D 40$ | $0 \times 000$ |
| 0xD44 | $0 \times 9 F 0$ |

Q2.2: Fill out the pipeline diagram for the following pipeline, assuming that branches are always predicted not taken.


- What is the CPI for the given code sequence?
- Consider splitting MEM into two stages, M1 and M2. How does the CPI change?
- What is the CPI if the BNE is always correctly predicted?

Q2.3: Fill out the pipeline diagram for the following pipeline, assuming that branches are always predicted not taken. [M. Golden and T. Mudge, "A comparison of two pipeline organizations", 1994]


- What is the CPI for the given code sequence?
- Consider splitting EX/MEM into two stages, M1 and EX/M2. How does the CPI change?
- What is the CPI if the BNE is always correctly predicted?

Q2.4: Suppose that the "load-use interlock" (LUI) pipeline from Q2.2 meets timing at 1 GHz . What is the minimum frequency at which the "address-generation interlock" (AGI) pipeline from Q2.3 performs better on the given code sequence, assuming perfect branch prediction?

Q2.5: Under what circumstances might you consider using the AGI pipeline design over the LUI pipeline?



