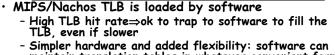
CS162 Operating Systems and Systems Programming Lecture 15

Page Allocation and Replacement

March 19, 2008 Prof. Anthony D. Josep http://inst.eecs.berkeley.edu/~cs162

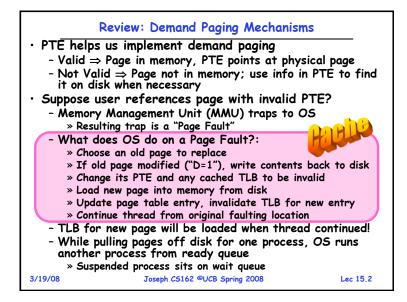
Review: Software-Loaded TLB



maintain translation tables in whatever convenient format

- How can a process run without hardware TLB fill?
- Fast path (TLB hit with valid=1):
 - » Translation to physical page done by hardware
- Slow path (TLB hit with valid=0 or TLB miss) » Hardware receives a TLB Fault
- What does OS do on a TLB Fault?
- » Traverse page table to find appropriate PTE
- » If valid=1, load page table entry into TLB, continue thread
- » If valid=0, perform "Page Fault" detailed previously
- » Continue thread
- Everything is transparent to the user process:
 - It doesn't know about paging to/from disk
- It doesn't even know about software TLB handling

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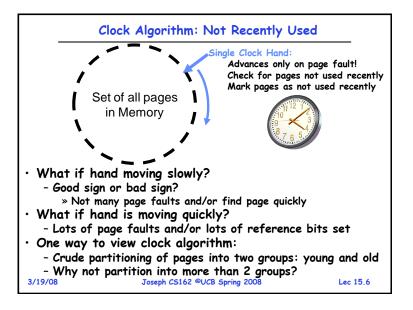


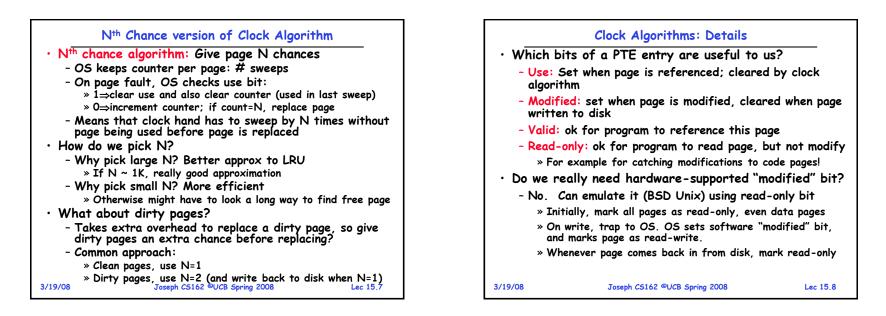
Review: Implementing LRU
· Perfect:
- Timestamp page on each reference
 Keep list of pages ordered by time of reference
- Too expensive to implement in reality for many reasons
• Clock Algorithm: Arrange physical pages in circle with
single clock hand
- Approximate LRU (approx to approx to MIN)
- Replace an old page, not the oldest page Set of all pages
• Details:
- Hardware "use" bit per physical page:
» Hardware sets use bit on each reference > If use bit isn't set, means not referenced in a long time
» Nachos hardware sets use bit in the TLB; you have to copy
this back to page table when TLB entry gets replaced
- On page fault:
» Advance clock hand (not real time)
» Check use bit: 1→used recently; clear and leave alone 0→selected candidate for replacement
- Will always find a page or loop forever?
» Even if all use bits set, will eventually loop around⇒FIFO 3/19/08 Set will eventually loop around⇒FIFO Lec 15.4

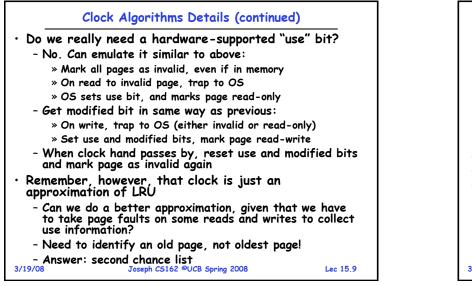


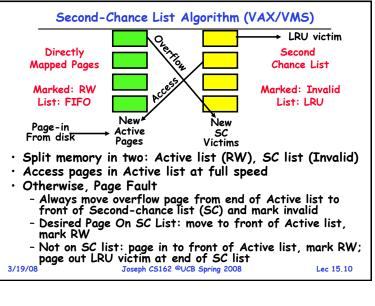
- Page Replacement Policies
 - Clock Algorithm, Nth chance algorithm, 2nd-Chance-List Algorithm
- Page Allocation Policies
- Working Set/Thrashing
- Distributed Problems
 - Brief History
 - Parallel vs. Distributed Computing
 - Parallelization and Synchronization
 - Prelude to MapReduce

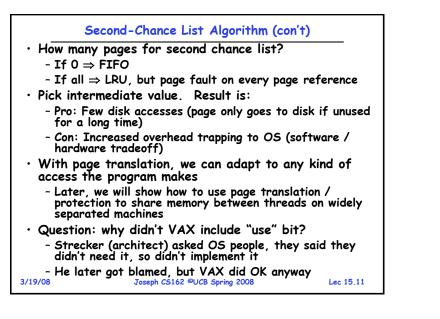
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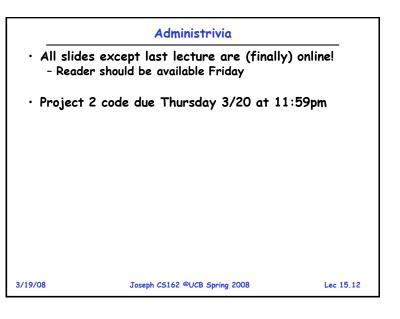




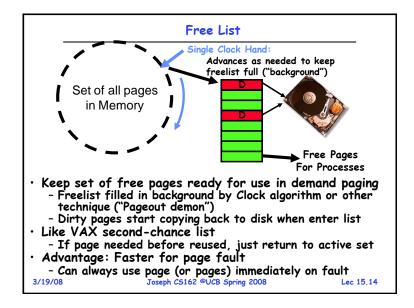








Strict powers	of 10:	• Strict pow	ers of 2:
- yotta:	10 ²⁴	- yotta:	2 ⁸⁰ ≅ 10 ²⁴
- exa:	10 ¹⁸	- exa:	2 ⁶⁰ ≅ 10 ¹⁸
- peta:	10 ¹⁵	- peta:	2 ⁵⁰ ≅ 10 ¹⁵
- tera:	10 ¹²	- tera:	2 ⁴⁰ ≅ 10 ¹²
- giga:	10 ⁹	- giga:	2 ³⁰ = 1,073,741,824 ≅ 10 ⁹
- mega:	10 ⁶	- mega:	2 ²⁰ = 1,048,576 ≅ 10 ⁶
- kilo:	10 ³	- kilo:	$2^{10} = 1024 \cong 10^3$
- milli(m):	10 ⁻³		
- micro (μ):	10-6	 When to use one or the other? Powers of 2 Memory sizes 	
- nano(n):	10 ⁻⁹		
- pico:	10-12		
- femto:	10 ⁻¹⁵	- Powers	
- atto:	10 ⁻¹⁸	» Time » Banc	
- yocto:	10-24	» Dano	awia in



 Want to make sure that all processs that are loaded into memory can make forward progress Example: IBM 370 - 6 pages to handle SS MOVE instruction: instruction is 6 bytes, might span 2 pages 2 pages to handle from 2 pages to handle to Possible Replacement - process selects replacement frame from set of all frames; one process can take a frame from another Local replacement - each process selects from only its own set of allocated frames 		
 boes every process get the same fraction of memory? Different fractions? Should we completely swap some processes out of memory? Each process needs <i>minimum</i> number of pages Want to make sure that all processes that are loaded into memory can make forward progress Example: IBM 370 - 6 pages to handle SS MOVE instruction:	_	
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set of allocated frames	TEs	from set of all frames; one process can take a frame
c 15.15 3/19/08 Joseph CS162 ©UCB Spring 2008 Lec 15.16		
	c 15.15	3/19/08 Joseph CS162 ©UCB Spring 2008 Lec 15.16

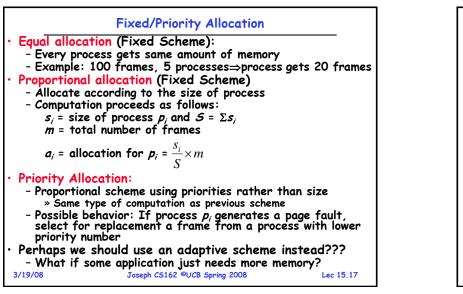
Demand Paging (more details)

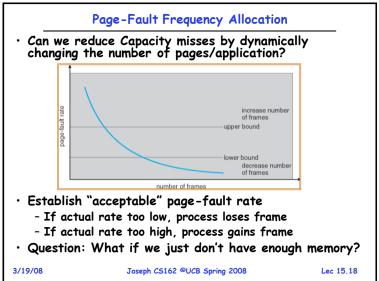
- Does software-loaded TLB need use bit? Two Options:
 - Hardware sets use bit in TLB; when TLB entry is replaced, software copies use bit back to page table
 - Software manages TLB entries as FIFO list; everything not in TLB is Second-Chance list, managed as strict LRU
- Core Map
 - Page tables map virtual page \rightarrow physical page
 - Do we need a reverse mapping (i.e. physical page \rightarrow virtual page)?
 - » Yes. Clock algorithm runs through page frames. If sharing, then multiple virtual-pages per physical page
 - » Can't push page out to disk without invalidating all PTEs

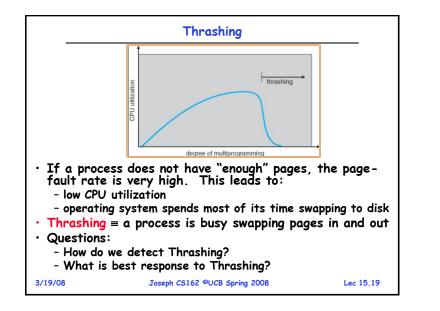
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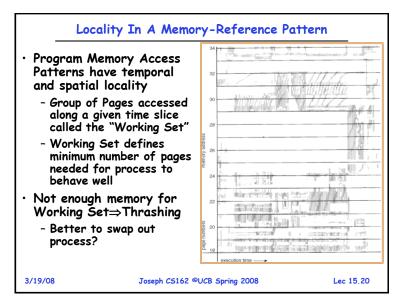
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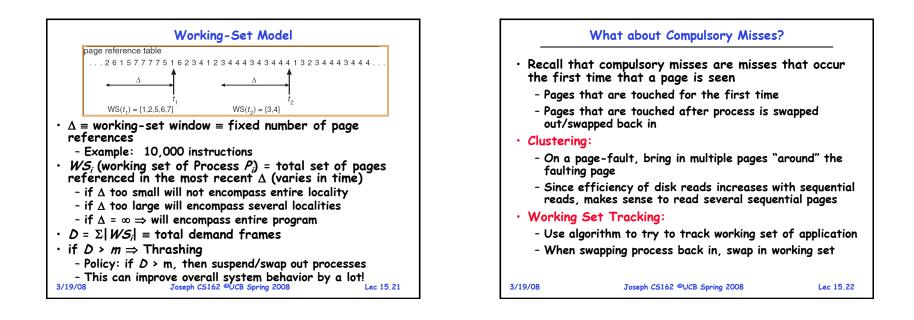
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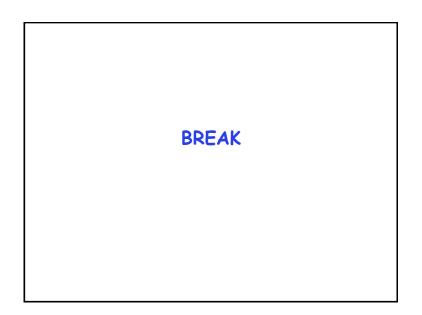


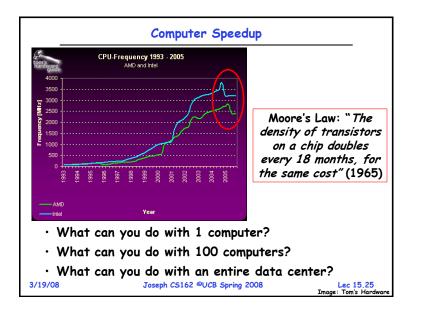


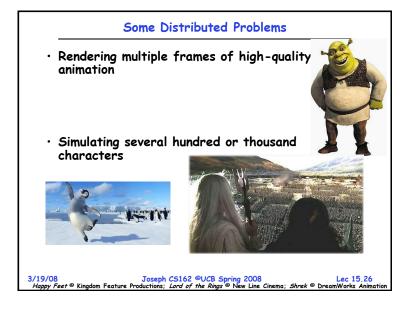


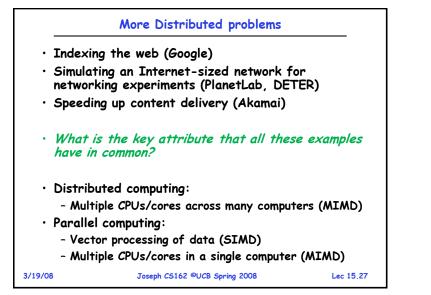


· Replaceme		
	lace pages on queue, replace page o eplace page that will be used farthe	at end est in future
	place page used farthest in past	
· Clock Algo	rithm: Approximation to LRU	
- Arrange	all pages in circular list	
- Sweep t	hrough them, marking as not "in use	e″ _
- It page	not "in use" for one pass, than can	replace
· N''-chanc	e clock algorithm: Another appro es multiple passes of clock hand be	IX LKU fono nonlecino
	nance List algorithm: Yet another	
 Divide p and man Working S 	ages into two groups, one of which aged on page faults.	is truly LRU
	bages touched by a process recently	,
 Thrashing Process 	 a process is busy swapping page will thrash if working set doesn't fi swap out a process 	es in and out
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A Brief History... 1975-85

1975-85:

- Primarily vector-based parallel computing in early years
- Gradually more thread-based parallelism introduced

1985-95:

- "Massively parallel architectures" rise in prominence
- Message Passing Interface (MPI) and other libs developed

Cray 2 supercomputer

(Wikipedia)

Lec 15.28

- Bandwidth was a big problem

1995-today:

- Berkeley Network of Workstations
 » COTS tech instead of special node machines
- Cluster/grid architecture increasing
- Web-wide cluster software

» Microsoft, Google, Amazon take this to the extreme (thousands of nodes/cluster) 3/19/08 Joseph CS162 @UCB Spring 2008

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