

Recall: Motivating Example: "Too Much Milk"

 Great thing about OS's – analogy between problems in OS and problems in real life

- Help you understand real life problems better

- But, computers are much stupider than people
- · Example: People need to coordinate:

Time	Person A	Person B
3:00	Look in Fridge. Out of milk	
3:05	Leave for store	
3:10	Arrive at store	Look in Fridge. Out of milk
3:15	Buy milk	Leave for store
3:20	Arrive home, put milk away	Arrive at store
3:25		Buy milk
3:30		Arrive home, put milk away

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Lec 8.3









• I'm not getting milk, You're getting milk

This kind of lockup is called "starvation!"



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	 Too Much Milk: Solution #4? eccal our target lock interface: acquire(&milklock) – wait until lock is free, then grab release(&milklock) – Unlock, waking up anyone waiting These must be atomic operations – if two threads are waiting for the lock and both see it's free, only one succeeds to grab the lock Then, our milk problem is easy: acquire(&milklock); if (nomilk); buy milk; release(&milklock); 		Where are we going with synchronization? Programs Shared Programs Higher- level API Locks Semaphores Monitors Send/Receive Hardware Locd/Store Disable Ints Test&Set Compare&Swap • We are going to implement various higher-level synchronization primitives using atomic operations Everything is pretty painful if only atomic primitives are load and store • Need to provide primitives useful at user-level Synchronization	
2/9/2023	Kubiatowicz CS162 © UCB Spring 2023	Lec 8.21	2/9/2023 Kubiatowicz CS162 © UCB Spring 2023	Lec 8.22
2/9/2023	 Administrivia Mideem Next Thursday (February 16, 7-9pm)! No class on day of midterm Thave extra office hours during class time Dipect 1 Design Document Due Date moved to Saturdays Project 1 Design reviews upcoming High-level discussion of your approach Ny and algorithm will you use? No and need final design (complete with all semicolons!) Pouvel I be asked about testing Ne there things you are doing that are not tested by tests we give you? Design of your apyroach strom previous terms Hease do not the find solutions from previous terms Hease do not the offic solutions from previous terms Hease do not not not not not not not not not no	Lec 8.23	<section-header><section-header><section-header><list-item><list-item><list-item><list-item><list-item><list-item><list-item><list-item><list-item><list-item><list-item><list-item><list-item><list-item><list-item><list-item><list-item><list-item><list-item><list-item><list-item><list-item><list-item><list-item><list-item><list-item><list-item><list-item><list-item><list-item></list-item></list-item></list-item></list-item></list-item></list-item></list-item></list-item></list-item></list-item></list-item></list-item></list-item></list-item></list-item></list-item></list-item></list-item></list-item></list-item></list-item></list-item></list-item></list-item></list-item></list-item></list-item></list-item></list-item></list-item></section-header></section-header></section-header>	Lec 8.24



New Lock Implementation: Discussion



- Avoid interruption between checking and setting lock value.
- Prevent switching to other thread that might be trying to acquire lock!
- Otherwise two threads could think that they both have lock!



- Note: unlike previous solution, this "meta-"critical section is very short
 - User of lock can take as long as they like in their own critical section: doesn't impact global machine behavior
 - Critical interrupts taken in time!

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What about Interrupt Re-enable in Going to Sleep?











In-Kernel Lock: Simulation



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In-Kernel Lock: Simulation

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Examples of Read-Modify-Write Atomic Read-Modify-Write Instructions test&set (&address) { /* most architectures */ · Problems with previous solution: result = M[address]; // return result from "address" and - Can't give lock implementation to users M[address] = 1; // set value at "address" to 1 return result: - Doesn't work well on multiprocessor } » Disabling interrupts on all processors requires messages and would be swap (&address, register) { /* x86 */ temp = M[address]; // swap register's value to very time consuming // value at "address" M[address] = register; // value from "address" put back to register register = temp; Alternative: atomic instruction sequences // value from "address" considered return from swap return temp; - These instructions read a value and write a new value atomically compare&swap (&address, reg1, reg2) { /* x86 (returns old value), 68000 */ - Hardware is responsible for implementing this correctly if (reg1 == M[address]) { // If memory still == reg1, M[address] = reg2; // then put reg2 => memory » on both uniprocessors (not too hard) return success: » and multiprocessors (requires help from cache coherence protocol) } else { // Otherwise do not change memory return failure: - Unlike disabling interrupts, can be used on both uniprocessors and } multiprocessors } load-linked&store-conditional(&address) { /* R4000, alpha */ loop: 11 r1, M[address]; movi r2, 1; // Can do arbitrary computation sc r2, M[address]; beqz r2, loop; 2/9/2023 2/9/2023 Kubiatowicz CS162 © UCB Spring 2023 Lec 8.42 Kubiatowicz CS162 © UCB Spring 2023 Lec 8 41 }

Using of Compare&Swap for queues



Implementing Locks with test&set



Problem: Busy-Waiting for Lock Multiprocessor Spin Locks: test&test&set · Positives for this solution · A better solution for multiprocessors: // (Free) Can access this memory location from user space! - Machine can receive interrupts int mylock = 0; // Interface: acquire(&mylock); - User code can use this lock release(&mylock); acquire(int *thelock) { - Works on a multiprocessor do { · Negatives while(*thelock); // Wait until might be free (quick check/test!) while(test&set(thelock)); // Atomic grab of lock (exit if succeeded) This is very inefficient as thread will consume cycles waiting } - Waiting thread may take cycles away from thread holding lock (no one wins!) release(int *thelock) { - Priority Inversion: If busy-waiting thread has higher priority than thread holding lock *thelock = 0: // Atomic release of lock \Rightarrow no progress! Simple explanation: Priority Inversion problem with original Martian rover - Wait until lock might be free (only reading - stays in cache) • For higher-level synchronization primitives (e.g. semaphores or monitors), - Then, try to grab lock with test&set waiting thread may wait for an arbitrary long time! - Repeat if fail to actually get lock - Thus even if busy-waiting was OK for locks, definitely not ok for other primitives · Issues with this solution: - Homework/exam solutions should avoid busy-waiting! - Busy-Waiting: thread still consumes cycles while waiting » However, it does not impact other processors!





Try #3: Better, using more atomics



Recall: Where are we going with synchronization?

Programs	Shared Programs
Higher- level API	Locks Semaphores Monitors Send/Receive
Hardware	Load/Store Disable Ints Test&Set Compare&Swap

- We are going to implement various higher-level synchronization primitives using atomic operations
 - Everything is pretty painful if only atomic primitives are load and store

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- Need to provide primitives useful at user-level

Producer-Consumer with a Bounded Buffer

- · Problem Definition
 - Producer(s) put things into a shared buffer
 - Consumer(s) take them out
 - Need synchronization to coordinate producer/consumer
- Don't want producer and consumer to have to work in lockstep, so put a fixed-size buffer between them
 - Need to synchronize access to this buffer
 - Producer needs to wait if buffer is full
 - Consumer needs to wait if buffer is empty
- Example 1: GCC compiler
 - cpp | cc1 | cc2 | as | ld
- Example 2: Coke machine
 - Producer can put limited number of Cokes in machine
 - Consumer can't take Cokes out if machine is empty
- Others: Web servers, Routers,



Bounded Buffer Data Structure (sequential case)

typedef struct buf {
 int write_index;
 int read_index;
 <type> *entries[BUFSIZE];
} buf_t;



- Insert: write & bump write ptr (enqueue)
- Remove: read & bump read ptr (dequeue)
- How to tell if Full (on insert) Empty (on remove)?
- And what do you do if it is?
- What needs to be atomic?

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Semaphores Like Integers Except...

- Semaphores are like integers, except:
 - No negative values
 - Only operations allowed are P and V can't read or write value, except initially
 - Operations must be atomic
 - » Two P's together can't decrement value below zero
 - » Thread going to sleep in P won't miss wakeup from V even if both happen at same time
- · POSIX adds ability to read value, but technically not part of proper interface!
- · Semaphore from railway analogy
 - Here is a semaphore initialized to 2 for resource control:



Two Uses of Semaphores

- Mutual Exclusion (initial value = 1)
- Also called "Binary Semaphore" or "mutex".
- · Can be used for mutual exclusion, just like a lock:

semaP(&mysem);
 // Critical section goes here
semaV(&mysem);

Scheduling Constraints (initial value = 0)

- Allow thread 1 to wait for a signal from thread 2
 - thread 2 schedules thread 1 when a given event occurs
- Example: suppose you had to implement ThreadJoin which must wait for thread to terminate:



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Revisit Bounded Buffer: Correctness constraints for solution

- Correctness Constraints:
 - Consumer must wait for producer to fill buffers, if none full (scheduling constraint)
 - Producer must wait for consumer to empty buffers, if all full (scheduling constraint)
 - Only one thread can manipulate buffer queue at a time (mutual exclusion)
- Remember why we need mutual exclusion
 - Because computers are stupid
 - Imagine if in real life: the delivery person is filling the machine and somebody comes up and tries to stick their money into the machine
- General rule of thumb: Use a separate semaphore for each constraint
 - Semaphore fullBuffers; // consumer's constraint
 - Semaphore emptyBuffers;// producer's constraint
 - Semaphore mutex; // mutual exclusion

Bounded Buffer, 3rd cut (coke machine)



2/9/2023

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2/9/2023	<section-header> Summary (1/2) Important concept: Atomic Operations An operation that runs to completion or not at all These are the primitives on which to construct various synchronization primitives Isabling of Interrupts, test&set, swap, compare&swap, load-locked & store-conditional Showed several constructions of Locks Must be very careful not to waste/tie up machine resources Shoudn't disable interrupts for long Shoudn't spin wait for long Shoudn't spin wait for long Showed primitive for constructing user-level locks Packages up functionality of sleeping </section-header>	Lec 8.75	 Semaphores: Like integers with restricted interface Two operations: P(): Wait if zero; decrement when becomes non-zero V(): Increment and wake a sleeping task (if exists) Can initialize value to any non-negative value Se an initialize value to any non-negative value Se aseparate semaphore for each constraint Monitors: A lock plus one or more condition variables Always acquire lock before accessing shared data Use condition variables to wait inside critical section Three Operations: Wait(), Signal(), and Broadcast() Monitors represent the logic of the program Quai if necessary Signal when change something so any waiting threads can proceed Rest time: More complex monitor example Readers/Writers in depth 	Lec 8.76