Homework 4: Page Walk

Due: Monday, July 27, 2020 at 11:59 PM PDT

Full Name	
Student ID	

Your task is to complete the problem below. If you are having trouble, look at the solutions to Problem 8 on the CS 162 Final Exam from Fall 2019. This homework does not have a coding portion.

Submission: Submit your work to Gradescope as a PDF file that matches this template. The intention is that you print out the template, write on the pages, and scan or take pictures of the pages for your submission. You may also fill out this template digitally (e.g., using a tablet). Do not add or remove pages.

1. (15 points) Consider an x86 computer with the following memory architecture:

   - 32-bit virtual address space
   - 32-bit physical address space
   - 4 KiB page size
   - Two-level page table (equal size at each level)
   - 4-entry, fully associative TLB, unified for both instructions and data
   - 32-bit page table entry (PTE) size

   (a) (1 point) Describe which bits of the 32-bit virtual address are used for each part of the virtual address translation.

   bits [`31` : ____] are ________________________________

   bits [____ : ____] are ________________________________

   bits [____ : `0`] are ________________________________

   (b) (5 points) For the virtual address of the first instruction, `0x1084 0108`, fill in the value of each line. For each page accessed when fetching that instruction, give the byte offset of the reference into that page.

   Index of entry in Root Page Table: ____________________________

   Byte offset of PTE in Root PT page: ____________________________

   Index of entry in L2 Page Table: ____________________________

   Byte offset of PTE within L2 PT page: ____________________________

   Code page offset: ____________________________

The state of the machine described on the previous page is shown below. The contents of several frames of physical memory are shown on the right with physical addresses. On the left are several machine registers, including the page table base register (`cr3`), which contains the physical frame number of the root page table. The TLB is initially empty (i.e., all TLB entries are initially invalid). Page table entries have the valid flag as the most significant bit and the physical frame number of valid entries in the low order bits. For this problem, you may ignore all other flags in each page table entry.

Registers

`cr3` (PTBR)	`0x0001 0050`
`eax`	`0x1084 2104`
`ebx`	`0x1084 2100`
`ecx`	`0x1004 0108`
`edx`	`0x1004 0108`

Instructions

```
0x1084 0108 movl (%eax), %ecx
0x1084 010a movl %edx, (%ebx)
```

TLB Contents

Valid	Tag	Frame

Physical Memory

Phys. Addr.	Contents
`0x1001 0000`	
`...`	
`0x1001 0100`	`0x1044 2104`
`0x1001 0104`	`0x8001 0030`
`0x1001 0108`	`0x1389 018b`
`0x1002 0000`	
`...`	
`0x1002 0100`	`0x1004 2100`
`0x1002 0104`	`0x1084 1100`
`0x1002 0108`	`0x8001 0020`
`0x1003 0000`	
`...`	
`0x1003 0100`	`0x8001 0040`
`0x1003 0104`	`0x1084 0104`
`0x1003 0108`	`0x8001 0010`
`0x1004 0000`	
`...`	
`0x1004 0100`	`0x8001 0010`
`0x1004 0104`	`0x1044 2108`
`0x1004 0108`	`0x8001 0030`
`0x1005 0000`	
`...`	
`0x1005 0100`	`0x1044 1108`
`0x1005 0104`	`0x8001 0030`
`0x1005 0108`	`0x8001 0040`

(c) (9 points) **You are to step through the instructions whose addresses and disassembly are shown on the previous page.** In the space provided below, write down the operation, address, and value associated with every memory access associated with the instructions, by filling in the blank cells in the table. For reads, the "Value" field should contain the data read from physical memory; for writes, it should contain the data written to physical memory. **Only include accesses to physical memory in the table; do not include changes to register values or updates to the TLB as separate rows in the table.** If you wish, you may update the state of the memory, registers, and TLB by writing on the figure on the previous page. **You may not need all of the rows provided in the table.** If a page fault occurs, then you should indicate in the "Comment" column that a page fault occurred and stop executing the instructions, leaving the remaining lines blank. Otherwise, filling out the "Comment" field is optional, and serves only to explain your reasoning to help us award partial credit.

Operation	Address	Value	TLB Hit?	Comment