GCD: VLSI's Hello World

CS250 Laboratory 1 (Version 090512)
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Overview

The goal of this assignment is to get you familiar with the VLSI CAD tools you will be using throughout the semester. You will learn about each of the stages in the ASIC tool flow, and get a chance to do some Chisel coding. Specifically, you will write an RTL model of a greatest common divisor (GCD) circuit, synthesize and place and route the design, verify its correctness by simulating at each stage (RTL, post-synthesis, post place and route), and perform power analysis.

Deliverables

This lab is due **Tuesday, September 11th at 11 AM**. The deliverables for this lab are:

- (a) your working Chisel RTL checked into your private git repository at Github
- (b) build results and reports generated by VCS, DC Compiler, Formality, IC Compiler, PrimeTime PX checked into your git repo
- (c) written answers to the questions given at the end of this document checked into your git repository as `writeup/report.pdf` or `writeup/report.txt`

You are encouraged to discuss your design with others in the class, but you must turn in your own work.

VLSI Toolflow Introduction

Figure 1 illustrates the toolflow you will be using for the first lab. You will use Synopsys VCS (`vcs`) to *simulate* and *debug* your RTL design. After you get your design right, you will use Synopsys Design Compiler (`dc_shell-xg-t`) to *synthesize* the design. Synthesis is the process of transforming an RTL model into a gate-level netlist. You will use Synopsys Formality (`fm_shell`) to *formally verify* that the RTL model and the gate-level model *match*. VCS is used again to simulate the synthesized gate-level netlist. After obtaining a working gate-level netlist, you will use Synopsys IC Compiler (`icc_shell`) to *place and route* the design. Placement is the process by which each standard cell is positioned on the chip, while routing involves wiring the cells together using traces on the various metal layers, with vias providing connections between the metal layers. The tools will provide feedback on the performance and area characteristics of your design after both synthesis and place and route. The results from place and route are more realistic but take much longer to produce. After placing and routing, you will generate and simulate the final gate-level netlist using VCS. You will use this gate-level simulation as a final verification step and to generate transition counts for every net in the design. Synopsys PrimeTime PX (`pt_shell`) takes these transition counts as input and correlates them with the capacitance values extracted from the final layout to estimate the power consumed by a design. The diagram below illustrates how the tools work together.

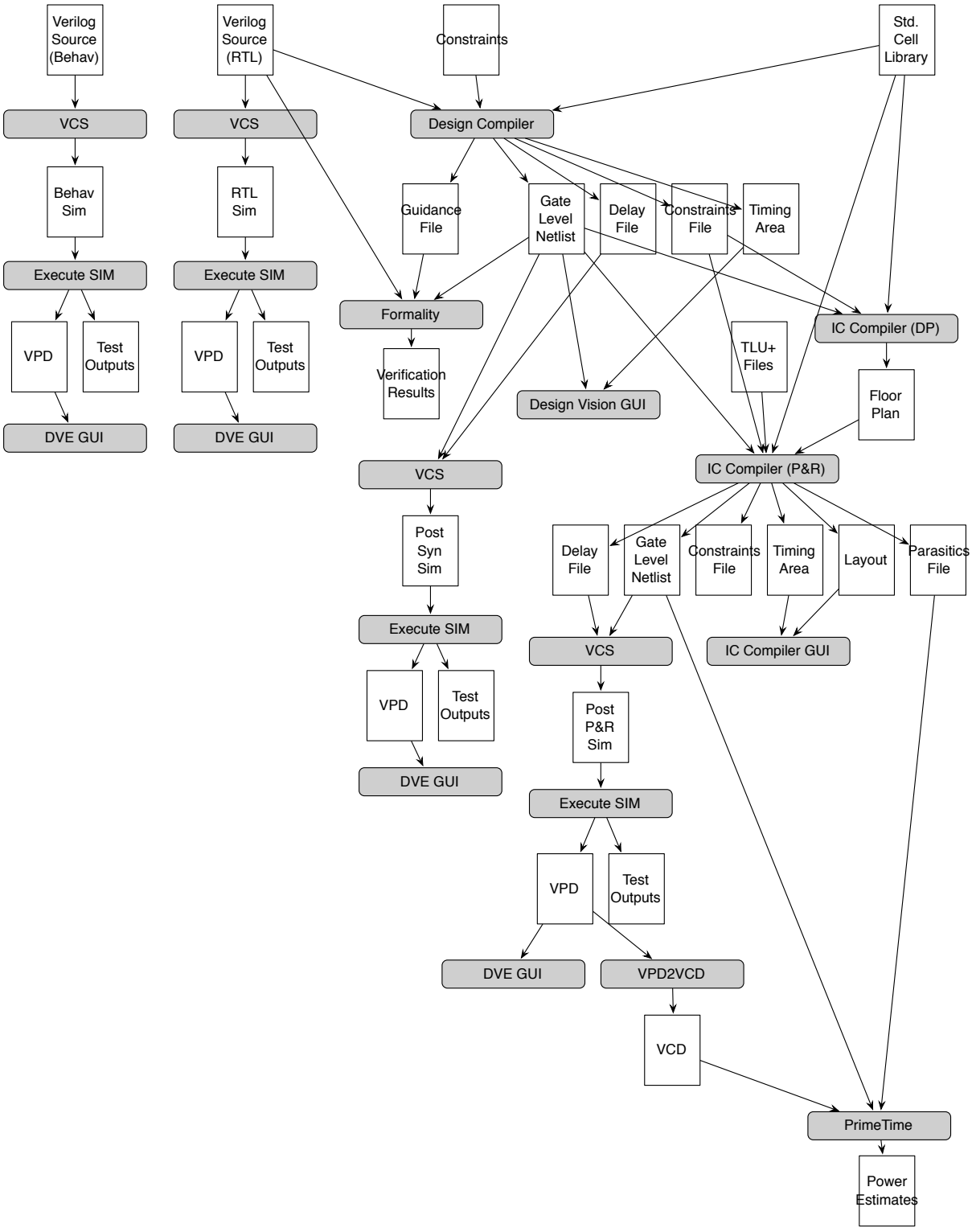

Figure 1: CS250 Toolflow for Lab 1

Prerequisites

As you can see from the diagram, many different tools are needed to take even a simple design from RTL all the way to a transistor-level implementation. Each tool is immensely complicated, and many engineers in industry specialize in only one. In order to produce a VLSI design in a single semester we will need to learn a bit about each one.

Each tool has a GUI interface. However, most of the commands you'll want to execute will be the same for every design iteration and become repetitive to type, so TCL scripts are used to automate these processes. When you use the GUI, in the terminal window you will see the command line that corresponds to each click, and these commands can be added to scripts. To keep files organized, each piece of the toolflow has its own build directory and its own Makefile. The Makefile initializes the program and points it at the setup scripts. A top-level Makefile runs each program in succession so that ideally, a single command can take an RTL design all of the way through the flow without any user intervention. This will facilitate design space exploration, by making it easy for you to modify some part of your design and see how the change impacts the power, area, and performancecharacteristics of the resulting chip.

Getting Started

You can follow along through with this lab by typing in the commands marked with a '%' symbol at the shell prompt. To cut and paste commands from this lab into your bash shell (and make sure bash ignores the '%' character) just use an alias to "undefine" the '%' character like this:

```
% alias %=""
```

Note: OS X Preview may not copy newlines correctly, if you have problems, try using Adobe Reader.

All of the CS250 laboratory assignments should be completed on one of the EECS Instructional machines allocated for the class. Please follow the setup instructions on the course website before attempting this lab. Remember, you will need to source a setup script before you can run the CAD tools. This script specifies the location of each tool and sets up necessary environment variables.

You will be using Git to manage your CS250 laboratory assignments. Please see *Tutorial 1: Using Git to Manage Source RTL* for more information about how to use Git. Each student will have a private git repository hosted on github.com. If you don't already have a Github account, you will need to create one. Once you have an account, you must send your Github account name and CS250 class account username to your TA before you will be able to access the lab materials.

The lab materials we provide will be hosted in a *template* repository. You will clone this template repository to a directory on the machine you're working on. Afterwards, you will set your remote repository to point at your private repository. This will create a local repository that is linked to two different remote repositories (one which is managed by the staff and is read only, while the other is your private repository). If any updates are made to the *template* repository, you should be able to easily merge the changes into your local repository.

As the CAD tools generate tons of data and your class account home directories have too low of a disk quota (not to mention network mounted filesystems are far slower than local disks), we will need to use the local disk of the machine to store the outputs of the CAD tools. By default, the permissions on a directory that you create in `work/` will be set to that its contents are only readable by your class account. You will use git to backup your design files to a server hosted by github. Assuming your username is `cs250-ab` (change this to your own class account username), you can create a local working git directory using the following command.

```
% cd /work/
% mkdir cs250-ab
% cd cs250-ab
% git init
% git remote add template https://github.com/ucberkeley-cs250/lab-templates.git
% git remote add origin https://github.com/ucberkeley-cs250/cs250-ab.git
```

To do this the lab you will make use of some infrastructure that we have provided. The infrastructure includes Makefiles, scripts, and the Verilog test harness required to complete the lab. The following commands fetch these files from the *template* repository, and then copy them into your private repository. To simplify the rest of the lab we will also define a '$LABROOT' environment variable which contains the absolute path to the project's top-level root directory.

```
  % cd /work/cs250-ab
  % git pull template master
Username for 'https://github.com': <github username>
Password for 'https://<username>@github.com':
remote: Counting objects: 191, done.
remote: Compressing objects: 100% (136/136), done.
remote: Total 191 (delta 41), reused 188 (delta 41)
Receiving objects: 100% (191/191), 185.87 KiB | 293 KiB/s, done.
Resolving deltas: 100% (41/41), done.
From https://github.com/ucberkeley-cs250/lab-templates
 * branch            master     -> FETCH_HEAD

  % git pull origin master
  ...
  % git push origin master
  ...
  % cd lab1-verilog
  % LABROOT=$PWD
```

So the two remote repositories are named *template* and *origin*. *origin* points to your private repository and *template* points to the read-only staff account. If the provided lab files are ever updated, a simple `git pull template master` will merge in these changes with your own local versions of the files.

Please run a git push as often as you can. `work/` is only intended as temporary storage and is not backed up.

Note: `work/` lives on a local drive, so if you ever decide to work on a different machine, you can push/pull your design files to/from github to move your design files from one machine's local drive to the other's. Follow the instructions below to move files between machines (assuming all the files of interest have already been committed to your local repository). This procedure will not move your build directories (you will need to rerun synthesis or place-and-route to regenerate the files on the new machine) so try not to switch machines unless you have to.

```
  (on machine A)
  % git push origin master
  (on machine B)
  % git pull origin master
```

The resulting `$LABROOT` directory contains the following subdirectories: `src` contains your source Verilog; `build` contains makefiles and scripts that automate the process of building your design; and `build-unscripted` is a directory for you to use when invoking the VLSI tools manually. The `src` directory contains the a Verilog test harness and other Verilog modules you will be using in this lab assignment. Please read through these files and understand how the design works. We have supplied a Verilog solution for you. Figure 2 shows each directory that you have been provided and includes comments about what they do.

We have provided two Verilog designs: a "behavioral" version, and an "RTL" version. The behavioral design somewhat resembles C code. It only describes the behavior of a module, and is not

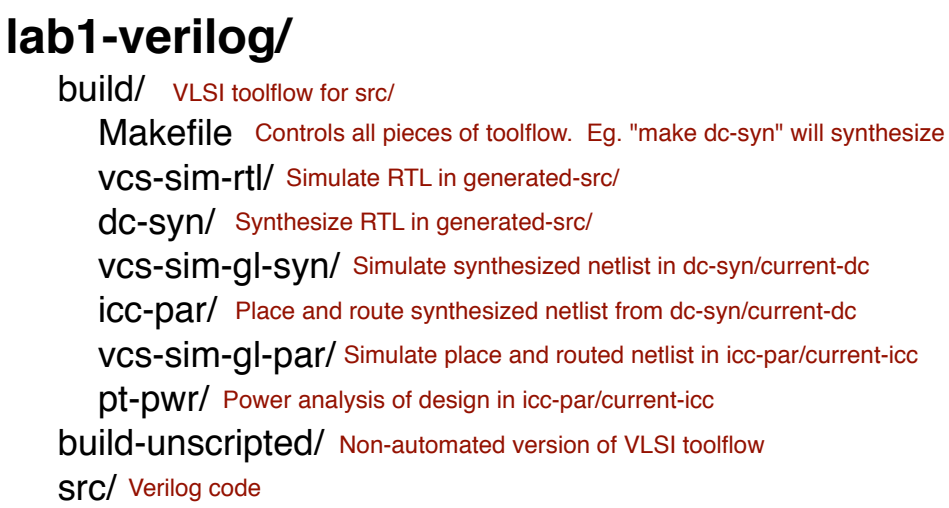

Figure 2: Directory organization for lab1-verilog/

intended to be synthesized into hardware. Testbenches are typically written in a behavioral style. The "RTL" design is a register transfer level (combinational logic and registers) description of the design. This RTL level description will be synthesized into a collection of logic gates and state elements, and eventually used to generate a complete ASIC layout.

Behavioral:

- `src/gcdGCDUnit_behav.v` - Behavioral implementation of gcdGCDUnit
- `src/gcdTestHarness_behav.v` - Test harness for the behavioral version

RTL:

- `src/gcdGCDUnit_rtl.v` - RTL implementation of gcdGCDUnit
- `src/gcdGCDUnitCtrl.v` - Control portion of the RTL implementation
- `src/gcdGCDUnitDpath.v` - Datapath portion of the RTL implementation
- `src/gcdTestHarness_rtl.v` - Test harness for the RTL version

A block diagram of the design is shown in Figure 3. The top level module is named `gcdGCDUnit` and has the interface shown in Figure 4. We have provided you with a test harness that will drive the inputs and verify the outputs of your design.

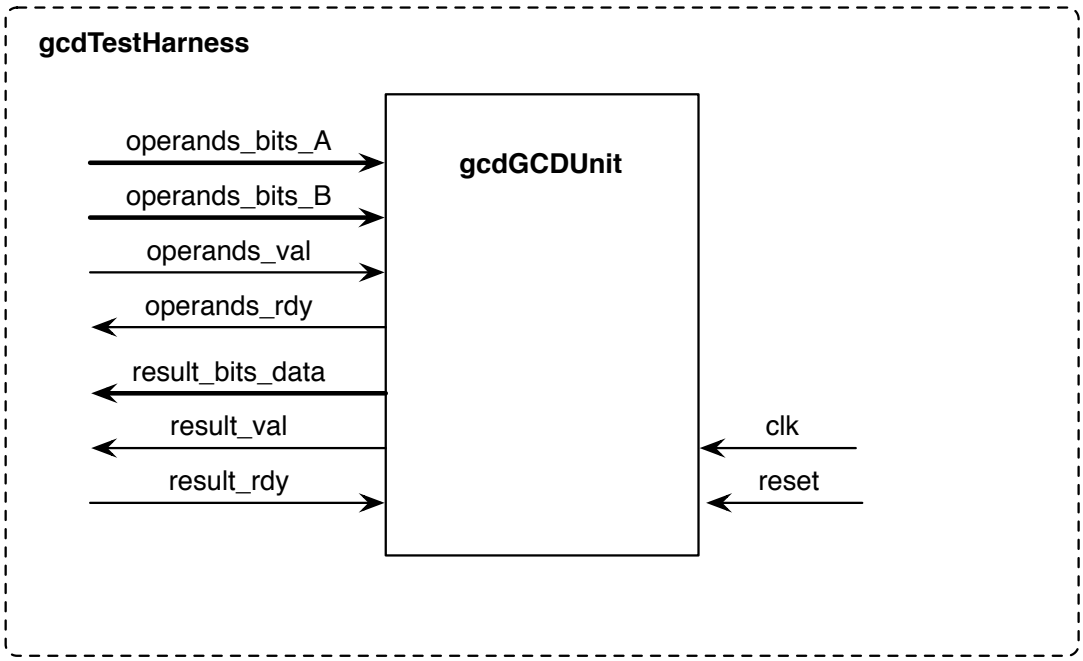

Figure 3: Block diagram for GCD Test Harness

```
module gcdGCDUnit#( parameter W = 16 )
(

  input clk, reset,

  input  [W-1:0] operands_bits_A,   // Operand A
  input  [W-1:0] operands_bits_B,   // Operand B
  input          operands_val,      // Are operands valid?
  output         operands_rdy,      // ready to take operands

  output [W-1:0] result_bits_data,  // GCD
  output         result_val,        // Is the result valid?
  input          result_rdy         // ready to take the result

);
```

Figure 4: Interface for the GCD module

The `build` and `build-unscripted` directory contain the following subdirectories which you will use when building your chip. The order in which they are listed is the order in which they occur in the toolflow.

- `vcs-sim-behav` - Behavioral simulation using Synopsys VCS
- `vcs-sim-rtl` - RTL simulation using Synopsys VCS
- `dc-syn` - Synthesis using Synopsys Design Compiler
- `vcs-sim-gl-syn` - Post synthesis gate-level simulation using Synopsys VCS

- `icc-par` - Automatic placement and routing using Synopsys IC Compiler
- `vcs-sim-gl-par` - Post place and route gate-level simulation using Synopsys VCS
- `pt-pwr` - Power analysis using Synopsys PrimeTime PX

Each subdirectory contains a Makefile and some contain script files as well. Running the "make" command in a subdirectory will launch the corresponding tool. For example, to perform synthesis using Design Compiler (DC):

```
% cd $LABROOT/build
% cd dc-syn
% make
```

Note: you must follow the ordering given in the list above.

Once you have verified that each of the steps in the flow succeeds, you can use the toplevel Makefile in the `build` directory to perform multiple of the steps in the flow in sequence. For example, once all the design files and scripts are set up properly, you should be able to use the following command to synthesize, floorplan, and place and route your design. You specify the name of the latest step in the flow you would like to run, and the Makefile ensures that every step preceding that one is performed first.

```
% cd $LABROOT/build
% make icc-par
```

Pushing a design through all the VLSI Tools

First, you will invoke several of the tools manually and enter commands interactively, before learning how to automate the process with scripts. You will perform the manual build in the `build-unscripted` directory, and the automated build using makefiles and scripts in the `build` directory.

Synopsys VCS: Simulating your Verilog

VCS compiles Verilog source files into a native binary that implements a simulation of the Verilog design. VCS can simulate both behavioral and RTL level Verilog modules. In behavioral models, a module's functionality can be described more easily by using higher levels of abstraction. In an RTL level model, a module's functionality is described at a level that can be mapped to a collection of registers and gates. Verilog behavioral models may not be synthesizable, however they can be useful in constructing testbenches and when simulating external devices that your design interfaces with. The test harness we have provided for this lab is a good example of how behavioral Verilog can be used. You will start by simulating the GCD module implemented in a behavioral style.

```
% cd $LABROOT/build-unscripted/vcs-sim-behav
% vcs -full64 -PP +lint=all +v2k -timescale=1ns/10ps \
  ../../src/gcdGCDUnit_behav.v \
  ../../src/gcdTestHarness_behav.v
```

By default, VCS produces a simulator binary called `simv`. The `-PP` command line option turns on support for using the `VPD` trace output format. The `+lint=all` argument turns on all Verilog warnings. Since it is quite easy to write legal Verilog code that doesn't behave as intended, you should always enable all warnings to help you catch mistakes. For example, VCS will warn you if you try to connect two nets with different bitwidths or don't wire up a port on a module. Always try to eliminate all VCS compilation errors *and* warnings. The `+v2k` command line option tells VCS to enable Verilog-2001 language features. Verilog allows a designer to specify how the abstract delay units in their design map into real time units using the `` `timescale `` compiler directive. To make it easy to change this parameter you will specify it on the command line instead of in the Verilog source. After these arguments you list the Verilog source files. The `-v` flag is used to indicate which Verilog files are part of a library (and thus should only be compiled if needed) and which files are part of the actual design (and thus should always be compiled). After running this command, you should see text output indicating that VCS is parsing the Verilog files and compiling the modules. Notice that VCS actually generates C++ code which is then compiled using `gcc`. When VCS is finished there should be a `simv` executable in the build directory. Now try running it:

```
% ./simv
...
 Entering Test Suite: exGCD_behav
  [ passed ] Test ( gcd(27,15) ) succeeded, [ 0003 == 00000003 ]
  [ passed ] Test ( gcd(21,49) ) succeeded, [ 0007 == 00000007 ]
  [ passed ] Test ( gcd(25,30) ) succeeded, [ 0005 == 00000005 ]
  [ passed ] Test ( gcd(19,27) ) succeeded, [ 0001 == 00000001 ]
  [ passed ] Test ( gcd(40,40) ) succeeded, [ 0028 == 00000028 ]
  [ passed ] Test ( gcd(250,190) ) succeeded, [ 000a == 0000000a ]
  [ passed ] Test ( gcd(0,0) ) succeeded, [ 0000 == 00000000 ]
...
```

Typing in all the Verilog source files on the command line can be very tedious, so we will use Makefiles to automate the process of compiling our simulator binaries.

```
% cd $LABROOT/build/vcs-sim-behav
% cat Makefile
...
vsrcs = \
        $(srcdir)/gcdGCDUnit_behav.v \
        $(srcdir)/gcdTestHarness_behav.v \
...
% make
% make run
```

You can leverage the same makefile to build the simulator for the RTL level Verilog version of the design.

```
% cd $LABROOT/build/vcs-sim-rtl
% cat Makefile
...
vsrcs = \
        $(srcdir)/gcdGCDUnitCtrl.v \
```

```
        $(srcdir)/gcdGCDUnitDpath.v \
        $(srcdir)/gcdGCDUnit_rtl.v \
        $(srcdir)/gcdTestHarness_rtl.v \
...
% make
% make run
./simv +verbose=1
...
  + Running Test Case: gcdGCDUnit_rtl
     [ passed ] Test ( vcTestSink ) succeeded, [ 0003 == 0003 ]
     [ passed ] Test ( vcTestSink ) succeeded, [ 0007 == 0007 ]
     [ passed ] Test ( vcTestSink ) succeeded, [ 0005 == 0005 ]
     [ passed ] Test ( vcTestSink ) succeeded, [ 0001 == 0001 ]
     [ passed ] Test ( vcTestSink ) succeeded, [ 0028 == 0028 ]
     [ passed ] Test ( vcTestSink ) succeeded, [ 000a == 000a ]
     [ passed ] Test ( vcTestSink ) succeeded, [ 0005 == 0005 ]
     [ passed ] Test ( vcTestSink ) succeeded, [ 0000 == 0000 ]
     [ passed ] Test ( Is sink finished? ) succeeded
...
```

Where should you start if a design doesn't pass all your tests? The answer is to debug your RTL code using the Discovery Visualization Environment (DVE) GUI to generate a waveform view of signals in your design. The simulator already has already written a trace of the activity of every net in your design to the `vcdplus.vpd` file. DVE can read the `vcdplus.vpd` file and visualize the wave form.

```
% ls
csrc  Makefile  simv  simv.daidir  timestamp  vcdplus.vpd
% dve -full64 -vpd vcdplus.vpd &
```

To add signals to the waveform window (see Figure 5) you can select them in the hierarchy window and then right click to choose *Add To Waves > New Wave View*.

Synopsys Design Compiler: RTL to Gate-Level Netlist

Design Compiler performs hardware synthesis. A synthesis tool takes an RTL hardware description and a standard cell library as input and produces a gate-level netlist as an output. The resulting gate-level netlist is a completely structural description of the design, with only standard cells (and later on, possibly SRAM macros) as leaves in the design hierarchy. To cut and past commands from this lab into your Design Compiler shell and make sure Design Compiler ignores the `dc_shell-topo>` string, we will use an alias to "undefine" the `dc_shell-topo>` string.

```
% cd $LABROOT/build-unscripted/dc-syn
% dc_shell-xg-t -64bit -topographical_mode
...
Initializing...
alias "dc_shell-topo>" ""
```

You will now execute some commands to setup your environment.

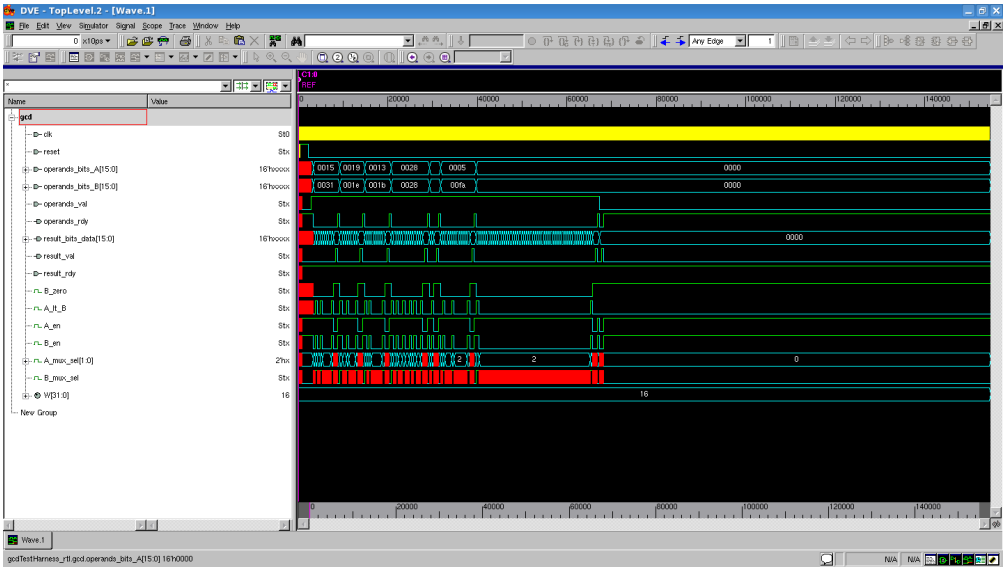

Figure 5: DVE Waveform Window

```
dc_shell-topo> set ucb_vlsi_home [getenv UCB_VLSI_HOME]
dc_shell-topo> set stdcells_home \
  $ucb_vlsi_home/stdcells/synopsys-90nm/default
dc_shell-topo> set_app_var search_path \
  "$stdcells_home/db $ucb_vlsi_home/install/vclib ../../src"
dc_shell-topo> set_app_var target_library "cells.db"
dc_shell-topo> set_app_var synthetic_library "dw_foundation.sldb"
dc_shell-topo> set_app_var link_library "* $target_library $synthetic_library"
dc_shell-topo> set_app_var alib_library_analysis_path "$stdcells_home/alib"
dc_shell-topo> set_app_var mw_logic1_net "VDD"
dc_shell-topo> set_app_var mw_logic0_net "VSS"
dc_shell-topo> create_mw_lib -technology $stdcells_home/techfile/techfile.tf \
  -mw_reference_library $stdcells_home/mw/cells.mw "gcdGCDUnit_rtl_LIB"
dc_shell-topo> open_mw_lib "gcdGCDUnit_rtl_LIB"
dc_shell-topo> check_library
dc_shell-topo> set_tlu_plus_file \
  -max_tluplus $stdcells_home/tluplus/max.tluplus \
  -min_tluplus $stdcells_home/tluplus/min.tluplus \
  -tech2itf_map $stdcells_home/techfile/tech2itf.map
dc_shell-topo> check_tlu_plus_files
dc_shell-topo> define_design_lib WORK -path "./work"
dc_shell-topo> set_svf "gcdGCDUnit_rtl.svf"
```

These commands point to your Verilog source directory, create a Synopsys work directory, and point to the standard libraries you will be using for the class. The `set_svf` command is used to set up a guidance file which is used by Synopsys Formality. Now you can load your Verilog design in to Design Compiler with the `analyze`, `elaborate`, `link`, and `check_design` commands.

```
dc_shell-topo> analyze -format verilog \
```

```
    "gcdGCDUnitCtrl.v gcdGCDUnitDpath.v gcdGCDUnit_rtl.v"
  dc_shell-topo> elaborate "gcdGCDUnit_rtl"
  dc_shell-topo> link
  dc_shell-topo> check_design
```

Before you can synthesize your design, you must specify some constraints; most importantly you must tell the tool your target clock period. The following command tells the Design Compiler that the pin named `clk` is the clock and that your target clock period is 1 nanosecond.

```
  dc_shell-topo> create_clock clk -name ideal_clock1 -period 1
```

Now you are ready to use the `compile_ultra` command to actually synthesize your design into a gate-level netlist. `-no_autoungroup` is specified in order to preserve the hierarchy during syntehsis.

```
 dc_shell-topo> compile_ultra -gate_clock -no_autoungroup
  ...
  Beginning Delay Optimization
  ----------------------------
    0:00:04    3113.2      0.02       0.1       0.0
    0:00:04    3142.7      0.00       0.0       0.0
    0:00:04    3142.7      0.00       0.0       0.0
    0:00:04    3222.8      0.00       0.0       0.0
    0:00:04    3222.8      0.00       0.0       0.0
    0:00:04    3222.8      0.00       0.0       0.0
    0:00:04    3222.8      0.00       0.0       0.0
    0:00:04    3222.8      0.00       0.0       0.0
    0:00:04    3222.8      0.00       0.0       0.0
    0:00:04    3222.8      0.00       0.0       0.0
  ...
```

The `compile_ultra` command will report how the design is being optimized. You should see Design Compiler performing technology mapping, delay optimization, and area reduction. The fragment from the `compile_ultra` shows the worst negative slack which indicates how much room there is between the critical path in your design and your specified clock constraint. Larger negative slack values are worse since this means that your design is missing the desired clock frequency by a great amount. Total negative slack is the sum of all negative slack summed over all the endpoints (register inputs or top level input/output ports) in the design.

Now you can generate the guidance information required by the formal verification tool, and produce the synthesized gate-level netlist and derived constraints files.

```
  dc_shell-topo> set_svf -off
  dc_shell-topo> change_names -rules verilog -hierarchy
  dc_shell-topo> write -format ddc -hierarchy -output gcdGCDUnit_rtl.mapped.ddc
  dc_shell-topo> write -f verilog -hierarchy -output gcdGCDUnit_rtl.mapped.v
  dc_shell-topo> write_sdf gcdGCDUnit_rtl.mapped.sdf
  dc_shell-topo> write_sdc -nosplit gcdGCDUnit_rtl.mapped.sdc
  dc_shell-topo> write_milkyway -overwrite -output "gcdGCDUnit_rtl_DCT"
  dc_shell-topo> source ./find_regs.tcl
  dc_shell-topo> find_regs gcdTestHarness_rtl/gcd
```

Take a look at various reports describing the synthesis results.

```
dc_shell-topo> report_timing -transition_time -nets -attributes -nosplit
...
Point                                          Fanout     Trans   Incr   Path
---------------------------------------------------------------------------
clock ideal_clock1 (rise edge)                                    0.00   0.00
clock network delay (ideal)                                       0.00   0.00
dpath/A_reg_reg_1_/CLK (DFFX1)                              0.00  0.00   0.00 r
dpath/A_reg_reg_1_/Q (DFFX1)                                0.05  0.19   0.19 f
dpath/out[1] (net)                             5                  0.00   0.19 f
dpath/U94/QN (NAND2X1)                                      0.05  0.03   0.22 r
dpath/n21 (net)                                1                  0.00   0.22 r
...
dpath/U60/QN (NAND2X1)                                      0.06  0.04   0.53 f
dpath/n97 (net)                                1                  0.00   0.53 f
dpath/U62/ZN (INVX2)                                        0.04  0.03   0.56 r
dpath/is_A_lt_B (net)                          3                  0.00   0.56 r
dpath/is_A_lt_B (gcdGCDUnitDpath_W16)                             0.00   0.56 r
is_A_lt_B (net)                                                   0.00   0.56 r
ctrl/is_A_lt_B (gcdGCDUnitCtrl)                                   0.00   0.56 r
ctrl/is_A_lt_B (net)                                              0.00   0.56 r
ctrl/U6/ZN (INVX2)                                          0.03  0.02   0.59 f
ctrl/n1 (net)                                  1                  0.00   0.59 f
...
ctrl/U5/QN (NAND2X1)                                        0.05  0.02   0.78 r
ctrl/en_A (net)                                1                  0.00   0.78 r
ctrl/en_A (gcdGCDUnitCtrl)                                        0.00   0.78 r
en_A (net)                                                        0.00   0.78 r
dpath/en_A (gcdGCDUnitDpath_W16)                                  0.00   0.78 r
dpath/en_A (net)                                                  0.00   0.78 r
dpath/clk_gate_A_reg_reg/EN (SNPS_CLOCK_GATE_HIGH..)              0.00   0.78 r
dpath/clk_gate_A_reg_reg/EN (net)                                 0.00   0.78 r
dpath/clk_gate_A_reg_reg/latch/D (LATCHX1)                  0.05  0.00   0.78 r
data arrival time                                                        0.78

clock ideal_clock1' (rise edge)                                   0.50   0.50
clock network delay (ideal)                                       0.00   0.50
dpath/clk_gate_A_reg_reg/latch/CLK (LATCHX1)                      0.00   0.50 r
time borrowed from endpoint                                       0.28   0.78
data required time                                                       0.78
---------------------------------------------------------------------------
data required time                                                       0.78
data arrival time                                                        0.78
---------------------------------------------------------------------------
slack (MET)                                                              0.00
...
```

This report shows the *critical path* of the design. The critical path has the longest propagation delay between any two registers in the design and therefore sets an upper bound on the design's operating frequency. In this report, we see that the critical path begins at the output of bit 1 of the operand A register in the datapath; goes through the comparator; into the control logic; and finally ends at the clock gate latch controlling the operand A register in the datapath. The critical path takes a total of 0.78ns which is less than the 1ns clock period constraint.

```
dc_shell-topo> report_area -nosplit -hierarchy
...
                          Global cell area          Local cell area
                          ------------------  ----------------------------
Hierarchical cell         Absolute   Percent  Combi-     Noncombi-  Black
                          Total      Total    national   national   boxes
------------------------  ---------  -------  ---------  ---------  ------
gcdGCDUnit_rtl            2869.8560    100.0     0.0000     0.0000  0.0000
ctrl                       193.5360      6.7   143.7696    49.7664  0.0000
dpath                     2676.3206     93.3  1810.0188   796.2622  0.0000
dpath/clk_gate_A_reg_reg    35.0208      1.2    12.9024    22.1184  0.0000
dpath/clk_gate_B_reg_reg    35.0208      1.2    12.9024    22.1184  0.0000
------------------------  ---------  -------  ---------  ---------  ------
Total                                         1979.5931   890.2654  0.0000
...
```

This report tells you about the post synthesis area results. The units are um^2. You can see that the datapath accounts for 93.3% of the total chip area.

```
dc_shell-topo> report_power -nosplit -hier
...
--------------------------------------------------------------------------------
                                  Switch   Int      Leak     Total
Hierarchy                         Power    Power    Power    Power    %
--------------------------------------------------------------------------------
gcdGCDUnit_rtl                     380.908  689.568 1.39e+07 1.08e+03 100.0
  dpath (gcdGCDUnitDpath_W16)      361.460  673.192 1.30e+07 1.05e+03  96.6
  ctrl (gcdGCDUnitCtrl)             19.448   16.376 8.80e+05   36.704   3.4
...
```

This report contains post synthesis power estimates. The dynamic power units are uW while the leakage power units are pW.

```
dc_shell-topo> report_reference -nosplit -hierarchy
...
****************************************
Design: gcdGCDUnitDpath_W16
****************************************
Reference          Library       Unit Area   Count    Total Area   Attributes
--------------------------------------------------------------------------------
AND2X1             saed90nm_typ     7.372800       1     7.372800
AO21X1             saed90nm_typ    10.137600       1    10.137600
```

```
AO222X1             saed90nm_typ    14.745600      13   191.692797
AOI21X1             saed90nm_typ    11.980800       4    47.923199
AOI22X1             saed90nm_typ    12.902400       3    38.707200
DFFX1               saed90nm_typ    24.883200      32   796.262390 n
INVX0               saed90nm_typ     5.529600      28   154.828804
INVX2               saed90nm_typ     6.451200       1     6.451200
MUX21X1             saed90nm_typ    11.059200      16   176.947205
NAND2X0             saed90nm_typ     5.529600       7    38.707201
NAND2X1             saed90nm_typ     5.529600      67   370.483210
NAND3X0             saed90nm_typ     7.372800       2    14.745600
NAND4X0             saed90nm_typ     8.294400       3    24.883201
NOR2X0              saed90nm_typ     5.529600      31   171.417604
NOR2X2              saed90nm_typ     9.216000       4    36.863998
NOR3X0              saed90nm_typ     8.294400       2    16.588800
NOR4X0              saed90nm_typ     9.216000       5    46.079998
OA22X1              saed90nm_typ    11.059200       5    55.296001
OAI21X1             saed90nm_typ    11.059200      13   143.769604
OR2X1               saed90nm_typ     7.372800       3    22.118400
SNPS_CLOCK_GATE..                   35.020801       1    35.020801 h, n
SNPS_CLOCK_GATE..                   35.020801       1    35.020801 h, n
XNOR2X1             saed90nm_typ    13.824000       8   110.592003
XOR2X1              saed90nm_typ    13.824000       9   124.416003
------------------------------------------------------------------------
Total 24 references                                    2676.326418
...
```

This report lists the standard cells used to implement each module. The `gcdGCDUnitDpath` module consists of 32 `DFFX1` cells, 67 `NAND2X1` cells, and so on. The total area consumed by each type of cell is also reported.

```
dc_shell-topo> report_resources -nosplit -hierarchy
...
Resource Report for this hierarchy in file ../../src/gcdGCDUnitDpath.v
===============================================================================
| Cell           | Module         | Parameters | Contained Operations       |
===============================================================================
| sub_x_28_1     | DW01_sub       | width=16   | sub_28                     |
| lt_x_46_1      | DW_cmp         | width=16   | lt_46                      |
===============================================================================

Implementation Report
===============================================================================
|                    |                  | Current            | Set            |
| Cell               | Module           | Implementation     | Implementation |
===============================================================================
| sub_x_28_1         | DW01_sub         | pparch (area,speed)                 |
| lt_x_46_1          | DW_cmp           | apparch (area)     |                |
===============================================================================
```

```
...
```

Synopsys provides a library of commonly used arithmetic components as highly optimized building blocks. This library is called Design Ware and Design Compiler will automatically use Design Ware components when it can. This report can help you determine when Design Compiler is using Design Ware components. The `DW01_sub` in the module name indicates that this is a Design Ware subtractor. This report also gives you what type of architecutre it used.

You can use makefiles and scripts to help automate the process of synthesizing your design.

```
% cd $LABROOT/build/dc-syn
% cat Makefile
...
vsrcs = \
        $(srcdir)/gcdGCDUnitCtrl.v \
        $(srcdir)/gcdGCDUnitDpath.v \
        $(srcdir)/gcdGCDUnit_rtl.v \
...
% make
```

Go ahead and take a look what the automated build system produced.

```
% cd $LABROOT/build/dc-syn
% ls -l
-rw-r--r-- 1 yunsup grad 4555 Aug 29 22:15 Makefile
drwxr-xr-x 7 yunsup grad 4096 Aug 29 22:15 build-dc-2010-08-29_22-15
-rw-r--r-- 1 yunsup grad 1108 Aug 28 12:06 constraints.tcl
lrwxrwxrwx 1 yunsup grad   25 Aug 29 22:15 current-dc -> build-dc-2010-08-29_22-15
drwxr-xr-x 2 yunsup grad 4096 Aug 29 21:39 rm_dc_scripts
drwxr-xr-x 2 yunsup grad 4096 Aug 28 12:00 rm_notes
drwxr-xr-x 2 yunsup grad 4096 Aug 29 21:50 rm_setup
% cd current-dc
% ls -l
drwxr-xr-x 2 yunsup grad   4096 Aug 29 22:15 WORK
-rw-r--r-- 1 yunsup grad     47 Aug 29 22:15 access.tab
-rw-r--r-- 1 yunsup grad 235827 Aug 29 22:15 command.log
-rw-r--r-- 1 yunsup grad   5141 Aug 29 22:15 common_setup.tcl
-rw-r--r-- 1 yunsup grad   1108 Aug 29 22:15 constraints.tcl
-rw-r--r-- 1 yunsup grad  18996 Aug 29 22:15 dc.tcl
-rw-r--r-- 1 yunsup grad   4621 Aug 29 22:15 dc_setup.tcl
-rw-r--r-- 1 yunsup grad   4625 Aug 29 22:15 dc_setup_filenames.tcl
-rw-r--r-- 1 yunsup grad   2730 Aug 29 22:15 find_regs.tcl
-rw-r--r-- 1 yunsup grad   4439 Aug 29 22:15 force_regs.ucli
drwxr-xr-x 3 yunsup grad   4096 Aug 29 22:15 gcdGCDUnit_rtl_LIB
drwxr-xr-x 2 yunsup grad   4096 Aug 29 22:15 log
-rw-r--r-- 1 yunsup grad   1087 Aug 29 22:15 make_generated_vars.tcl
drwxr-xr-x 2 yunsup grad   4096 Aug 29 22:15 reports
drwxr-xr-x 2 yunsup grad   4096 Aug 29 22:15 results
-rw-r--r-- 1 yunsup grad     29 Aug 29 22:15 timestamp
```

Notice that the Makefile does not overwrite build directories. It creates a new build directory every time your run make. This makes it easy to change your synthesis scripts or source Verilog, resynthesize your design, and compare your results to those from an earlier design. You can use symlinks to keep track of various build directories. Inside the `current-dc` directory, you can see all the tcl scripts as well as the directories named `results` and `reports`: `results` contains your synthesized gate-level netlist; and `reports` contains various post synthesis reports.

Synopsys provides a GUI front-end for Design Compiler called Design Vision which you will use to analyze the synthesis results. You should avoid using the GUI to actually perform synthesis since scripting the process is more efficient. Start Design Vision:

```
% cd $LABROOT/build/dc-syn/current-dc
% design_vision-xg -64bit
...
Initializing...
design_vision> alias "design_vision>" ""
design_vision> source dc_setup.tcl
design_vision> read_file -format ddc "results/gcdGCDUnit_rtl.mapped.ddc"
```

You can browse your design with the hierarchical view (see Figure 6). If you right click on a module and select the *Schematic View* option, the tool will display a schematic view of the standard cells used to implement that module.

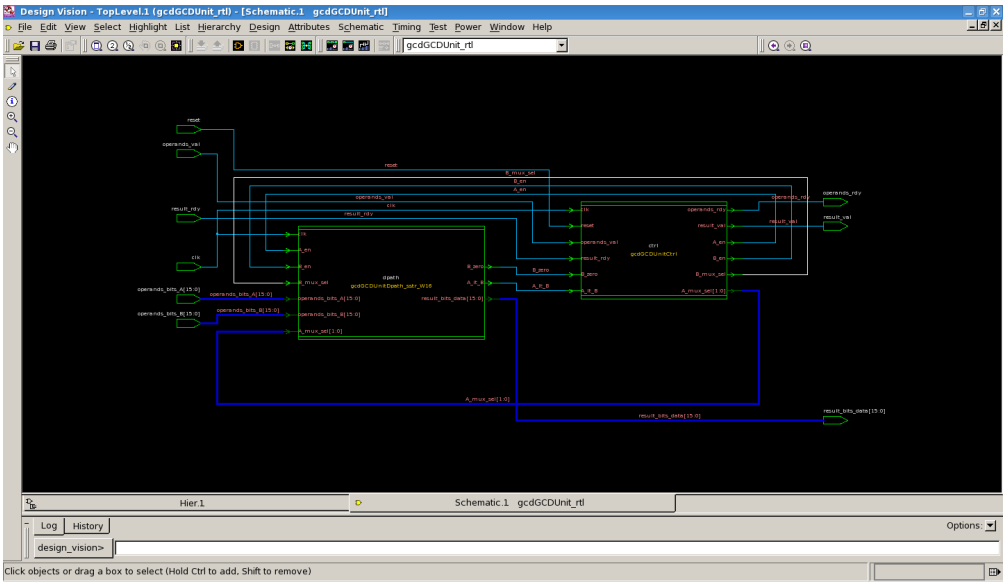

Figure 6: Design Vision Hierarchical View

Synopsys Formality: Formal Verification

Formality formally verifies whether or not the RTL and the synthesized gate-level netlist match.

```
% cd $LABROOT/build-unscripted/dc-syn
% fm_shell -64bit
```

```
...
fm_shell (setup)> alias "fm_shell" ""
fm_shell (setup)> alias "(setup)>" ""
fm_shell (setup)> alias "(match)>" ""
fm_shell (setup)> alias "(verify)>" ""
```

Execute some commands to setup your environment.

```
fm_shell (setup)> set ucb_vlsi_home [getenv UCB_VLSI_HOME]
fm_shell (setup)> set stdcells_home \
  $ucb_vlsi_home/stdcells/synopsys-90nm/default
fm_shell (setup)> set_app_var search_path \
  "$stdcells_home/db ~cs250/install/vclib ../../src"
fm_shell (setup)> set_app_var synopsys_auto_setup "true"
fm_shell (setup)> set_svf "gcdGCDUnit_rtl.svf"
fm_shell (setup)> read_db -technology_library "cells.db"
```

These commands point to your Verilog source directory, the svf file you generated during synthesis, and the standard libraries you will be using for the class. Now go ahead and open your original RTL design and the synthesized gate-level netlist in Formality.

```
fm_shell (setup)> read_verilog -r \
  "gcdGCDUnitCtrl.v gcdGCDUnitDpath.v gcdGCDUnit_rtl.v" \
  -work_library WORK
fm_shell (setup)> set_top r:/WORK/gcdGCDUnit_rtl
fm_shell (setup)> read_ddc -i "./gcdGCDUnit_rtl.mapped.ddc"
fm_shell (setup)> set_top i:/WORK/gcdGCDUnit_rtl
```

You are ready to begin verification to determine whether or not the two representations of the design match are equivalent.

```
fm_shell (setup)> match
fm_shell (match)> report_unmatched_points
fm_shell (match)> verify
...
************************ Verification Results ************************
Verification SUCCEEDED
   ATTENTION:  synopsys_auto_setup mode was enabled.
               See Synopsys Auto Setup Summary for details
-----------------------------------------------------------
 Reference design: r:/WORK/gcdGCDUnit_rtl
 Implementation design: i:/WORK/gcdGCDUnit_rtl
 52 Passing compare points
-------------------------------------------------------------------------
Matched Compare Points   BBPin  Loop BBNet   Cut  Port   DFF   LAT TOTAL
-------------------------------------------------------------------------
Passing (equivalent)         0     0     0     0    18    34     0    52
Failing (not equivalent)     0     0     0     0     0     0     0     0
*************************************************************************
...
```

We have provided you with Makefiles and scripts which automate this procedure.

```
% cd $LABROOT/build/dc-syn
% make fm
```

Synopsys VCS: Simulating Post Synthesis Gate-Level Netlist

After generating a synthesized gate-level netlist, you will verify that the netlist behaves as expected by running another simulation using VCS.

```
% cd $LABROOT/build-unscripted/dc-syn
% sdfcorrect.py gcdGCDUnit_rtl.mapped.sdf gcdGCDUnit_rtl.mapped.corrected.sdf
% cd $LABROOT/build-unscripted/vcs-sim-gl-syn
% vcs -full64 -PP +lint=all +v2k -timescale=1ns/10ps \
  -P ../dc-syn/access.tab -debug \
  +neg_tchk +sdfverbose \
  -sdf typ:gcdGCDUnit_rtl:../dc-syn/gcdGCDUnit_rtl.mapped.corrected.sdf \
  +incdir+$UCB_VLSI_HOME/install/vclib \
  -v $UCB_VLSI_HOME/install/vclib/vcQueues.v \
  -v $UCB_VLSI_HOME/install/vclib/vcStateElements.v \
  -v $UCB_VLSI_HOME/install/vclib/vcTest.v \
  -v $UCB_VLSI_HOME/install/vclib/vcTestSource.v \
  -v $UCB_VLSI_HOME/install/vclib/vcTestSink.v \
  $UCB_VLSI_HOME/stdcells/synopsys-90nm/default/verilog/cells.v \
  ../dc-syn/gcdGCDUnit_rtl.mapped.v \
  ../../src/gcdTestHarness_rtl.v \
  +define+CLOCK_PERIOD=0.5
% ./simv -ucli +verbose=1
ucli% source ../dc-syn/force_regs.ucli
ucli% run
...
  + Running Test Case: gcdGCDUnit_rtl
     [ passed ] Test ( vcTestSink ) succeeded, [ 0003 == 0003 ]
     [ passed ] Test ( vcTestSink ) succeeded, [ 0007 == 0007 ]
     [ passed ] Test ( vcTestSink ) succeeded, [ 0005 == 0005 ]
     [ passed ] Test ( vcTestSink ) succeeded, [ 0001 == 0001 ]
     [ passed ] Test ( vcTestSink ) succeeded, [ 0028 == 0028 ]
     [ passed ] Test ( vcTestSink ) succeeded, [ 000a == 000a ]
     [ passed ] Test ( vcTestSink ) succeeded, [ 0005 == 0005 ]
     [ passed ] Test ( vcTestSink ) succeeded, [ 0000 == 0000 ]
     [ passed ] Test ( Is sink finished? ) succeeded
...
```

Makefiles are provided which build the simulator and execute the testbench.

```
% cd $LABROOT/build/vcs-sim-gl-syn
% make
% make run
```

Synopsys IC Compiler: Gate-Level Netlist to Layout

IC Compiler performs placement and routing of the standard cells in your design. It takes a gate-level netlist, standard cell library, floorplan information, and technology files describing the metal layers available for routing as input and produces a layout as an output. After this step, you can visually inspect the standard cells and routes on the metal layers. For this step, you will use IC Compiler in an interactive fashion, so go ahead and launch it with its GUI enabled.

```
% cd $LABROOT/build-unscripted/icc-par
% icc_shell -64bit -gui
...
Initializing...
icc_shell> alias "icc_shell>" ""
```

Execute the following commands to setup your environment:

```
icc_shell> set ucb_vlsi_home [getenv UCB_VLSI_HOME]
icc_shell> set stdcells_home \
  $ucb_vlsi_home/stdcells/synopsys-90nm/default
icc_shell> set_app_var search_path "$stdcells_home/db"
icc_shell> set_app_var target_library "cells.db"
icc_shell> set_app_var link_library "* $target_library"
```

These commands point the tool to the standard libraries you will be using in this class. Before you jump into place and route, you will create a Milkyway database in which to store your placed and routed design. Observe that when you create the Milkyway database you specify the technology file which describes the design rules of the target process (e.g., detailed information about allowed thicknesses and spacings on the poly and metal layers), and the Milkyway reference database which contains the layouts of the standard cells. Next, load your synthesized gate-level netlist from the `dc-syn` directory. You must also specify the TLU+ files which include information necessary to perform parasitic extraction for calculating wire delays. You also need to create power and ground ports.

```
icc_shell> create_mw_lib \
  -tech "$stdcells_home/techfile/techfile.tf" \
  -bus_naming_style {[%d]} \
  -mw_reference_library "$stdcells_home/mw/cells.mw" \
  "gcdGCDUnit_rtl_LIB"
icc_shell> open_mw_lib gcdGCDUnit_rtl_LIB
icc_shell> import_designs "../dc-syn/gcdGCDUnit_rtl.mapped.ddc" \
  -format "ddc" -top "gcdGCDUnit_rtl" -cel "gcdGCDUnit_rtl"
icc_shell> set_tlu_plus_files \
  -max_tluplus "$stdcells_home/tluplus/max.tluplus" \
  -min_tluplus "$stdcells_home/tluplus/min.tluplus" \
  -tech2itf_map "$stdcells_home/techfile/tech2itf.map"
icc_shell> derive_pg_connection \
  -power_net "VDD" -power_pin "VDD" -ground_net "VSS" -ground_pin "VSS" \
  -create_ports "top"
```

Make an initial floorplan and synthesize power rails. At this point, you can see a visualization of the estimated voltage drops on the power rails (Figure 7). The numbers on the right are specified in mW.

```
icc_shell> initialize_floorplan \
  -control_type "aspect_ratio" -core_aspect_ratio "1" \
  -core_utilization "0.7" -row_core_ratio "1" \
  -left_io2core "30" -bottom_io2core "30" -right_io2core "30" -top_io2core "30" \
  -start_first_row
icc_shell> create_fp_placement
icc_shell> synthesize_fp_rail \
  -power_budget "1000" -voltage_supply "1.2" -target_voltage_drop "250" \
  -output_dir "./pna_output" -nets "VDD VSS" -create_virtual_rails "M1" \
  -synthesize_power_plan -synthesize_power_pads -use_strap_ends_as_pads
```

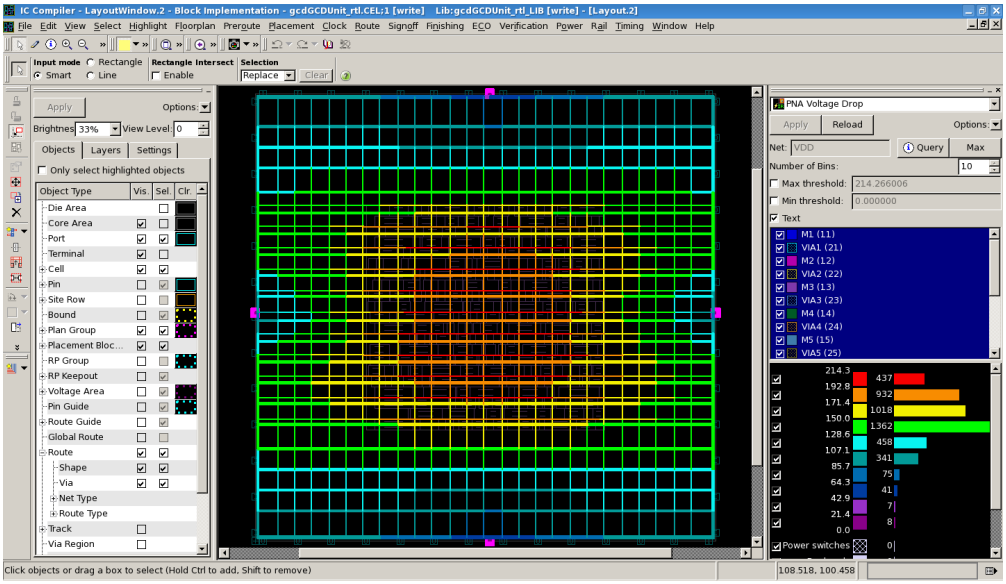

Figure 7: Estimated voltage drops shown in IC Compiler

If you have met your power budget, go ahead and commit the power plan.

```
icc_shell> commit_fp_rail
```

You will now perform clock tree synthesis. Because the clock is one of the most critical and highest fan-out nets in the design, it must be routed first. The tool will analyze the clock net and insert buffers to minimize clock skew before performing routing.

```
icc_shell> clock_opt -only_cts -no_clock_route
icc_shell> route_zrt_group -all_clock_nets -reuse_existing_global_route true
```

Take a look at the generated clock tree. Choose *Clock > Color By Clock Trees*. Hit *Reload*, and then hit *OK* on the popup window. Now you will be able to see the synthesized clock tree (Figure 8).

Go ahead and route the remaining nets.

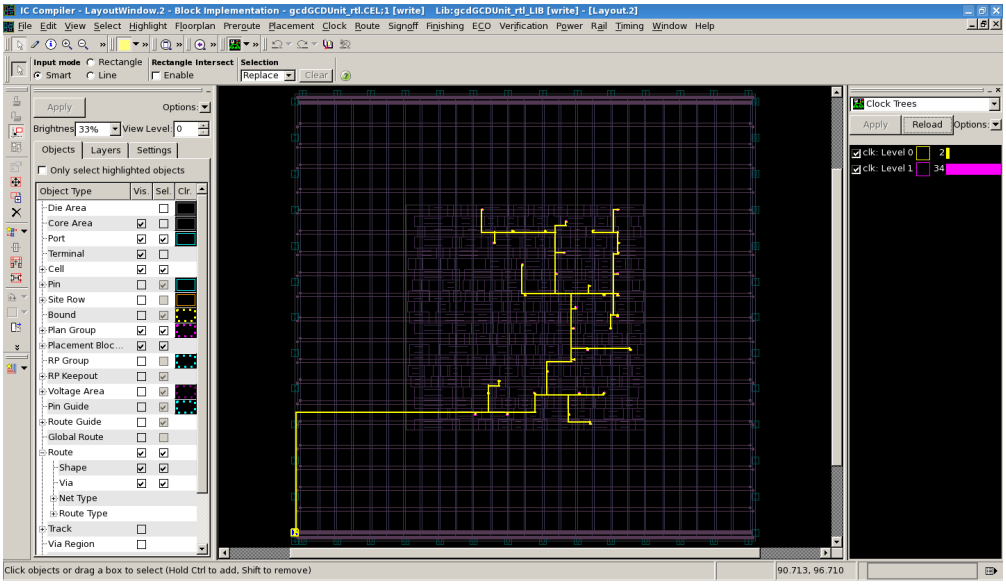

Figure 8: Synthesized clock tree shown in IC Compiler

```
icc_shell> route_opt -initial_route_only
icc_shell> route_opt -skip_initial_route -effort low
```

Figure 9 shows the routed signals. The Synopsys 90nm process provides nine metal layers (metal 1 is mostly used by the standard cell layout itself) for routing your signals.

Notice that there are various gaps in the placement. You will add *filler* cells to fill up these spaces. Filler cells are just empty standard cells which connect the power and ground rails. Notice that you need to rerun routing due to some Design Rule Check (DRC) errors.

```
icc_shell> insert_stdcell_filler \
  -cell_with_metal "SHFILL1 SHFILL2 SHFILL3" \
  -connect_to_power "VDD" -connect_to_ground "VSS"
icc_shell> route_opt -incremental -size_only
```

Congratulations! Now you have your design mapped onto silicon. Go ahead and generate the post place and route netlist and the constraint file. You also need to generate parasitics files necessary to estimate the power consumption of your design.

```
icc_shell> change_names -rules verilog -hierarchy
icc_shell> write_verilog "gcdGCDUnit_rtl.output.v"
icc_shell> write_sdf "gcdGCDUnit_rtl.output.sdf"
icc_shell> write_sdc "gcdGCDUnit_rtl.output.sdc"
icc_shell> extract_rc -coupling_cap
icc_shell> write_parasitics -format SBPF -output "gcdGCDUnit_rtl.output.sbpf"
icc_shell> source ./find_regs.tcl
icc_shell> find_regs gcdTestHarness_rtl/gcd
icc_shell> save_mw_cel
icc_shell> close_mw_cel
```

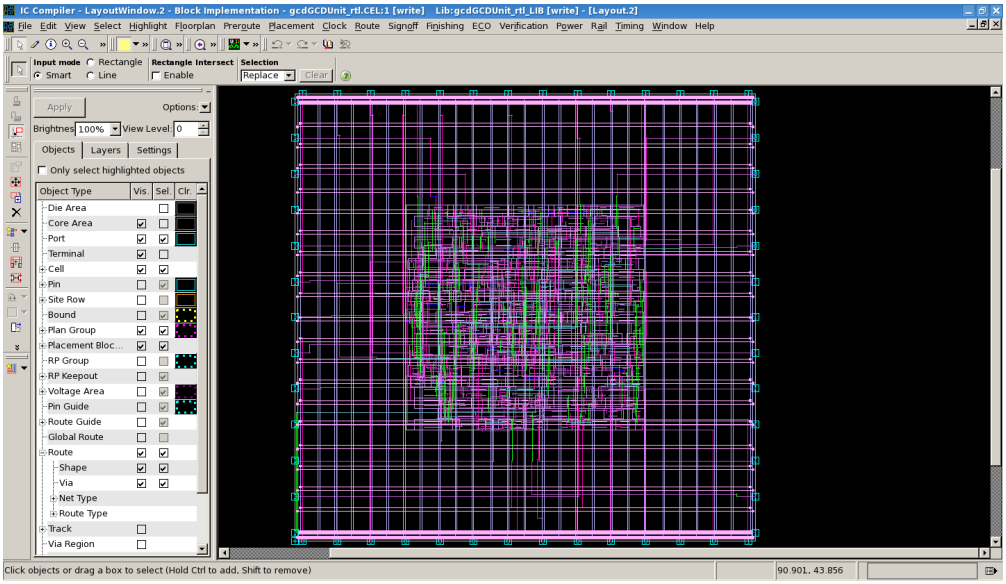

Figure 9: Routed signals shown in IC Compiler

This process can be automated using Makefiles. Notice that the Makefile creates new build directories like the one in Design Compiler.

```
% cd $LABROOT/build/icc-par
% make
% ls -l
-rw-r--r-- 1 yunsup grad 15232 Aug 28 18:40 Makefile
drwxr-xr-x 6 yunsup grad  4096 Aug 29 23:42 build-icc-2010-08-29_23-41
drwxr-xr-x 8 yunsup grad  4096 Aug 29 23:41 build-iccdp-2010-08-29_23-41
lrwxrwxrwx 1 yunsup grad    26 Aug 29 23:41 current-icc -> build-icc-2010-08-29_23-41
lrwxrwxrwx 1 yunsup grad    28 Aug 29 23:41 current-iccdp -> build-iccdp-2010-08-29_23-41
drwxr-xr-x 2 yunsup grad  4096 Aug 29 23:19 rm_icc_dp_scripts
drwxr-xr-x 2 yunsup grad  4096 Aug 29 23:29 rm_icc_scripts
drwxr-xr-x 2 yunsup grad  4096 Aug 29 23:38 rm_icc_zrt_scripts
drwxr-xr-x 2 yunsup grad  4096 Aug 28 16:20 rm_notes
drwxr-xr-x 2 yunsup grad  4096 Aug 29 23:34 rm_setup
```

Synopsys VCS: Simulating Post Place and Route Gate-Level Netlist

After you obtain the post place and route gate-level netlist, you will double-check the netlist by running a simulation using VCS. You also need to produce switching activity information in several formats for power estimation. Use `vpd2vcd` and `vcd2saif` to convert a `vpd` file into a `vcd` and an `saif` file.

```
% cd $LABROOT/build-unscripted/icc-par
% sdfcorrect.py gcdGCDUnit_rtl.output.sdf gcdGCDUnit_rtl.output.corrected.sdf
% cd $LABROOT/build-unscripted/vcs-sim-gl-par
% vcs -full64 -PP +lint=all +v2k -timescale=1ns/10ps \
```

```
  -P ../icc-par/access.tab -debug \
  +neg_tchk +sdfverbose \
  -sdf typ:gcdGCDUnit_rtl:../icc-par/gcdGCDUnit_rtl.output.corrected.sdf \
  +incdir+$UCB_VLSI_HOME/install/vclib \
  -v $UCB_VLSI_HOME/install/vclib/vcQueues.v \
  -v $UCB_VLSI_HOME/install/vclib/vcStateElements.v \
  -v $UCB_VLSI_HOME/install/vclib/vcTest.v \
  -v $UCB_VLSI_HOME/install/vclib/vcTestSource.v \
  -v $UCB_VLSI_HOME/install/vclib/vcTestSink.v \
  $UCB_VLSI_HOME/stdcells/synopsys-90nm/default/verilog/cells.v \
  ../icc-par/gcdGCDUnit_rtl.output.v \
  ../../src/gcdTestHarness_rtl.v \
  +define+CLOCK_PERIOD=0.5
% ./simv -ucli +verbose=1
ucli% source ../icc-par/force_regs.ucli
ucli% run
...
  + Running Test Case: gcdGCDUnit_rtl
     [ passed ] Test ( vcTestSink ) succeeded, [ 0003 == 0003 ]
     [ passed ] Test ( vcTestSink ) succeeded, [ 0007 == 0007 ]
     [ passed ] Test ( vcTestSink ) succeeded, [ 0005 == 0005 ]
     [ passed ] Test ( vcTestSink ) succeeded, [ 0001 == 0001 ]
     [ passed ] Test ( vcTestSink ) succeeded, [ 0028 == 0028 ]
     [ passed ] Test ( vcTestSink ) succeeded, [ 000a == 000a ]
     [ passed ] Test ( vcTestSink ) succeeded, [ 0005 == 0005 ]
     [ passed ] Test ( vcTestSink ) succeeded, [ 0000 == 0000 ]
     [ passed ] Test ( Is sink finished? ) succeeded
...
% vpd2vcd vcdplus.vpd vcdplus.vcd
% vcd2saif -input vcdplus.vcd -output vcdplus.saif
```

You can use the provided Makefile to build the post synthesis gate-level netlist simulator, run, and convert the switching activity file into a `vcd` and a `saif` format.

```
% cd $LABROOT/build/vcs-sim-gl-par
% make
% make run
% make convert
```

Synopsys PrimeTime PX: Estimating Power

PrimeTime PX is an add-on feature to PrimeTime that analyzes power dissipation of a cell-based design. PrimeTime PX supports two power analysis modes: averaged and time-based. Averaged mode estimates average power consumption based on toggle rates. Time-based mode estimates the peak power consumption as well as the averaged power using gate-level simulation activity.

```
% cd $LABROOT/build-unscripted/pt-pwr
% pt_shell -64bit
```

```
...
pt_shell> alias "pt_shell>" ""
```

Go ahead and execute some commands to setup your environment. Enable the power analysis mode.

```
pt_shell> set ucb_vlsi_home [getenv UCB_VLSI_HOME]
pt_shell> set stdcells_home \
  $ucb_vlsi_home/stdcells/synopsys-90nm/default
pt_shell> set search_path "$stdcells_home/db"
pt_shell> set target_library "cells.db"
pt_shell> set link_path "* $target_library"
pt_shell> set power_enable_analysis "true"
```

Load the post place and route gate-level netlist into PrimeTime PX.

```
pt_shell> read_verilog "../icc-par/gcdGCDUnit_rtl.output.v"
pt_shell> current_design "gcdGCDUnit_rtl"
pt_shell> link
```

First try averaged mode power analysis. This mode takes the `saif` format file as input. Load in the parasitics information produced by IC Compiler before you run `report_power`.

```
pt_shell> set power_analysis_mode "averaged"
pt_shell> read_saif "../vcs-sim-gl-par/vcdplus.saif" \
  -strip_path "gcdTestHarness_rtl/gcd"
pt_shell> report_switching_activity -list_not_annotated
pt_shell> read_parasitics -increment \
  -format sbpf "../icc-par/gcdGCDUnit_rtl.output.sbpf.max"
pt_shell> report_power -verbose -hierarchy
...
                                Switch   Int      Leak      Total
Hierarchy                       Power    Power    Power     Power    %
------------------------------------------------------------------------------
gcdGCDUnit_rtl                  9.48e-05 9.48e-05 1.52e-05  2.05e-04 100.0
  dpath (gcdGCDUnitDpath_W16)   8.29e-05 6.67e-05 1.42e-05  1.64e-04  80.0
    clk_gate_A_reg_reg (SNPS_CLOCK_GATE_HIGH_gcdGCDUnitDpath_W16_1)
                                3.14e-05 1.35e-05 2.22e-07  4.52e-05  22.1
    clk_gate_B_reg_reg (SNPS_CLOCK_GATE_HIGH_gcdGCDUnitDpath_W16_0)
                                3.14e-05 1.27e-05 2.22e-07  4.44e-05  21.7
  ctrl (gcdGCDUnitCtrl)         1.19e-05 2.81e-05 9.46e-07  4.09e-05  20.0
...
```

This shows you the average power consumption of your design, broken down by module.

Now try time-based power analysis. This mode takes a `vcd` format file as input. Load the parasitics information and run `report_power`. The report will include the estimated peak power as well as average power.

```
pt_shell> set power_analysis_mode "time_based"
```

```
pt_shell> read_vcd "../vcs-sim-gl-par/vcdplus.vcd" \
  -strip_path "gcdTestHarness_rtl/gcd"
pt_shell> report_switching_activity -list_not_annotated
pt_shell> read_parasitics -increment \
  -format sbpf "../icc-par/gcdGCDUnit_rtl.output.sbpf.max"
pt_shell> report_power -verbose -hierarchy
...
                                Switch   Int      Leak      Total
Hierarchy                       Power    Power    Power     Power    %
------------------------------------------------------------------------------
gcdGCDUnit_rtl                  1.37e-04 1.05e-04 1.51e-05  2.57e-04 100.0
  dpath (gcdGCDUnitDpath_W16)   1.21e-04 7.69e-05 1.42e-05  2.12e-04  82.3
    clk_gate_A_reg_reg (SNPS_CLOCK_GATE_HIGH_gcdGCDUnitDpath_W16_1)
                                4.62e-05 1.33e-05 2.22e-07  5.96e-05  23.2
    clk_gate_B_reg_reg (SNPS_CLOCK_GATE_HIGH_gcdGCDUnitDpath_W16_0)
                                4.80e-05 1.21e-05 2.22e-07  6.03e-05  23.4
  ctrl (gcdGCDUnitCtrl)         1.67e-05 2.79e-05 9.37e-07  4.54e-05  17.7


                                Peak     Peak            Glitch   X-tran
Hierarchy                       Power    Time            Power    Power
------------------------------------------------------------------------------
gcdGCDUnit_rtl                  1.49e-02  72.000-72.001  3.19e-07 7.61e-09
  dpath (gcdGCDUnitDpath_W16)   9.05e-03 173.325-173.326 2.29e-07    0.000
    clk_gate_A_reg_reg (SNPS_CLOCK_GATE_HIGH_gcdGCDUnitDpath_W16_1)
                                2.69e-03 129.999-130.000 2.78e-09    0.000
    clk_gate_B_reg_reg (SNPS_CLOCK_GATE_HIGH_gcdGCDUnitDpath_W16_0)
                                2.71e-03  49.999-50.000     0.000    0.000
  ctrl (gcdGCDUnitCtrl)         9.44e-03  27.999-28.000  9.05e-08 7.61e-09
...
```

Makefiles can be used to automate this procedure.

```
% cd $LABROOT/build/pt-pwr
% make
```

Introduction to Chisel

Chisel is a hardware description language currently under development at UC Berkeley. In this section, your assignment is to re-implement GCD in Chisel, and then to push the Chisel generated Verilog representation of the design through the toolflow. So far, we have been working in the `lab1-verilog/` directory, but now we will start working in `lab1-chisel/`.

For our purposes, Chisel adds one extra step to the beginning of the traditional tool flow. The Chisel code is used to generate Verilog files, after which point the rest of the flow stays the same. One major difference arises when debugging a design: when doing so, we only modify the Chisel code and never edit the Chisel generated Verilog files directly. The Verilog serves purely as an intermediate representation of the design.

Next, we will describe the directory structure used for the Chisel based design. `src/` is where Chisel code should go, and `src/work.scala` is the top level file that instantiates the modules in your design. We have provided an incomplete implementation of GCD in the `src/gcd.scala` file which you should fill in with your Chisel code. The interface between the module and test the test harness is provided, so you only need to implement body of the component. If you like, you can use the Verilog implementation as a guide and do an almost direct translation, or you can experiment with some of Chisel's language features to make the implementation more clear and concise. Typing `make vlsi` in the top level project directory will invoke the Chisel compiler to produce a Verilog representation of your design and place the resulting file in the `vlsi/generated-src` directory.

To push this code through the VLSI toolflow, go to `vlsi/build`, which is essentially the same as `lab1-verilog/build` and push the design through the flow by following the same steps outlined earlier in the lab.

Using the Chisel tool flow

Before starting, make sure you have the most recent version of the lab template.

```
% cd /work/cs250-ab/lab1-chisel/
% git pull template master
```

Figure 10 shows each directory in the lab1-chisel hierarchy and includes comments about what each one contains.

lab1-chisel/

- Makefile — "make verilog" takes .scala from src/ and generates vlsi/generated-src/*.v
- .gitignore — Tells Git to ignore generated-src/, dynamically generated files in sbt/
- sbt/ — "Magic" directory for chisel
- src/ — Chisel code (*.scala). top.scala is a mandatory top level file that instantiates design
- emulator/ — Chisel target: C emulator
  - Makefile — Automate emulator testing
  - generated-src/ — C code generated by Chisel
  - testbench/ — Testbench that drives Chisel C emulator
- vlsi/ — Chisel target: VLSI
  - build/ — VLSI toolflow for vlsi/generated-src
    - Makefile — Controls all pieces of toolflow. Eg. "make dc-syn" will synthesize
    - vcs-sim-rtl/ — Simulate RTL in generated-src/
    - dc-syn/ — Synthesize RTL in generated-src/
    - vcs-sim-gl-syn/ — Simulate synthesized netlist in dc-syn/current-dc
    - icc-par/ — Place and route synthesized netlist from dc-syn/current-dc
    - vcs-sim-gl-par/ — Simulate place and routed netlist in icc-par/current-icc
    - pt-pwr/ — Power analysis of design in icc-par/current-icc
  - generated-src/ — Verilog code generated by Chisel (*.v)
  - Makefile — Does nothing by default. Will be used later for design space exploration

Notation:
blue means that these files generated dynamically, and are not stored in the repository

Figure 10: Directory organization for lab1-chisel/

Change your `$LABROOT` environment variable to point to the top level directory of the Chisel version of this design.

```
% cd /work/cs250-ab/lab1-chisel/
% LABROOT=$PWD
$ cd src
$ vim work.scala
```

You are now looking at the top level Chisel file. This is just boilerplate code that instantiates the top level module in your design. This is also where the interfaces to testbenches are defined. Next, open the code describing the GCD module that is being instantiated in `top.scala`

```
% vim gcd.scala
```

This is where you need to fill in the design with some of your own Chisel code. When you are ready to test your code, there are two methods you can choose from. First, the Chisel compiler can produce C++ code which implements a cycle accurate simulation of your design. To generate the C++ code, compile the simulator, and run the testbench, run the following commands:

```
% cd $LABROOT
% make emulator
% cd emulator
% make run
```

In addition to a C++ description of a simulator, the Chisel compiler can also generate Verilog code that can be used as input to an ASIC flow like the one you experimented with earlier in this lab. As long as the components in Chisel have the same names as their counterparts in the Verilog implementation (which is true in this case because we supplied the top level interface to you with the same naming scheme) you can re-use the same Verilog testbench for your Chisel-generated Verilog code. Once your design passes the tests in simulation, go ahead and push it through the rest of the steps in the flow.

```
% cd $LABROOT
% make vlsi
% cd vlsi/build/vcs-sim-rtl
% make run
```

Debugging

You can use either the C++ simulator, or simulate the generated Verilog files using VCS (in the vcs-sim-rtl directory) to debug your Chisel design.

To debug using the C++ simulator, you can add printf statements to `testbench/GCD-emulator.cpp`. All internal signals are renamed as `GCD__oldsignalname` unless there are duplicates, and the top level input/outputs are always accesible. Look in `generated-src/GCD.h` Another technique is to use GDB (traditional debugger for C/C++ programs) Other methods are currently under development.

Here is an example of how you might use GDB to debug your Chisel design:

```
% cd $LABROOT/emulator
% vim generated-src/GCD.cpp
(find the line number of the last line in the clock_lo function)
% gdb GCD-emulator
gdb% break GCD.cpp:linenumYouFound
gdb% run
gdb% p/x GCD__signalname
gdb% p/x GCD__signalname_shadow (the value signal will have during the next cycle)
gdb% c (go to next cycle)
```

To debug using the Verilog , you can use the same procedure that was described earlier. Notice that the design will contain many signals with the `T_` prefix, which hold intermediate values produced by the Chisel compiler.

```
% cd $LABROOT
% cd vlsi/build/vcs-sim-rtl
% make run
% dve -full64 -vpd vcdplus.vpd &
```

Questions

Your writeup should not exceed two pages in length. Make your writing as crisp as you can!

Q1. W=16 vs. W=32 (For Verilog implementation only)

Throughout the lab, you assumed that the operands A, B, and the result were 16 bits wide. Now we'd like to build a GCD unit which operates on 32 bit values and produces a 32 bit result.

- What changes would you need to make to the `gcdGCDUnit_rtl` module?
- Does the Verilog provided test harness `gcdTestHarness_rtl` work with the 32-bit version of GCD? If not, what changes do you need to make in order to test our new 32-bit `gcdGCDUnit_rtl` module? Demonstrate that your 32-bit `gcdGCDUnit_rtl` functions correctly.
- How does this change effect the area/power/performance properties of the chip? Fill in the boxes in the following table by finding the values in the reports generated by the tools. Write a python script to go through all the reports and extract the data you are after. Use the output of your script to fill in the boxes in the table. Running a script to gather the data should look something like this:

  ```
  % cd $LABROOT/build
  % ./collect_data.py
  ```

Q2. Chisel vs. Verilog

Tell us how the results of pushing your Chisel generated Verilog version of GCD differ from the results produced when building the Verilog RTL version of GCD we provided. Be sure to describe the differences between key metrics such as performance, energy, and area by using the script you wrote for Q1. If there are differences, can you determine the cause?

	Unit	`gcdGCDUnit_rtl (W=16)`	`gcdGCDUnit_rtl (W=32)`
Post Synthesis Critical Path Length	ns		
Post Synthesis Area	um^2		
Post Synthesis Power	mW		
Post Place+Route Critical Path Length	ns		
Post Place+Route Area	um^2		
Post Place+Route Power	mW		
Average Power (max)	mW		
Peak Power (max)	mW		
Total Cell Count (exclude `SHFILL*` Cell)			
`DFFX*` Cell Count			

Q3. 90nm vs. 32nm (Verilog Implementation only

Now, you will push the Verilog version of GCD that we gave you through the toolflow, but this time targeting a 32nm process. First, please run `git pull template master` to fetch the latest version of the lab template files. Use the build infrastructure in the `lab1-verilog/build-32nm` directory. All you need to do is type `make` in that directory and the tools should all run in sequence. One they have finished, fill out a table like the one from Q1 but comparing the 90nm and 32nm implementations of GCD. Use the script you wrote for Q1 to extract the necessary information from the reports produced by the tools.

Read me before you commit!

- Commiting is not enough for us to grade this lab, you will also need to push your changes to github with the following command: `git push origin master`
- As you may have learned in this lab, makefiles for Design Compiler, IC Compiler, PrimeTime PX makes a new build directory for every new run. Don't submit multiple build directories. Make sure that you only turn in the most recent build result.
- You don't need to submit results for the VCS simulation. We will build and run simulation based on your committed source code or gate-level netlist.
- When you commit a symbolic link in Git, it stores the link as a file, and if the link is to a folder, it does not look past this. Therefore just adding current-dc will do nothing, you also need to do a git add of build directory that it points to.
- Try using .gitignore to avoid tracking `build-unscripted` or any older builds
- You don't need to submit build results which are done manually (from the first part of the lab)

- To summarize, your Git tree for lab1 should look like the following (use the github.com browser to check that everything is there):

```
/yunsup
  /lab1-verilog
    /src: no change
    /build: COMMIT PYTHON SCRIPT
      /dc-syn: COMMIT THE MOST RECENT BUILD VERSION
      /icc-par: COMMIT THE MOST RECENT BUILD VERSION
      /pt-pwr: COMMIT THE MOST RECENT BUILD VERSION
      /vcs-sim-behav: no change
      /vcs-sim-gl-par: no change
      /vcs-sim-gl-syn: no change
      /vcs-sim-rtl: no change
    /build-unscripted: no change
  /lab1-chisel
    /src: COMMIT CHISEL CODE
    /vlsi:
      /build:
        /dc-syn: COMMIT THE MOST RECENT BUILD VERSION
        /icc-par: COMMIT THE MOST RECENT BUILD VERSION
        /pt-pwr: COMMIT THE MOST RECENT BUILD VERSION
        /vcs-sim-behav: original files only
        /vcs-sim-gl-par: original files only
        /vcs-sim-gl-syn: original files only
        /vcs-sim-rtl: original files only
  /writeup: COMMIT REPORT
```

Acknowledgements

Many people have contributed to versions of this lab over the years. The lab was originally developed for CS250 VLSI Systems Design course at University of California at Berkeley by Yunsup Lee. Contributors include: Krste Asanović, Christopher Batten, John Lazzaro, and John Wawrzynek. Versions of this lab have been used in the following courses:

- CS250 VLSI Systems Design (2009-2011) - University of California at Berkeley
- CSE291 Manycore System Design (2009) - University of California at San Diego