Outline

- Well plugs - why?
  - Latch-up
  - Body effect
- Large transistor layout
- Input/Output pads
p-well inverter Layout
Other Planar CMOS Processes

- **n-well**
  - Strong n-type

- **twin-tub**
  - Both types controlled

- **Silicon on Insulator (SOI)**
  - Insulator (sapphire)
  - "Islands"
Latest Modern Process

Transistor channel is a raised fin.
Gate controls channel from sides and top.

How do we increase the width of a FinFET?
# Semi-conductor Materials

<table>
<thead>
<tr>
<th>I</th>
<th>II</th>
<th>III</th>
<th>IV</th>
<th>V</th>
<th>VI</th>
<th>VII</th>
<th>Zero</th>
</tr>
</thead>
<tbody>
<tr>
<td>H</td>
<td>Li</td>
<td>Be</td>
<td>B</td>
<td>C</td>
<td>N</td>
<td>O</td>
<td>F</td>
</tr>
<tr>
<td>Na</td>
<td>Mg</td>
<td>Al</td>
<td>Si</td>
<td>P</td>
<td>S</td>
<td>Cl</td>
<td>Ar</td>
</tr>
<tr>
<td>K</td>
<td>Zn</td>
<td>Ga</td>
<td>Ge</td>
<td>As</td>
<td>Se</td>
<td>Br</td>
<td>Kr</td>
</tr>
<tr>
<td>Rb</td>
<td>Cd</td>
<td>In</td>
<td>Sn</td>
<td>Sb</td>
<td>Te</td>
<td>I</td>
<td>Xe</td>
</tr>
</tbody>
</table>

- **II**: 4 valence electrons in outer shell. Outer shell holds 8 electrons.
- **III**: 3 valence electrons. "Acceptor impurities"
- **VI**: 5 valence electrons. "Donors"

Why Si?
Doping Materials

Intrinsic Silicon

Doped Silicon

n-type material
electron rich

p-type material
hole “bubble” rich

10\(^{15}\) atoms/cm\(^2\) — 10\(^{19}\) atoms/cm\(^2\)

“donor”

“acceptor”
The **depletion region** and it’s modulation explains lots of important properties important to circuit designers: drain/source capacitance, body-effect.

MOS Transistor

MOS Transistor

Gate (poly)

oxide

diffusion

n+

Channel

p-Type Substrate

Surface Inversion

\[ V_g \geq V_{th} \]

\[ V_{th} = 0.2 \times V_{dd} \]

\[ \approx 1 \text{V} \]

VGS = 0
Parasitic Bipolar Transistors

In this case collector tried to Vdd

This may be a useful device. ex. photo detector.

Can we make these?
Latchup

n-substrate

Dangerous situation! pnpn

Vertical n-p-n
β ≈ 100

Lateral p-n-p
β ≈ 2

If the base of either transistor gets biased (> 0.6V) relative to the emitter, - Latch up.

Vdd is shorted to GND!! + stuck that way!!

Well/Substrate Contacts help Rs

... they short each base.

But are not perfect.
Latchup

- **Triggers:** any effect that can properly bias one of the bipolar transistors will trigger the latch-up loop.
  - transmission line reflections or ringing on the chip outputs
  - “hot plug-in”
  - ESD (electrostatic discharge)
  - internal transients on pwr and gnd busses due to switchin or capacitive coupling
  - radiation: x-ray, cosmic, alpha rays create electron/hole pairs

- **Cures:**
  - bipolar beta reduction
  - resistive shunting
  - process techniques - SOI, epi-substrate
  - special precautions for I/O pad drivers.
Body Effect (back-gate effect)

- Opportunity to have user control over Vth?

\[ AV_{th} = \gamma (V_{sb})^{1/2} \]

Typically: \( \gamma = 0.5 V^{1/2} \)

- \( V_{sb} = 0V \); \( V_{th} = 0.2V_{dd} \) (\( = +1V \) @ \( V_{dd} = +5V \))
- \( V_{sb} = 5V \); \( V_{th} = 1V + 0.5V^{1/2} \cdot (5V)^{1/2} \)

- Better for “native” devices.

- Slower circuits: \( I_{ds} \propto V_{gs} - V_{th} \)
Body Effect in Stacks or Cascades

Cascaded n-pullups (p-pulldowns)

\[\begin{align*}
V_{in} & \quad V_a \quad V_{in} \quad V_b \quad V_{in} \\
\downarrow & \quad \downarrow \quad \downarrow \quad \downarrow \quad \downarrow
\end{align*}\]

\(t_0: \quad V_a = V_b = V_c = V_{in} = 0\)

\(t_+: \quad V_{in} \rightarrow V_{dd}\)

\(t_0: \quad V_a = V_{dd} - V_{th}\)

\(V_b = \quad \)

\(V_c = \quad \)

Can we live with this?

Maybe - but, watch out for the

\begin{center}
- Body Effect -
\end{center}

When even source node not grounded (at \(V_{dd}\))
Well/Substrate Plugs

Connect n substrate to VDD &
p well to GND
Guard Bands

- Use deep diffusion as barrier to stray carriers in substrate
- Isolate highly energetic areas (output pads, big drivers)
- Important in mixed-signal ICs to protect Analog circuits
Layout of Wide Transistors

- Clock drivers, bus drivers, output pad drivers

Issues:
1) gate RC delay,
2) layout aspect ratio
3) drain capacitance
Wide Transistor Layout

Three stage buffer layout:
I/O Pad Circuits: Options

- Typical Multi-tier Wire Bond (PBGA) Package
- Flip Chip PBGA (FC-PBGA)

Bonding Pad Ring Layout

Area Pad Chip Layout
Off Chip Pad Drivers

Basic Functions
- I/O buffering
- Electro-static discharge (ESD) protection
- Level conversion / deglitching

Basic bidirectional pad:

\[ \text{tri-state drivers:} \]

Both relatively big or slow. Why?

Tri-state driver for large \( C \) loads:

\[
\begin{array}{ccccccc}
\text{en} & \text{d} & \text{out} & \text{p} & \text{n} \\
00 & 01 & 01 & 10 & 0 \\
01 & 00 & 11 & 00 & 0 \\
10 & 00 & 00 & 00 & 0 \\
11 & 00 & 10 & 10 & 0 \\
\end{array}
\]
Electro-static Charge Protection

FIGURE 5.56 An electrostatic model of a person. (a) Physical configuration; (b) Equivalent circuit.

Simple protection structure:

Diode structure

How do we make the resistor?
I/O Pad Cell

- **0.6 μm three-metal process**
  - Similar I/O drivers
  - Big driver transistors provide ESD protection
  - Guard rings around driver

Area pad design is similar, but often a “redistribution layer” is used to separate pad from driver circuits.
End of Lecture 13