CS250
VLSI Systems Design

Lecture 2: Chisel Introduction

Spring 2017

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HDL History

- Verilog originated at Automated Integrated Design Systems (renamed Gateway) in 1985. Acquired by Cadence in 1989.
- Invented as simulation language. Synthesis was an afterthought. Many of the basic techniques for synthesis were developed at Berkeley in the 80's and applied commercially in the 90's.
- Around the same time as the origin of Verilog, the US Department of Defense developed VHDL (A double acronym! VSIC (Very High-Speed Integrated Circuit) HDL). Because it was in the public domain it began to grow in popularity.
- Afraid of losing market share, Cadence opened Verilog to the public in 1990.
- An IEEE working group was established in 1993, and ratified IEEE Standard 1394 (Verilog) in 1995.
- Verilog is the language of choice of Silicon Valley companies, initially because of high-quality tool support and its similarity to C-language syntax.
- VHDL is still popular within the government, in Europe and Japan, and some Universities.
- Most major CAD frameworks now support both.
- Latest Verilog version is "System Verilog" .
- Other alternatives these days:
  - Bluespec (MIT spin-out) models digital systems using "guarded atomic actions"
  - C-to-gates Compilers (ex: Cadence C-to-s, Vivado HLS)

Problems with Verilog

- Designed as a simulation language. "Discrete Event Semantics"
  - Many constructs don't synthesize: ex: deassign, timing constructs
  - Others lead to mysterious results: for-loops
  - Difficult to understand synthesis implications of procedural assignment (always blocks), and blocking versus non-blocking assignments
  - No "real" registers.
  - Your favorite complaint here!
  - In common use, most users ignore much of the language and stick to a very strict "style". Companies post use rules and run lint style checkers. Nonetheless leads to confusion (particularly for beginners), and bugs.

- The real power of a textual representation of circuits is the ability to write circuit "compilers". Verilog has very weak "meta-programming" support". Simple parameter expressions, generate loops and case.
- Various hacks around this over the years, ex: embedded TCL scripting.

```
// Gray-code to binary-code converter
module gray2bin1 (bin, gray);
    parameter SIZE = 8;
    output [SIZE-1:0] bin;
    input  [SIZE-1:0] gray;

    genvar i;

    generate for (i=0; i<SIZE; i=i+1) begin:bit
      assign bin[i] = ^gray[SIZE-1:i];
    end endgenerate
  endmodule
```

Chisel

Constructing Hardware In a Scala Embedded Language

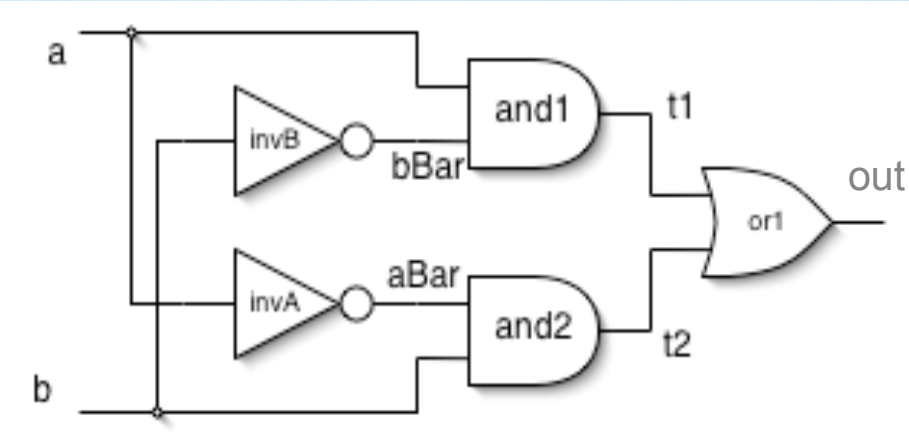
- Experimental attempt at a fresh start to address these issues.
  - Clean simple set of design construction primitives, just what is needed for RTL design
  - Powerful "metaprogramming" model for building circuit generators
- Why embedded?
  - Avoid the hassle of writing and maintaining a new programming language (most of the work would go into the non-hardware specific parts of the language anyway).
- Why Scala?
  - Brings together the best of many others: Java JVM, functional programming, OO programming, strong typing, type inference.
- Still relatively new. Bugs will show up. Your feedback is needed.
- In class, brief presentation of basics. Ask questions.
- Tutorial/manual and other documents available online: chisel.berkeley.edu
- Note: Chisel is not High-level Synthesis. Much closer to Verilog/VHDL than C-to-gates.

Outline

- Brief Introduction to Chisel
- Literal Constructors
- Bundles, Port Constructors, Vecs
- Components and Circuit Hierarchy
- More on Multiplexors
- Registers
- Conditional Update Rules
- FSMs
- More on Interface Bundles, and Bulk Connections
- Running

Simple Combinational Logic Example

```
// simple logic expression

(a & ~b) | (~a & b)
```

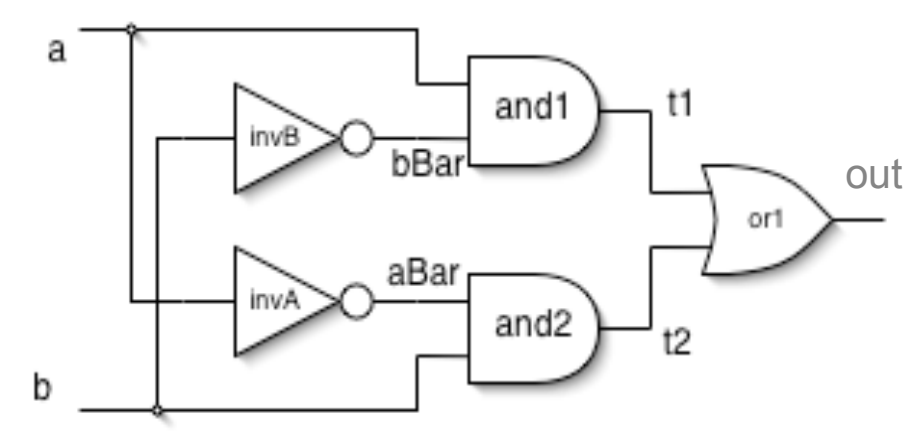


- Notes:
  - The associated logic circuits are not "executed". They are active always (like continuous assignment in Verilog).
  - Unlike Verilog, no built-in logic gates. Expressions instead.
  - The "variables", `a` and `b`, are "named wires", and were given names here because they are inputs to the circuit. Other wires don't need names.
  - Here we assumed that the inputs, and therefore all generated wires, are one bit wide, but the same expression would work for wider wires. The logic operators are "bitwise".
    - Chisel includes a powerful wire width inference mechanism.

Simple Combinational Logic Example

- In the previous example because the wires `a` and `b`, are named, each can be used in several places. Similarly we could name the circuit output:

```
// simple logic expression

val out =(a & ~b) | (~a & b)
```



- The keyword `val` comes from Scala. It is a way to declare a program variable that can only be assigned once - a constant (not a logic constant - but a constant circuit declaration - can't later change the expression that generates out).
- This way `out` can be generated at one place in the circuit and then "fanned-out" to other places where `out` appears.

```
// fan-out

val z =(a & out) | (out & b)
```

- Another reason to name a wire is to help in debugging.

Functional Abstraction

- Naming wires and using fanout gives us a way to reuse an output in several places in the generated circuit. Function abstraction gives us a way to reuse a **circuit description**:

```
// simple logic function

def XOR (a: Bits, b: Bits) = (a & ~b) | (~a & b)
```

- Here the function inputs and output are assigned the type `Bits`. More on types soon.
- Now, wherever we use the `XOR` function, we get a copy of the associated logic. Think of the function as a "constructor".

```
// Constructing multiple copies

val z =(x & XOR(x,y)) | (XOR(x,y) & y)
```

- Functions wrapping up simple logic are light-weight. This results in hierarchy in your code, but no hierarchy in the Chisel output.
- We'll see later that **Chisel Modules** are used for building hierarchy in the resulting circuit.

Datatypes in Chisel

- **Chisel datatypes are used to specify the type of values held in state elements or flowing on wires.**
- Hardware circuits ultimately operate on vectors of binary digits, but more abstract representations for values allow clearer specifications and help the tools generate more optimal circuits.
- The basic types in Chisel are:

`Bits`	Raw collection of bits (parent type)
`SInt`	Signed integer number
`UInt`	Unsigned integer number
`Bool`	Boolean

- All signed numbers represented as 2's complement.
- Chisel supports several higher-order types: Bundles and Vecs.

Type Inference

- **Although it is useful to keep track of the types of your wires, because of Scala type inference, it is not always necessary to declare the type.**
- For instance in our earlier example:

```
// simple logic expression
val out =(a & ~b) | (~a & b)
```

the type of out was inferred from the types of `a` and `b` and the operators.

- If you want to make sure, or if there is not enough information around for the inference engine, you can always specify the type explicitly:

```
// simple logic expression
val out: Uint =(a & ~b) | (~a & b)
```

- Also, as we shall see, explicit type declaration is necessary in some situations.

Bundles

- **Chisel Bundles represent collections of wires with named fields.**
- Similar to "struct" in C. In chisel, Bundles are defined as a class (similar to in C++ and Java):

```
class ComplexNum(W:Width) extends Bundle {
  val real = SInt(W)          // Real Component
  val imag = SInt(W)         // Imaginary Component
}
```

- Chisel has class methods for Bundle (i.e., automatic connection creation) therefore user created bundles need to "extend" class Bundle. (More later)
- Each field is given a name and defined with a constructor of the proper type and with parameters specifying width and direction.
- Instances of `ComplexNum` can now be made:

```
val myNum = new ComplexNum(32.W)
```

- Bundle definitions can be nested and built into hierarchies,
- And are used to define the interface of "modules" …

Bundles with directions

```
class FIFOInput extends Bundle {
  val rdy = Output(Bool())          // Indicates if FIFO has space
  val data = Input(UInt(32.W))      // The value to be enqueued
  val enq = Input(Bool())           // Assert to enqueue data
}
```

- Instances of `FIFOInput` can now be made:

```
val jonsIO = new FIFOInput
```

- Bundle definitions can be nested and built into hierarchies,
- And are used to define the interface of "modules" …
- Bundle "flip" operator is used to create the "opposite" Bundle (wrt to direction)

```
val jonsIO = Flipped(new FIFOInput)
```

- Truth is, that this particular interface is predefined, call "`DecoupledIO`"

Literals

- Literals are values specified directly in your source code.
- Chisel defines type specific constructors for specifying literals.

```
"ha".U      // hexadecimal 4-bit literal of type Bits
"o12".U     // octal 4-bit literal of type Bits
"b1010".U   // binary 4-bit literal of type Bits
5.S         // signed decimal 4-bit literal of type Fix
-8.S        // negative decimal 4-bit literal of type Fix
5.U         // unsigned decimal 3-bit literal of type UFix
true.B      // literals for type Bool, from Scala boolean literals
false.B
```

- By default Chisel will size your literal to the minimum necessary width.
- Alternatively, you can specify a width value as an argument:

```
"ha".asUInt(8.W)    // hexadecimal 8-bit literal of type Bits, 0-extended
-5.asSInt(32.W)     // 32-bit decimal literal of type Fix, sign-extended
```

- Error reported if specified width value is less than needed.

Builtin Operators

- Chisel defines a set of hardware operators for the builtin types.

Bool Operators:

Chisel	Explanation	Width
`!x`	Logical NOT	1
`x && y`	Logical AND	1
`x || y`	Logical OR	1

Bits Operators:

Chisel	Explanation	Width
`x(n)`	Extract bit, 0 is LSB	1
`x(n, m)`	Extract bitfield	`n - m + 1`
`x << y`	Dynamic left shift	`w(x) + maxVal(y)`
`x >> y`	Dynamic right shift	`w(x) - minVal(y)`
`x << n`	Static left shift	`w(x) + n`
`x >> n`	Static right shift	`w(x) - n`
`Fill(n, x)`	Replicate x, n times	`n * w(x)`
`Cat(x, y)`	Concatenate bits	`w(x) + w(y)`
`Mux(c, x, y)`	If c, then x; else y	`max(w(x), w(y))`
`~x`	Bitwise NOT	`w(x)`
`x & y`	Bitwise AND	`max(w(x), w(y))`
`x | y`	Bitwise OR	`max(w(x), w(y))`
`x ^ y`	Bitwise XOR	`max(w(x), w(y))`
`x === y`	Equality (triple equals)	1
x =/= y	Inequality	1
`andR(x)`	AND-reduce	1
`orR(x)`	OR-reduce	1
`xorR(x)`	XOR-reduce	1

UInt, SInt Operators: (bitwdths given for `UInts`)

Chisel	Explanation	Width
`x + y`	Addition	`max(w(x), w(y))`
`x - y`	Subtraction	`max(w(x), w(y))`
`x * y`	Multiplication	`w(x) + w(y)`
`x / y`	Division	`w(x)`
`x % y`	Modulus	`bits(maxVal(y) - 1)`
`x > y`	Greater than	1
`x >= y`	Greater than or equal	1
`x < y`	Less than	1
`x <= y`	Less than or equal	1
`x >> y`	Arithmetic right shift	`w(x) - minVal(y)`
`x >> n`	Arithmetic right shift	`w(x) - n`

Bit-width Inference

- **A nice feature of the Chisel compiler is that it will automatically size the width of wires.**
- The bit-width of ports (of modules) and registers must be specified, but otherwise widths are inferred with the application of the following rules:

operation	bit width
`z = x + y` *or* `z = x +% y`	`w(z) = max(w(x), w(y))`
`z = x +& y`	`w(z) = max(w(x), w(y)) + 1`
`z = x - y` *or* `z = x -% y`	`w(z) = max(w(x), w(y))`
`z = x -& y`	`w(z) = max(w(x), w(y)) + 1`
`z = x & y`	`w(z) = min(w(x), w(y))`
`z = Mux(c, x, y)`	`w(z) = max(w(x), w(y))`
`z = w * y`	`w(z) = w(x) + w(y)`
`z = x << n`	`w(z) = w(x) + maxNum(n)`
`z = x >> n`	`w(z) = w(x) - minNum(n)`
`z = Cat(x, y)`	`w(z) = w(x) + w(y)`
`z = Fill(n, x)`	`w(z) = w(x) * maxNum(n)`

Bundles and Vecs

- **Bundle and Vec are classes for aggregates of other types.**
- The Bundle class similar to "struct" in C, collection with named fields:

```
class MyFloat extends Bundle {
  val sign = Bool()
  val exponent = SInt(8.W)
  val significant = UInt(23.W)
}
val x = Wire(new MyFloat())
val xs = x.sign
```

- The Vec class is an indexable array of same type objects:

```
val myVec = Wire(Vec(5, SInt(23.W))) // Vec of 5 23-bit signed integers.
val fourth = myVec(3) // select the fourth element
```

- Note: Vec is not a memory array. It's a collection of wires (or registers).
- Vec and Bundle inherit from class, **Data** (along with UInt, SInt, and Bool). Every object that ultimately inherits from Data can be represented as a bit vector in a hardware design.
-

```
class BigBundle extends Bundle {
  val myVec = Vec(5, SInt(23.W)) // Vector of 5 23-bit signed integers.
  val flag = Bool()
  val f = new MyFloat() // Previously defined bundle.
}
```

Ports

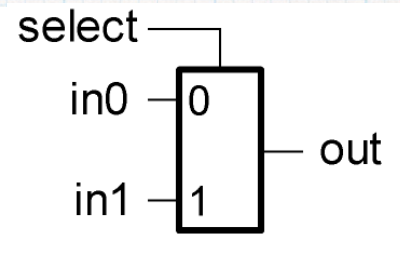
- ***A port is any*** `Data` object with directions assigned to its members.
- Port constructors allow a direction to be added at construction time:

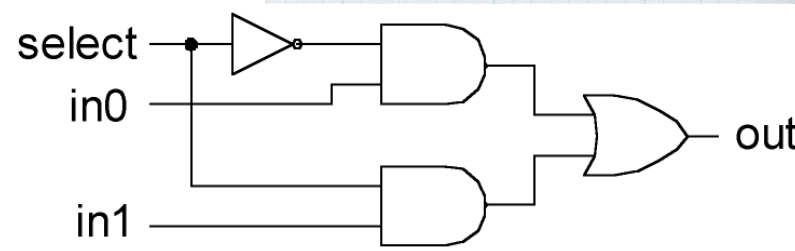
```
class Decoupled extends Bundle {
  val rdy =  Output(Bool())
  val data = Output(UInt(32.W))
  val enq =  Input(Bool())
}
```

Modules

- **Modules are used to define hierarchy in the generated circuit.**
- Similar to modules in Verilog.
- Each defines a port interface, wires together subcircuits.
- Module definitions are class definitions that extend the Chisel Module class.

```
class Mux2 extends Module {
  val io = IO(new Bundle{
    val select = Input(UInt(1.W))
    val in0 = Input(UInt(1.W))
    val in1 = Input(UInt(1.W))
    val out = Output(UInt(1.W))
  })
  io.out := (io.select & io.in1) |
            (~io.select & io.in0)
}
```



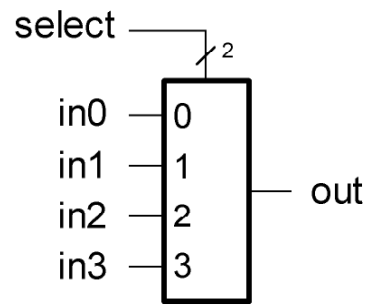


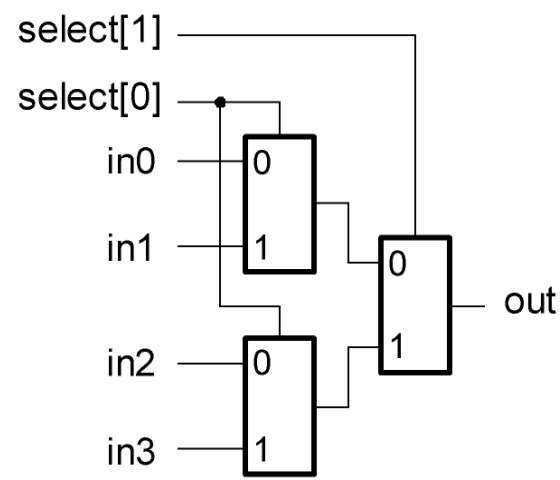
- The Module slot `io` is used to hold the interface definition, of type Bundle. `io` is assigned a Bundle that defines its ports.
- In this example,
  - `io` is assigned to an **anonymous** Bundle,
  - ":=" assignment operator, in Chisel wires the input of LHS to the output of circuit on the RHS

Component Instantiation

- Modules are used to define hierarchy in the generated circuit.

```
class Mux4 extends Module {
  val io = IO(new Bundle {
    val in0    = Input(UInt(1.W))
    val in1    = Input(UInt(1.W))
    val in2    = Input(UInt(1.W))
    val in3    = Input(UInt(1.W))
    val select = Input(UInt(2.W))
    val out    = Output(UInt(1.W))
  })
  val m0 = Module(new Mux2)
  m0.io.select := io.select(0); m0.io.in0 := io.in0; m0.io.in1 := io.in1

  val m1 = Module(new Mux2)
  m1.io.select := io.select(0); m1.io.in0 := io.in2; m1.io.in1 := io.in3

  val m3 = Module(new Mux2)
  m3.io.select := io.select(1)
  m3.io.in0 := m0.io.out; m3.io.in1 := m1.io.out

  io.out := m3.io.out
}
```





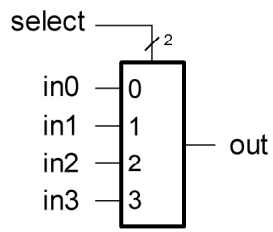
Component Functional Abstraction

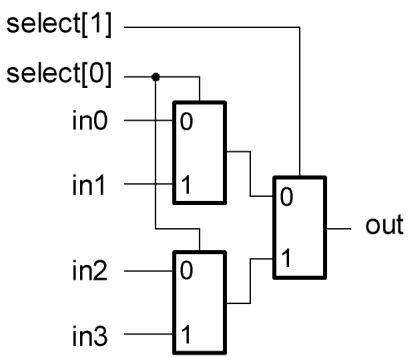
- Functional constructors for Modules can simplify your code.

```
object Mux2 {
  def apply (select: UInt, in0: UInt, in1: UInt) = {
    val m = Module(new Mux2)
    m.io.in0 := in0
    m.io.in1 := in1
    m.io.select := select
    m.io.out                          // return the output
  }
}
```

- object Mux2 creates a Scala singleton object on the Mux2 component class.
- apply defines a method for creation of a Mux2 instance

```
class Mux4 extends Module {
  val io = IO(new Bundle {
    val in0    = Input(UInt(1.W))
    val in1    = Input(UInt(1.W))
    val in2    = Input(UInit(1.W))
    val in3    = Input(UInit(1.W))
    val select = Input(UInit(2.W))
    val out    = Output(UInt(1.W))
  })
  io.out := Mux2(io.select(1),
                 Mux2(io.select(0), io.in0, io.in1),
                 Mux2(io.select(0), io.in2, io.in3))
}
```





More on Multiplexors

- **Chisel defines a constructor for n-way multiplexors**

```
MuxLookup(index, default,
          Array(key1->value1, key2->value2,..., keyN->valueN))
```

- The index to key match is implemented using the "===" operator.
- Therefore MuxLookup would work for any type for which === is defined.
- "===" is defined on bundles and vecs, as well as the primitive Chisel types.
- Users might can override "===" for their own bundles.

- **MuxCase generalizes this by having each key be an arbitrary condition**

```
MuxCase(default, Array(c1 -> a, c2 -> b, ...))
```

- where the overall expression returns the value corresponding to the first condition evaluating to true.

Registers

- **Simplest form of state element supported by Chisel is a positive-edge-triggered register. Is instantiated functionally as:**

```
Reg(next = (a & ~b) | (~a & b))
```

- This circuit has an output that is a copy of the input signal delayed by one clock cycle.
- Note, we do not have to specify the type of Reg as it will be automatically inferred from its input when instantiated in this way.
- In Chisel, clock and reset are global signals that are implicitly included where needed
- Example use. Rising-edge detector that takes a boolean signal in and outputs true when the current value is true and the previous value is false:

```
def risingedge(x: Bool) = x && !Reg(next = x)
```

The Counter Example

- Constructor for an up-counter that counts up to a maximum value, `max`, then wraps around back to zero (i.e., modulo `max+1`):

```
def wraparound(n: UInt, max: UInt) =
  Mux(n > max, 0.U, n)

def counter(max: UInt) = {
  val y = Reg(init = 0.asUInt(max.getWidth))
  y := wraparound(y + 1.U, max)
  y
}
```

- Constructor for a circuit to output a pulse every `n` cycles:

```
// Produce pulse every n cycles.
def pulse(n: UInt) = counter(n - 1.U)) === 0.U
```

- "Toggle flip-flop" - toggles internal state when `ce` is true:

```
// Flip internal state when input true.
def toggle(ce: Bool) = {
  val x = Reg(init = false.B))
  x := Mux(ce, !x, x)
  x
}
```

```
def squareWave(period: UInt) = toggle(pulse(period/2))
```

Conditional Updates

- **Instead of wiring register inputs to combinational logic blocks, it is often useful to specify when updates to the registers will occur and to specify these updates spread across several separate statements (think FSMs).**

```
val r = Reg(UInt(16.W))
  when (c === 0) {
    r := r + 1.U
  }
```

- register r is updated on the next rising-clock-edge iff c is zero.
- The argument to when is a predicate circuit expression that returns a Bool.
- The update block can only contain update statements using the update operator, simple expressions, and named wires defined with val.
- Cascaded conditional updates possible with ".elsewhen" and ".otherwise". Ex:

```
when(c1){
  r := 1.U
}.elsewhen(c2){
  r := 2.U
}.otherwise {
 r := 3.U
}
```

- Leads to:

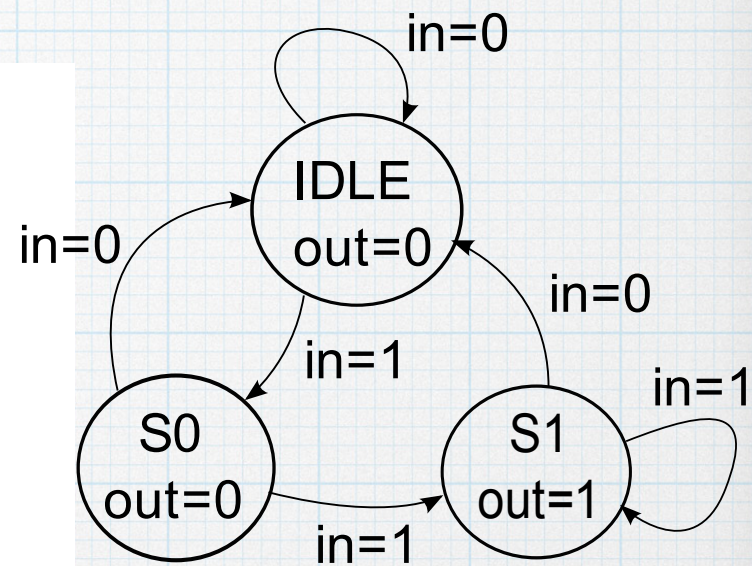
c1	c2	r
0	0	3
0	1	2
1	0	1
1	1	1

- See tutorial for more examples, and variations on this them.

Finite State Machine Specification (1)

- When blocks help in FSM specification:

```
class MyFSM extends Module {
  val io = IO(new Bundle {
    val in  = Input(Bool())
    val out = Output(Bool())
  })
  val IDLE :: S0 :: S1 :: Nil = Enum(3)
  val state = Reg(init = IDLE);
  when (state === IDLE) {
    when (io.in) { state := S0 }
  }
  when (state === S0) {
    when (io.in) { state := S1 }
    .otherwise { state := IDLE }
  }
  when (state === S1) {
    when (!io.in) { state := IDLE }
  }
  io.out := state === S1;
}
```

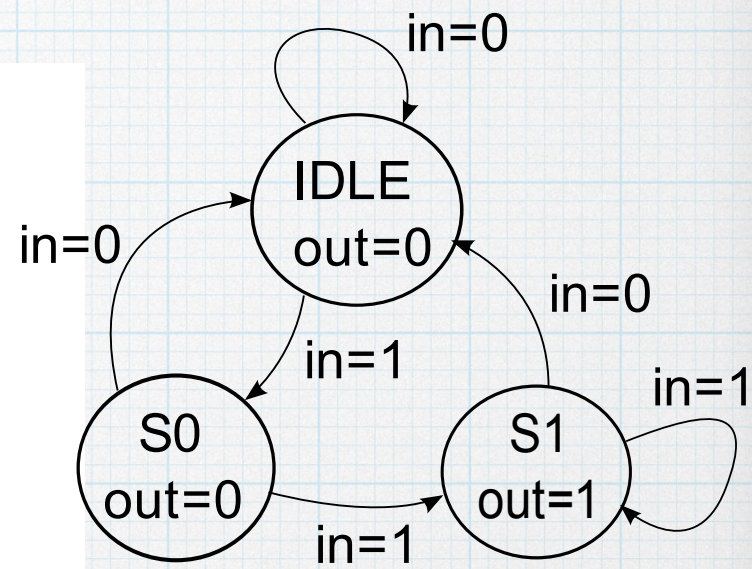


- Enum(3) generates three Uint lits, used here to represent states values.
- See tutorial for more complex FSM example (?).

Finite State Machine Specification (2)

- Switch helps in FSM specification:

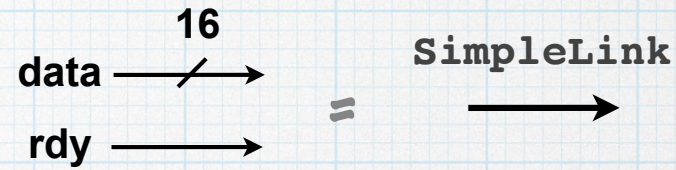
```
class MyFSM extends Component {
  val io = new Bundle {
    val in = Input(Bool())
    val out = Output(Bool())
  }
  val IDLE :: S0 :: S1 :: Nil = Enum(3)
  val state = Reg(resetVal = IDLE);
  switch (state) {
    is (IDLE) {
      when (io.in) { state := S0 }
    }
    is (S0) {
      when (io.in) { state := S1 }
      .otherwise { state := IDLE }
    }
    is (S1) {
      when (!io.in) { state := IDLE }
    }
  }
  io.out := state === S1;
}
```



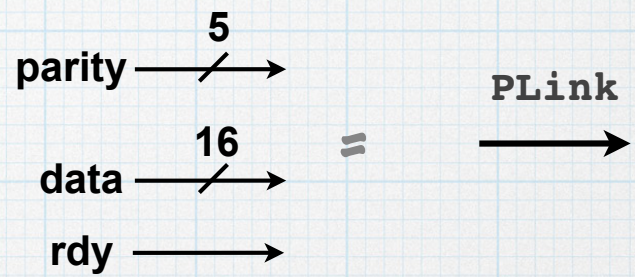
Interfaces and Bulk Connections (1)

- Bundles help with interface definitions

```
class SimpleLink extends Bundle {
  val data = Output(UInt(16.W))
  val rdy  = Output(Bool())
}
```




```
// Bundle Inheritance
class PLink extends SimpleLink {
  val parity = Output(Unit(5.W))
}
```



- `PLink` extends `SimpleLink` by adding parity bits.

```
// Super Bundle through nesting
class FilterIO extends Bundle {
  val x = Flipped(new PLink())
  val y = new PLink()
}
```

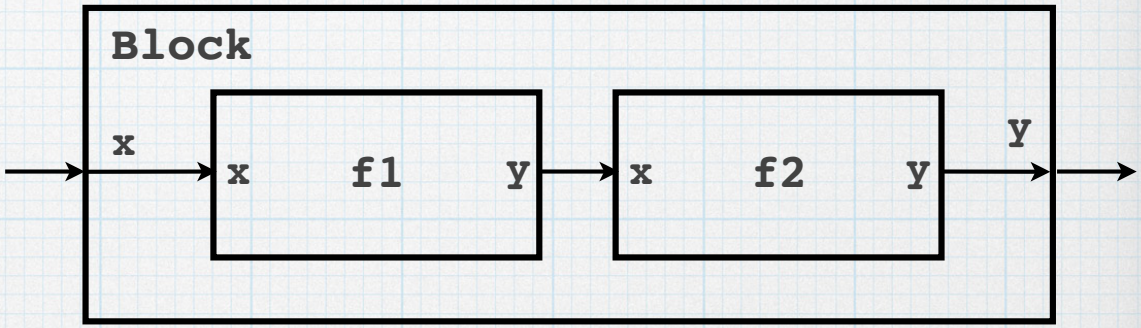
  - `FilterIO` aggregates other bundles.
  - "`Flipped`" recursively changes the "gender" of members.

Interfaces and Bulk Connections (2)

- Bundles help with making connections

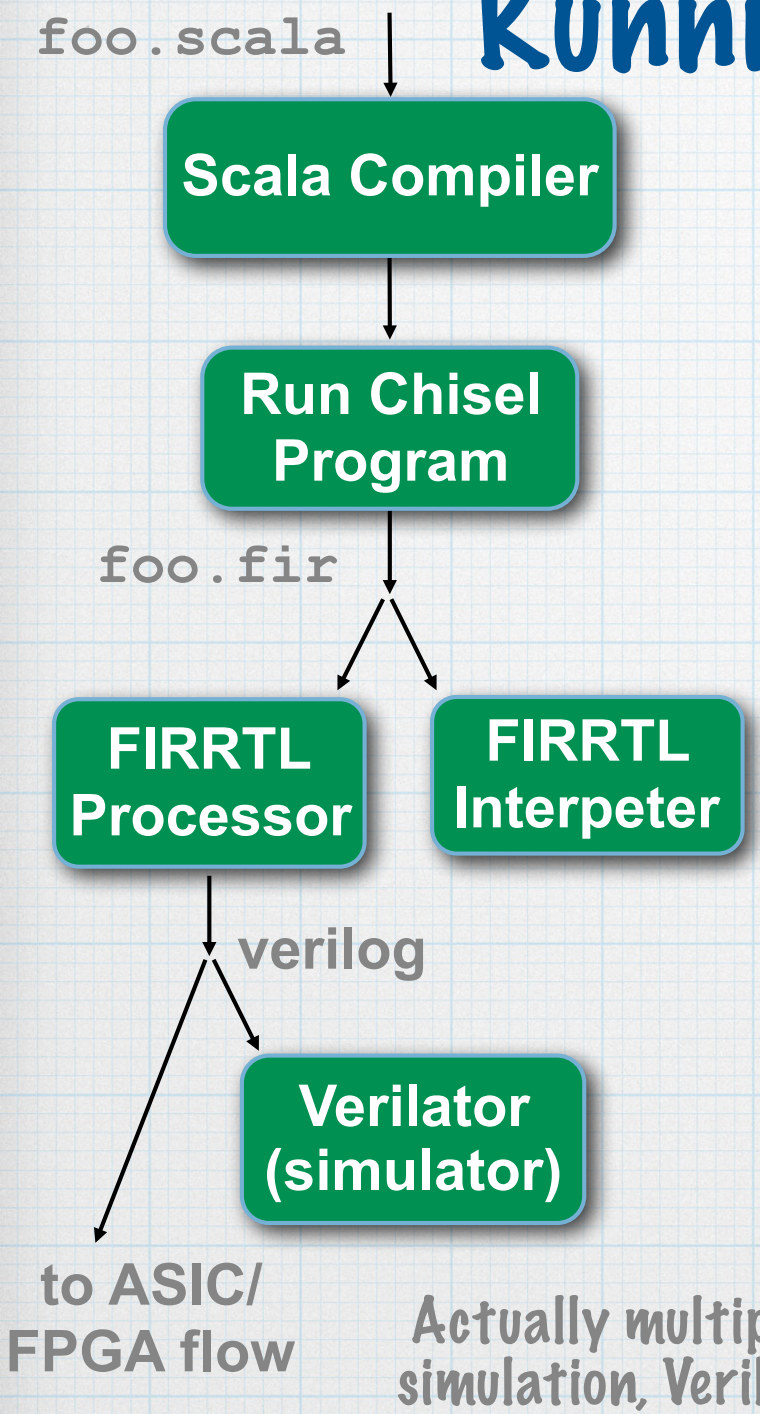
```
class Filter extends Module {
  val io = IO(new FilterIO())
...
}
```


```
/ Bulk connections
class Block extends Module {
  val io = IO(new FilterIO())

  val f1 = Module(new Filter())
  val f2 = Module(new Filter())

  f1.io.x <> io.x;
  f1.io.y <> f2.io.x;
  f2.io.y <> io.y;
}
```



- "<>" bulk connects bundles of opposite gender, connecting leaf ports of the same name to each other.
- "<>" also promotes child component interfaces to parent component interfaces.

Running and Testing (1)



Scala Compiler generates an executable (Chisel program)

Execution of the Chisel program:

- generates an internal data structure and output called FIRRTL (flexible intermediate representation for RTL)
- FIRRTL "processor":
  - resolves wire widths
  - checks connectivity
  - generates target output (verilog for now)
  - FIRRTL interpeter or verilator used for simulation

Actually multiple different verilog targets "are" possible, pure simulation, Verilog for ASIC mapping, Verilog for FPGA mapping

More Information

- We will use Chisel 2.2.x not 3.0
- chisel.eecs.berkeley.edu/documentation.html

Chisel3 Cheat Sheet

Version 0.5 (beta): December 14, 2016

Notation In This Document:
For Functions and Constructors:
Arguments given as `kwd:type` (name and type(s))
Arguments in brackets (`[...]`) are optional.
For Operators:
`c`, `x`, `y` are Chisel `Data`; `n`, `m` are Scala `Int`
`w(x)`, `w(y)` are the widths of `x`, `y` (respectively)
`minVal(x)`, `maxVal(x)` are the minimum or maximum possible values of `x`

Basic Chisel Constructs

Chisel Wire Operators:

`val x = UInt()`	Allocate `a` as wire of type `UInt()`
`x := y`	Assign (connect) wire `y` to wire `x`
`x <> y`	Bulk connect `x` and `y`, control wires directionalityis automatically inferred

When executes blocks conditionally by `Bool`, and is equivalent to Verilog `if`

```
when(condition1) {
  // run if condition1 true and skip rest
} .elsewhen(condition2) {
  // run if condition2 true and skip rest
} .otherwise {
  // run if none of the above ran
}
```

Switch executes blocks conditionally by data

```
switch(x) {
  is(value1) {
    // run if x === value1
  } is(value2) {
    // run if x === value2
  }
}
```

Enum generates value literals for enumerations

```
val s1::s2:: ... ::sn::Nil
    = Enum(nodeType:UInt, n:Int)
```

`s1, s2, ..., sn`	will be created as `nodeType` literals with distinct values
`nodeType`	type of `s1, s2, ..., sn`
`n`	element count

Math Helpers:

`log2Up(in:Int): Int`	log_2(in) rounded up

Basic Data Types

Constructors:
`Bool([x:Boolean])`
`Bits/UInt/SInt([x:Int/String], [width:Int])`

`x`	*(optional)* create a literal from Scala type/ parsed `String`, or declare unassigned if missing
`width`	*(optional)* bit width (inferred if missing)

Bits, UInt, SInt Casts: reinterpret cast except for:

`UInt` → `SInt`	Zero-extend to SInt

State Elements

Registers retain state until updated
`val my_reg = Reg([outType:Data], [next:Data], [init:Data])`

`outType`	*(optional)* register type (or inferred)
`next`	*(optional)* update value every clock
`init`	*(optional)* initialization value on reset

Updating: assign to latch new value on next clock:
`my_reg := next_val`

Read-Write Memory provide addressable memories
`val my_mem = Mem(n:Int, out:Data)`

`out`	memory element type
`n`	memory depth (elements)

Using: access elements by indexing:
`val readVal = my_mem(addr:UInt/Int)`
for synchronous read: assign output to `Reg`
`mu_mem(addr:UInt/Int) := y`

Modules

Defining: subclass `Module` with elements, code:

```
class Accum(width:Int) extends Module {
  val io = new Bundle {
    val in = UInt(INPUT,  width)
    val out  = UInt(OUTPUT, width)
  }
  val sum = new Reg(UInt())
  sum := sum + io.in
  io.out := sum
}
```

Usage: access elements using dot notation:
(code inside a `Module` is always running)

```
val my_module = Module(new Accum(32))
my_module.io.in := some_data
```

Operators:

Chisel	Explanation	Width
`!x`	Logical NOT	`1`
`x && y`	Logical AND	`1`
`x || y`	Logical OR	`1`
`x(n)`	Extract bit, `0` is LSB	`1`
`x(n, m)`	Extract bitfield	`n - m + 1`
`x << y`	Dynamic left shift	`w(x) + maxVal(y)`
`x >> y`	Dynamic right shift	`w(x) - minVal(y)`
`x << n`	Static left shift	`w(x) + n`
`x >> n`	Static right shift	`w(x) - n`
`Fill(n, x)`	Replicate `x`, `n` times	`n * w(x)`
`Cat(x, y)`	Concatenate bits	`w(x) + w(y)`
`Mux(c, x, y)`	If `c`, then `x`; else `y`	`max(w(x), w(y))`
`~x`	Bitwise NOT	`w(x)`
`x & y`	Bitwise AND	`max(w(x), w(y))`
`x | y`	Bitwise OR	`max(w(x), w(y))`
`x ^ y`	Bitwise XOR	`max(w(x), w(y))`
`x === y`	Equality(triple equals)	`1`
`x != y`	Inequality	`1`
`x =/= y`	Inequality	`1`
`x + y`	Addition	`max(w(x),w(y))`
`x +% y`	Addition	`max(w(x),w(y))`
`x +& y`	Addition	`max(w(x),w(y))+1`
`x - y`	Subtraction	`max(w(x),w(y))`
`x -% y`	Subtraction	`max(w(x),w(y))`
`x -& y`	Subtraction	`max(w(x),w(y))+1`
`x * y`	Multiplication	`w(x)+w(y)`
`x / y`	Division	`w(x)`
`x % y`	Modulus	`bits(maxVal(y)-1)`
`x > y`	Greater than	`1`
`x >= y`	Greater than or equal	`1`
`x < y`	Less than	`1`
`x <= y`	Less than or equal	`1`
`x >> y`	Arithmetic right shift	`w(x) - minVal(y)`
`x >> n`	Arithmetic right shift	`w(x) - n`

UInt bit-reduction methods:

Chisel	Explanation	Width
`x.andR`	AND-reduce	`1`
`x.orR`	OR-reduce	`1`
`x.xorR`	XOR-reduce	`1`

As an example to apply the andR method to an SInt use x.asUInt.andR

End of HDLs/Chisel Introduction

Advanced Chisel Later:

Memory Blocks
Polymorphism and Parameterization
Higher-order Functions