Speedster FPGA Family

achronix
SEMICONDUCTOR CORPORATION

DS001 Rev. 1.2 – October 16, 2009 Advance

Highlights

- Fastest FPGA in the world
  - Up to 1.5 GHz performance
  - Fully reprogrammable, SRAM-based
  - Based on proven 65 nm TSMC processes
- Large capacity
  - Up to 1.5 Million ASIC gates
  - 800 MHz 18 Kb RAM blocks
  - 1.5 GHz 18 x 18 embedded multipliers
  - Up to 40 channels of embedded 5 or 10.3 Gbps SerDes
- Industry-standard register transfer level (RTL) synthesis support:
  - Synplify Pro from Synplicity
  - Precision Synthesis from Mentor Graphics
- High performance achieved without requiring manual modification or optimization
  - Use existing Verilog or VHDL RTL code
  - Rapid timing closure yielding significant time-to-market advantages
- Performance trade-offs capability:
  - Lower power consumption
  - Higher effective capacity
- 10.3 Gbps SerDes supporting high-speed serial interfaces including:
  - PCI-Express
  - Gigabit Ethernet
  - CEI-6G
  - 10.3 Gbps Backplane
  - Interlaken
  - XAUI
  - Infiniband
  - XFI
- Industry-standard memory interfaces supported:
  - SDR SDRAM (200 Mbps)
  - QDR SRAM (400 Mbps)
  - QDRII SRAM (800 Mbps)
  - RLDRAM II (1066 Mbps)
  - DDR1 SDRAM (400 Mbps)
  - DDR2 SDRAM (800 Mbps)
  - DDR3 SDRAM (1066 Mbps)
- Industry-standard datapath interfaces supported:
  - SPI-4.2 (up to 1000 Mbps)
  - SFI-4.1 (622 Mbps)
  - XSBI (644 Mbps)

Product Table

Table 1: *Speedster FPGA Family Members*

Features	SPD30	SPD60	SPD100	SPD180
Number of 4-Input LUTs	24,576	47,040	93,848	163,840
picoPIPE Pipeline Elements	1,725,000	3,400,000	7,200,00	11,700,000
Number of 18 Kbit Block RAMs	66	144	334	556
Available Block RAM (Kbit)	1188	2592	6012	10008
Available Distributed RAM (Kbit)	384	735	1232	2560
Number of 18 x 18 Multipliers	50	98	120	270
Number of 5 Gbps SerDes Lanes	–	8	–	–
Number of 10.375 Gbps SerDes Lanes	8	20	36	40
DDR3/DDR2 Controller (1066 Mbps)(1)	2	4	4	4
Number of PLLs	8	16	16	16
Use Programmable I/Os	488	792	832	933

Notes:

1. DDR Controller width selectable from 8 to 72 bits.

Device Overview

The Speedster® FPGA fabric employs a regular array of Reconfigurable Logic Blocks (RLBs) connected through programmable routing interconnect. Each RLB contains eight 4-input look-up tables (LUTs), and supplementary logic structures, such as carry chains. Alternatively, an RLB can be configured as 128 bits of 1.5 GHz performance distributed RAM (LRAM).

In addition to programmable LUTs, Speedster FPGAs also contain dedicated 18 Kb block RAMs and 18 x 18 block multipliers, all capable of 1.5 GHz performance. The high-performance interconnect allows all of the fabric components to be connected at the maximum throughput. For example, multipliers can be combined with LUT-based adders, accumulators and other functions, to build high-performance DSP functions.

The RLBs, block RAMs and multipliers are arranged in columns on a Speedster FPGA (a simplified example is shown in **Figure 1**). Surrounding the fabric are the Boundary Elements which ensure synchronization of signals with the externally provided or internally generated clocks from the PLL (see **"Boundary Elements,"** on page 5 for details).

A key architectural element in all Speedster FPGA devices is the I/O Frame which contains configurable I/Os, SerDes, clock generator blocks with Phase Lock Loops (PLLs), and the device configuration logic. Speedster FPGAs contain up to 40 high-performance SerDes lanes and up to an additional 850 high-speed reconfigurable I/Os. Dedicated clock I/O pins are located near the corners of each Speedster device. In addition, there are dedicated I/Os for the embedded programming and configuration logic (CFG) designed to support a variety of programming options. Up to four DDR/DDR2/DDR3 PHY interfaces and controllers are also included in each Speedster FPGA.

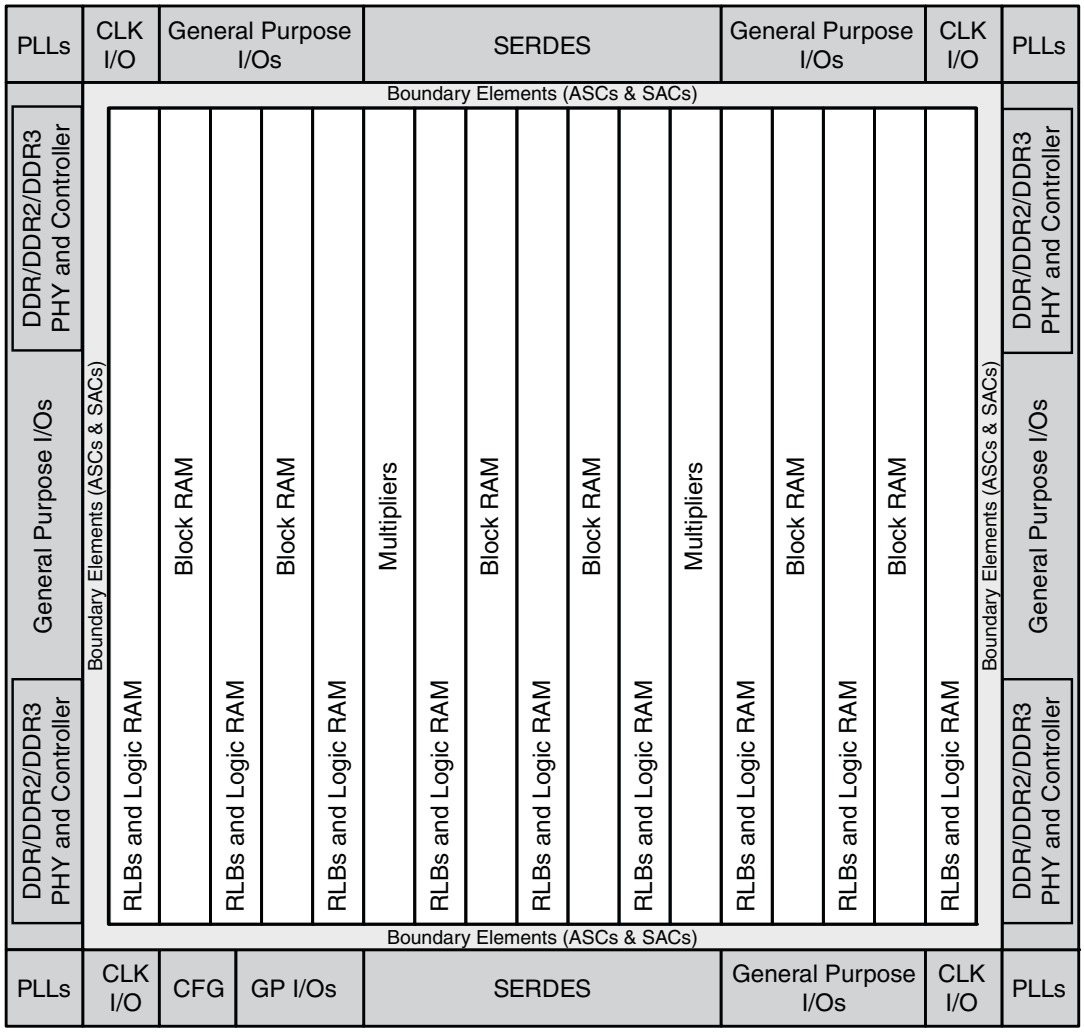


Figure 1: *Speedster Device Overview*

Technology Overview

The Speedster FPGA family from Achronix Semiconductor delivers the world's fastest commercially available FPGAs. Using CMOS process technology and conventional SRAM-based device configuration, Speedster FPGAs are capable of operating at 1.5 GHz system throughput. Using unique picoPIPE™ technology, Speedster FPGAs typically achieve four to five times the data throughput compared with conventional FPGAs in the same technology node. Speedster FPGAs are suitable for a wide range of high-performance communications, networking, digital signal processing, reconfigurable computing, imaging and industrial applications.

Achronix FPGAs have a conventional synchronous I/O frame (S-Frame) surrounding a picoPIPE logic fabric (**Figure 2**). The I/O frame includes configurable I/Os, SerDes, clocks, phased-lock loops (PLLs), etc. The frame provides the off-chip interfaces and forms the boundary between the picoPIPE core and these interfaces. All data entering and exiting the core must pass through the I/O frame.

The picoPIPE fabric is formed from an array of Reconfigurable Logic Blocks (RLBs), connected through a programmable fabric. Each RLB is surrounded by Switch Boxes (SBs) as shown in **Figure 2**. The Switch Boxes route global signals across the picoPIPE fabric.

Each RLB contains eight, 4-input Look-Up Tables (LUTs), carry-chain logic, and storage elements. Alternatively, the RLB can be configured as 128 bits of distributed RAM (LRAM). In addition to RLBs and programmable routing, the picoPIPE fabric also contains dedicated block RAMs and multipliers. These features are designed to achieve a much higher throughput over conventional FPGAs.

Achronix FPGAs achieve higher throughput compared with existing FPGAs because of the fine-grained pipeline stages. Unlike existing FPGA implementations, these pipeline stages can be automatically inserted anywhere in a design without changing its logic functionality.

The remainder of this technology overview is provided for informational purposes only. Although the implementation is based on revolutionary concepts, the user enters RTL, synthesizes, simulates, and implements designs in the same way as with conventional FPGAs.

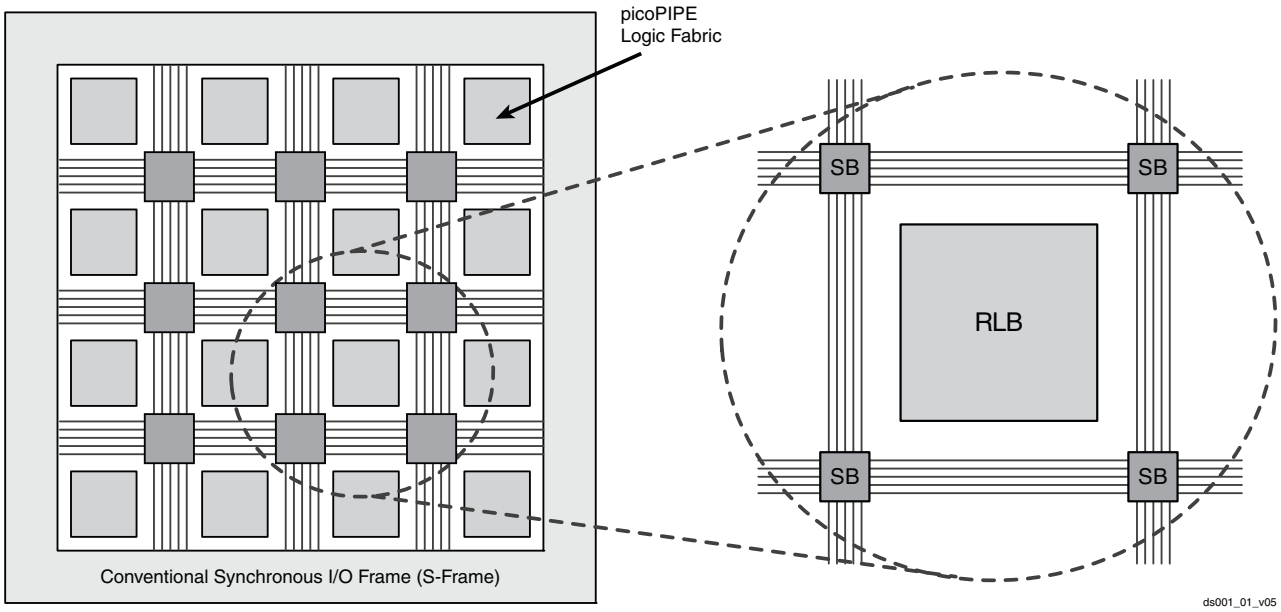


Figure 2: *Achronix FPGA Architecture*

Data Tokens

A data token is defined as the presence of valid data at the input of a storage element. In conventional logic, a data token is a logic value at a clock edge at the input of a flip-flop. Data is always present, but is only valid (and therefore propagated) at a clock edge.

In picoPIPE logic, the data value is accompanied by a valid signal. Thus, picoPIPE elements (CEs, FEs, and BEs – see **"picoPIPE Elements,"** on page 4 for details) are capable of either being empty (no data) or holding a token (valid data). A data token in picoPIPE logic can be considered as the data and the clock edge merged together. The key innovation enabling the picoPIPE fabric to operate at high frequency is this new representation of data tokens, with validity being determined not by an explicit global clock, but by a local handshaking protocol.

picoPIPE Elements

The basic storage elements of picoPIPE logic are the Connection Element (CE), the Functional Element (FE), the Boundary Element (BE) and the pipeline stage as shown in **Figure 3**.

Pipeline stages connect CEs, FEs and BEs to form pipeline networks as shown in **Figure 4**. Once combined into networks, the picoPIPE implementation exactly matches the functionality of conventional logic, but is capable of much higher throughput.

Each pipeline stage is capable of holding a data token. As a result, picoPIPE logic is highly pipelined by design. In conventional logic designs, adding pipeline stages involves adding explicit registers, changing the logic function as it introduces a new data token. In contrast, picoPIPE pipeline stages can be added without automatically adding a new data token into the circuit. This capability is possible because picoPIPE logic combines the clock and data into a single data token. A new data token is, therefore, not introduced when simply adding a new pipeline stage — pipeline stages (i.e., extra Connection Elements) can be inserted anywhere in a circuit without changing the logic function computed by the circuit, as long as the added stage is not initialized with data.

In conventional logic, when a pipeline stage (register/storage element) is added, it must still be clocked from a global clock. This automatically inserts a new data token, changing the functionality of the logic. With picoPIPE technology, inserting a connection element does not automatically cause a new data token to be inserted; thus, the logic is unchanged. Adding pipeline stages does add a small amount of latency, but nothing else.

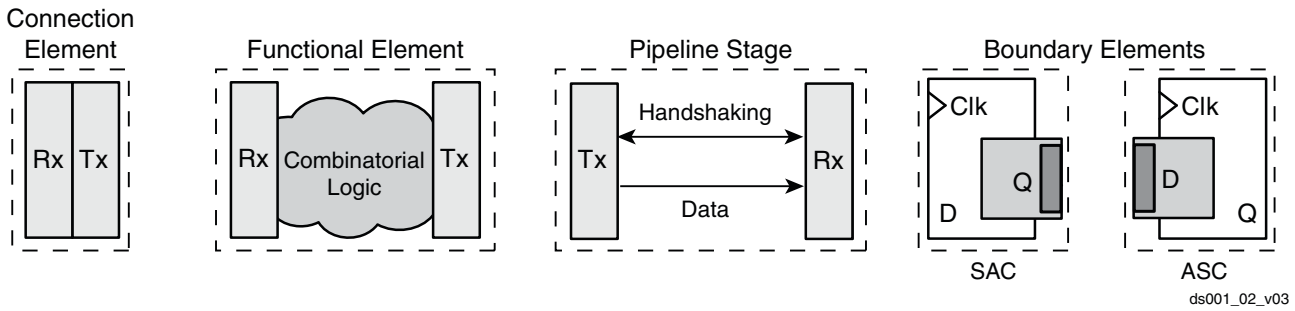


Figure 3: *picoPIPE Building Blocks*

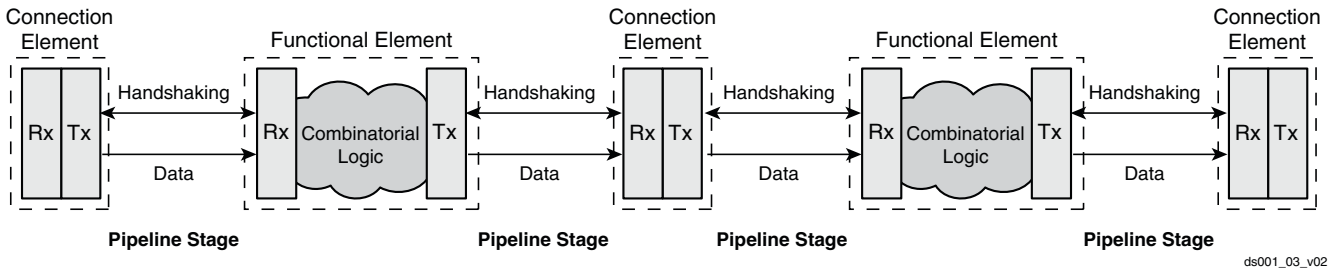


Figure 4: *PicoPIPE Pipeline Stage*

Connection Elements

CEs are unlike any existing logic structure. They are capable of being initialized into one of two states, either state-holding, or non-state-holding. When initialized as state-holding, a CE performs a similar function as a register in a conventional design — a data token is initially created for that pipeline stage. When initialized as non-state-holding, it behaves similar to a repeater. The main difference between a series of un-initialized CEs and a wire, is that each pipeline stage is still capable of containing a data token, even if it does not start with one initially. This property plays a large role in enabling the increased throughput of Achronix FPGAs, while maintaining exact logical equivalence to a conventional circuit.

Functional Elements

FEs have functionality equivalent to combinatorial logic. The only difference relates to how inputs and outputs are handled. The local handshaking within a picoPIPE network means the FEs must handshake data in and out, ensuring only valid, settled data is propagated.

Boundary Elements

Boundary Elements (BEs) populate the boundary where the picoPIPE fabric meets the FPGA frame. BEs occur in two variants: Synchronous-to-Asynchronous Converter (SAC) and the Asynchronous-to-Synchronous Converter (ASC). SACs convert data tokens from the frame into data tokens in the picoPIPE fabric (ingress). ASCs convert data tokens from the fabric back into data tokens in the frame (egress). Therefore, every signal entering and exiting the picoPIPE fabric passes through either a SAC or an ASC.

Implementing Synchronous Logic

The picoPIPE fabric implements conventional logic, maintaining equivalence between the two for every signal on every cycle.

FEs provide the combinatorial computation, implementing logic described by the Verilog or VHDL RTL code. CEs provide both the connectivity (local and global routing) and storage (registers) enabling sequential computation. In the FPGA architecture, RLBs contain FEs and CEs while the Switch Blocks contain only CEs.

Data tokens enter the picoPIPE fabric via a SAC proceed through a succession of CEs and FEs, and then exit via an ASC.

The S-Frame ensures that every data token enters the picoPIPE core at a clock edge, and every data token leaving the picoPIPE core is clocked out at a clock edge. The functional relationship of inputs and outputs is maintained between the synchronous design specified by the RTL, and the implemented functionality as observed on the boundary of the frame. SACs ensure that every valid data token in the frame (data on an input at an input clock edge) becomes a data token within the picoPIPE core. Likewise on the output, every data token leaving the picoPIPE core becomes a data token as it enters the frame (a data value is clocked out of the core).

The number of data tokens entering, and leaving the picoPIPE core is exactly the same as it would be if the core were implemented with conventional logic.

Another consideration is the number of storage elements in the original design. In conventional logic, each storage element is implemented with a register, creating its own internal data token. As CEs can be configured to be state-holding, for every storage element in the original design, a CE is initialized to add an initial data token. Thus the number of internal data tokens specified in the implementation is consistent with the original design.

Note: *As described above, additional tokenless CEs may be introduced without modifying the functionality.*

Pipeline Stages

As **Figure 5**, page 6 shows, there are often many levels of logic between (sequential) storage elements. It takes time for data to propagate from the register output (Q), through the combinatorial logic and settle at a stable state on the next register's D input. As the clock cannot occur until all data is settled, the clock speed cannot run faster than the longest path in the entire design. Data in every path that is shorter than the longest path (by definition, all other paths) must wait for the longest path.

In stark contrast, picoPIPE technology allows optimum pipelining without changing the logic functionality, as shown in **Figure 5**. Each pipeline stage has less logic depth and therefore completes its operation rapidly, allowing the rate of data tokens through the logic to be increased, therefore increasing the effective clock rate.

Note: *In picoPIPE technology, data tokens are a combination of valid data, and clock information.*

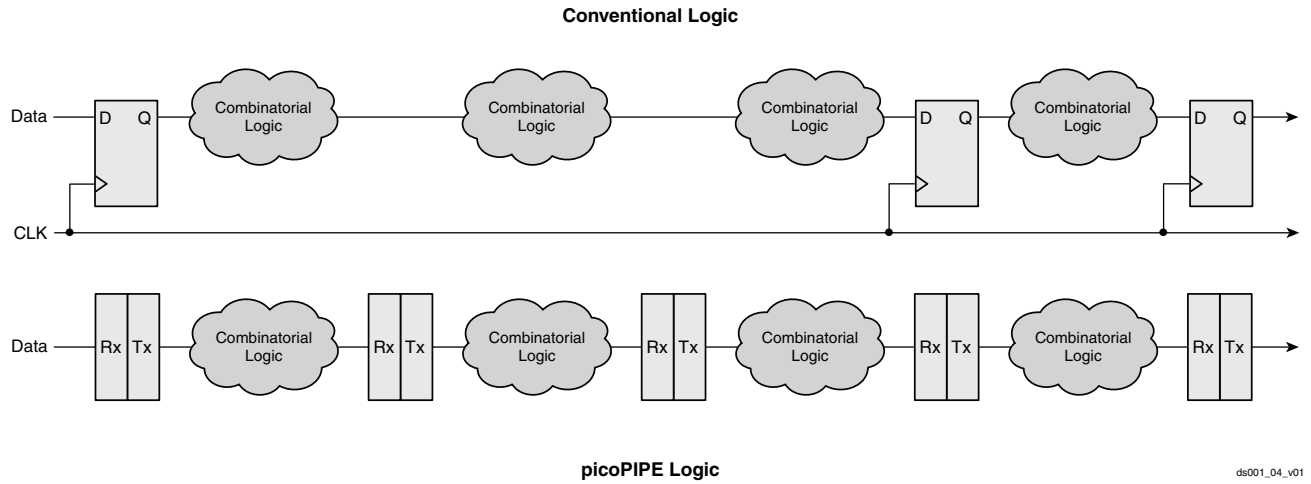


Figure 5: *picoPIPE vs. Existing FPGA Implementation*

Within conventional FPGAs, signals travel on long routing tracks and pass through routing components (**Figure 6**). These signals suffer from high-capacitance (especially through interconnects) — the larger the FPGA, the longer the paths to be traversed. Additionally, there are often many levels of logic between state-holding elements (registers).

Within Speedster FPGAs, the built-in pipelining ensures that signals only travel on short routing tracks, reducing the capacitance of the signal at each stage. For larger devices, signals still may need to propagate from one corner of the device to the other. While larger devices may have slightly increased latency, unlike other FPGAs, they do not have decreased throughput as each pipeline stage is capable of holding a new data token. Therefore, the inherent pipelining of picoPIPE technology allows maximum throughput to be maintained, regardless of how large the FPGA is. Fine-grained pipelining also ensures there is a maximum of one level of logic per pipeline stage, allowing an extremely fast data-token rate.

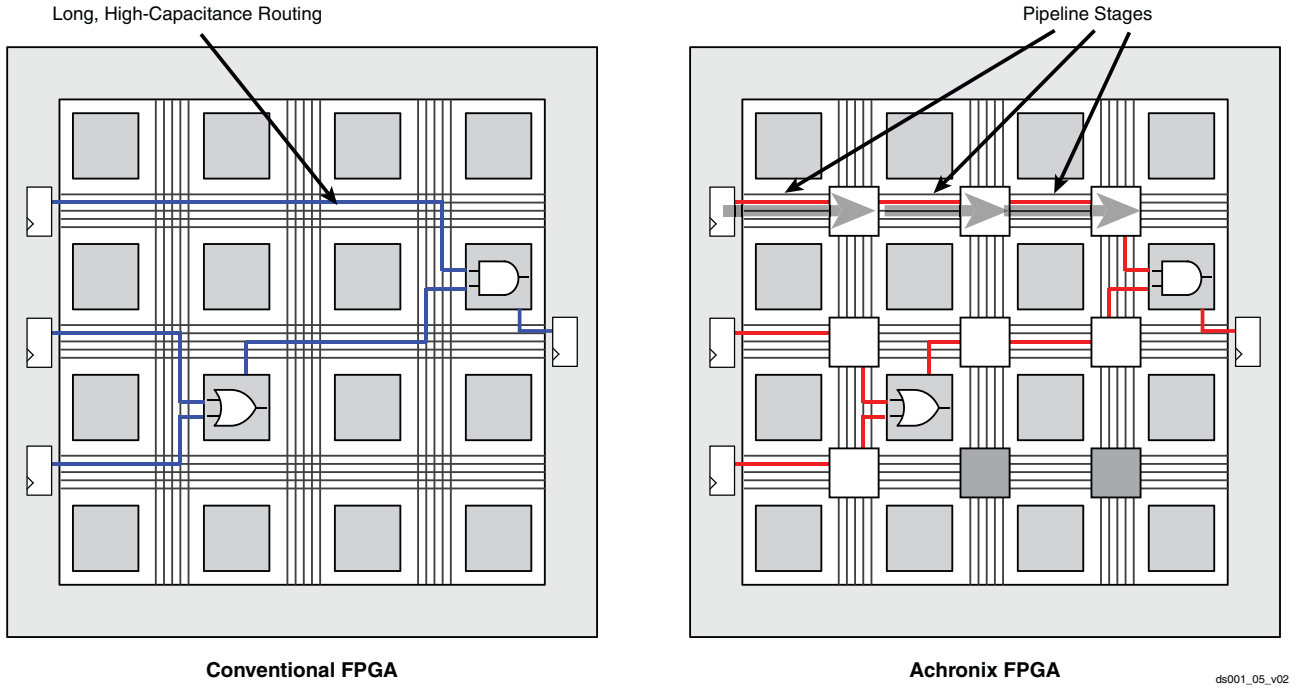


Figure 6: *Conventional Implementation vs. picoPIPE Implementation*

Logic Fabric

The logic fabric is composed of multiple tiles — identical building blocks organized in a regular grid structure, as shown in **Figure 7**.

Functional Partition: Logic and Interconnect

The logic portion of the tile is called a Reconfigurable Logic Block (RLB), which is in turn subdivided into Logic Clusters and Look Up Table (LUT) structures (detailed below). The RLB is the main resource for the implementation of user logic. Each RLB contains:

- Four Logic Clusters (LC), arranged in two pairs
- One pair, the Carry Logic Cluster (CLC) has carry chains
- A fast local interconnect structure

The interconnect portion of the tile is the Switch Block (SB) — a programmable interconnect matrix allowing custom routing of all signals linking RLBs to each other, as well as to Block RAMs, multipliers, and BEs.

Functional logic is implemented exclusively in the RLBs, with the pipelining capability inherent in both the RLB and the SB playing a key role (as described in **"Technology Overview,"** on page 3) in performance enhancement.

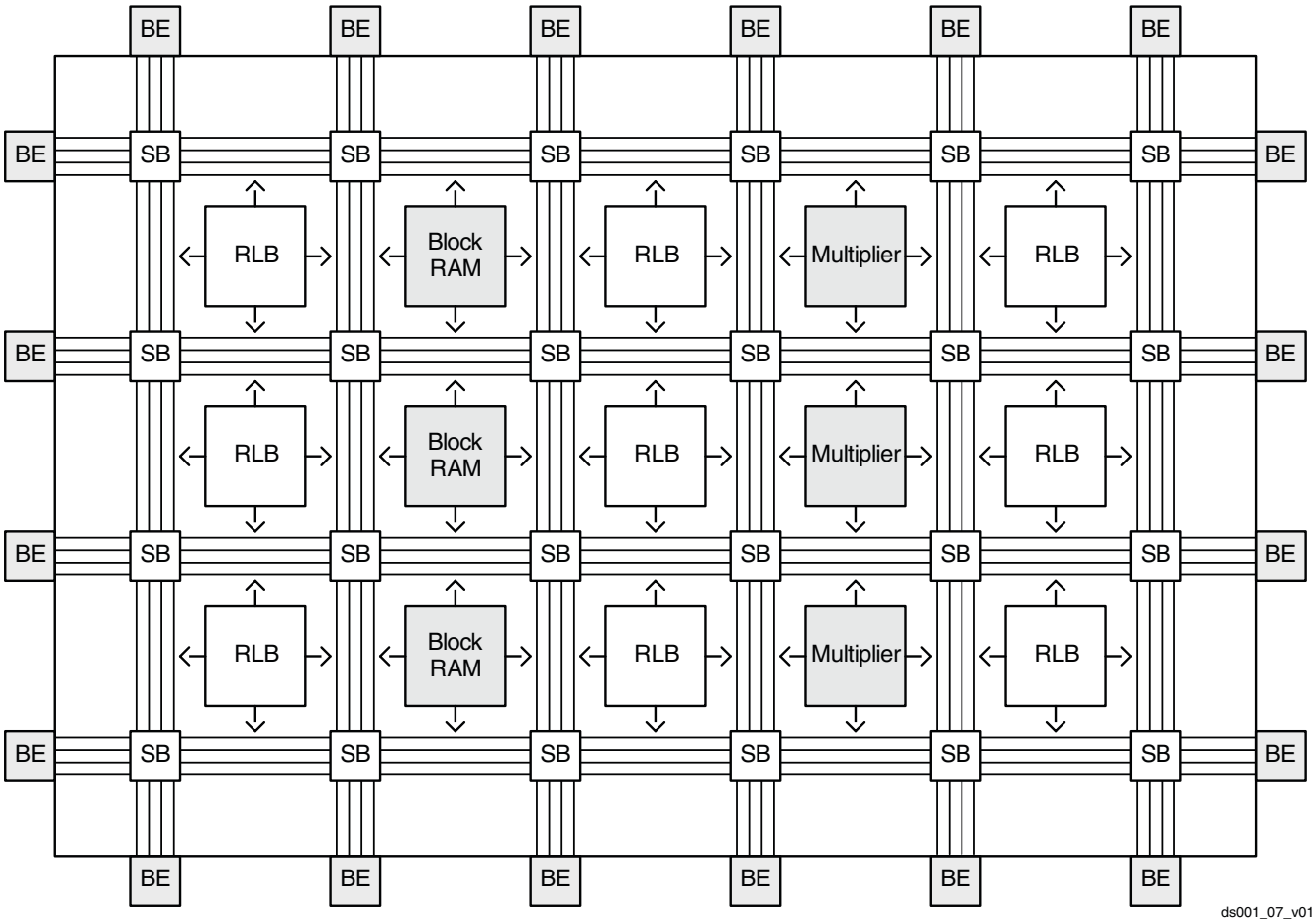


Figure 7: Logic Fabric Architecture (Conceptual – Sizes not to Scale)

The Reconfigurable Logic Block in Logic Mode

The RLB functions in one of two modes (never both at once):

- Logic mode (for implementation of combinatorial and sequential logic)
- LRAM mode (for implementation of small distributed memory elements)

LRAM mode allows each RLB to implement a two-port (W/R) 128-bit RAM block.

The RLB is illustrated in **Figure 8**. Essentially, an RLB consists of two pairs of Logic Clusters, one pair with a carry chain. This carry chain has its own RLB input and output to allow chaining to be cascaded through multiple RLBs.

Table 2: *RLB Resources*

Logic Clusters	FEs (4-Input LUTs)	Carry Chain	LRAM
4	8	2 × 2 bits each	128 bits

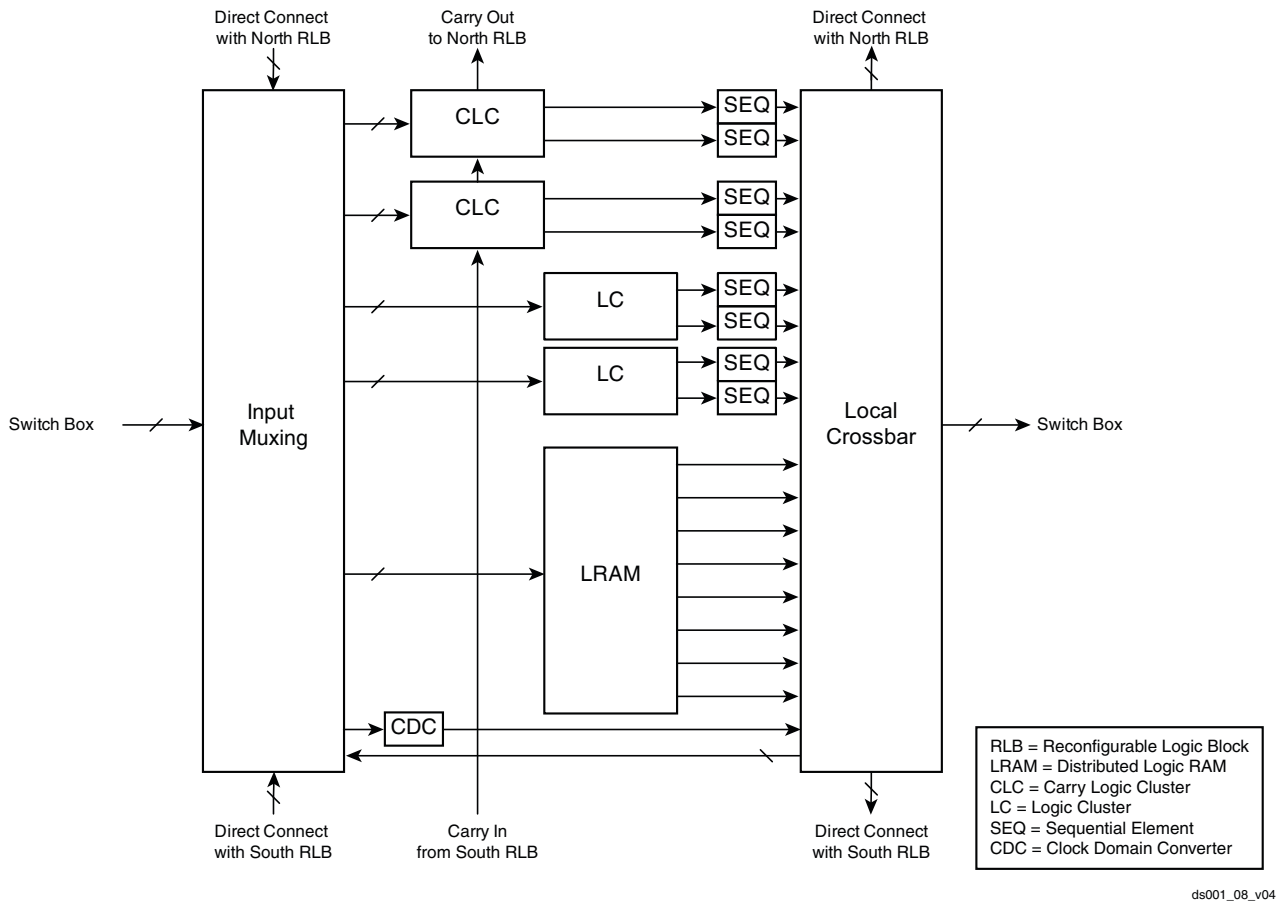


Figure 8: *The Reconfigurable Logic Block*

The Logic Cluster

The Logic Cluster (LC) is illustrated in **Figure 9**, page 9.

The standard 4-input LUT is the fundamental logic building block of the fabric. Each LUT has four inputs and a single output, and can be configured to make the output reflect any combinatorial (truth table) function of the inputs. The two four-input LUTs can implement a single five-input LUT function with the utilization of the MUX2. The MUX2 also enables the implementation of certain six, seven, eight and nine-input functions.

Each output of the logic cluster connects to a Sequential Element (SEQ), which is a Connection Element (CE) that can be initialized with a token. The SEQ elements with an initial token map to a flip-flop in the user RTL design. Of course, even when a flip-flop is not required, the CE provides a pipeline stage for performance optimization.

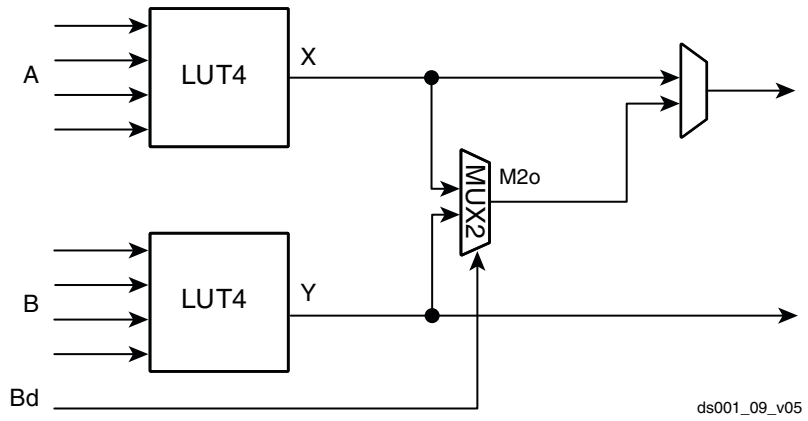


Figure 9: *The Logic Cluster*

The Carry Logic Cluster

The Carry Logic Cluster (CLC) is illustrated in **Figure 10**. All functionality possible with the standard Logic Cluster can also be implemented in a CLC. In addition, each cluster has the logic needed for generation of an arithmetic carry signal and propagation to the CLC to the north based on the RLB inputs and the carry in signal from its neighbor to the south

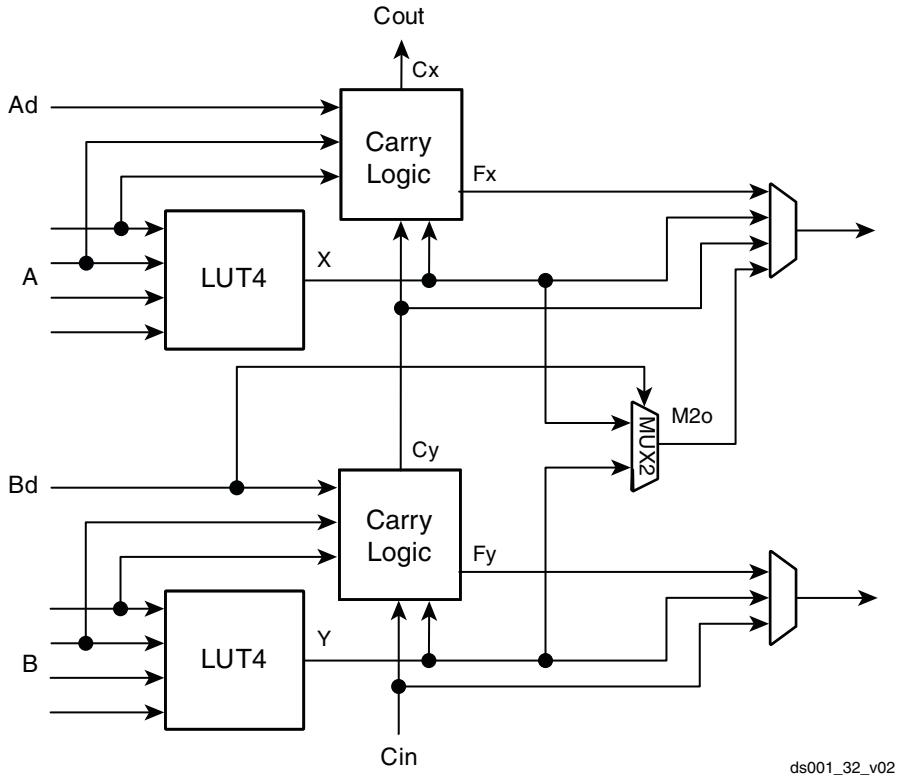


Figure 10: *Carry Logic Cluster*

The Clock Domain Converter

Each RLB contains one Clock Domain Converter (CDC). The CDC provides the interface between distinct clock domains -- blocks of circuitry operating at different clock rates. The CDC orchestrates the transfer of tokens from one domain (token source) to another domain (token sink). In completing this transfer, the CDC must violate the normal token-preservation behavior of picoPIPE elements. If the source domain is faster, the CDC must destroy tokens. Thus, it behaves similarly to a wire in a synchronous design between a fast-clocked flip-flop and a slow-clocked flip-flop. Alternatively, if the sink domain is faster, the CDC must repeat tokens — again behaving similarly to a wire in the corresponding synchronous circuit.

The Boundary Element

Figure 11 illustrates the Boundary Element in its proper context — transporting signals:

- From the Frame into the picoPIPE logic fabric (SAC)
- From the picoPIPE logic fabric to the Frame (ASC).

The BEs are essentially hybrid elements, exhibiting properties of both traditional design blocks and picoPIPE elements.

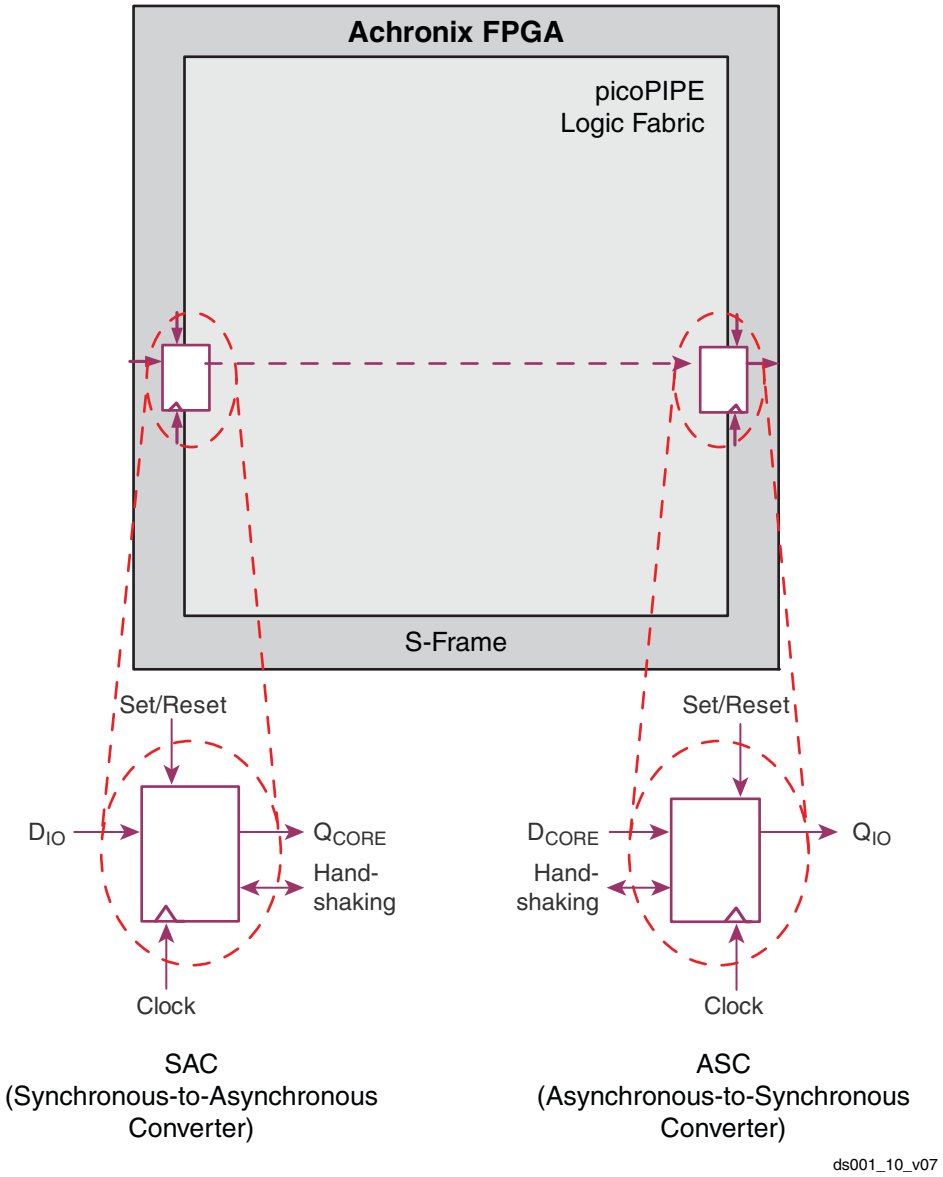


Figure 11: The Boundary Element (ASCs and SACs)

Flip-Flop Mode

In flip-flop mode, a SAC appears to the Frame as a standard flip-flop. On its output, it supports the picoPIPE handshaking protocol. Thus, a SAC's data output can be in any of the three picoPIPE states (Data High, Data Low, or No Data). Its state, like any flip-flop, depends on the clock and data inputs (from the Frame side), but it also depends on the picoPIPE handshaking state.

Similarly, an ASC appears as a standard flip-flop to the Frame, and as a pipeline stage (Connection Element) to the picoPIPE core.

Wire Mode

In wire mode, the SAC acts as an edge detector, passing a token into the picoPIPE only when there is a change. For asynchronous egress signals, an ASC appears as a latch, holding the result of the most recent transition.

Memory Resources

Block RAM

Basic Features

Each Speedster device features multiple instances of 18,432-bit block RAM deployed in vertical columns. The block RAM is supported in multiple organization modes with two fully independent read/write ports supported.

The key features (per Block RAM) are summarized in **Table 3**, and illustrated in **Figure 12**.

Table 3: *Block RAM Key Features*

Feature	Value
Block RAM Size	18 Kb
Organization	16K x 1, 8K x 2, 4K x 4, 2048 x 9, 2048 x 8, 1024 x 18, 1024 x 16, 512 x 36, 512 x 32
Performance	1.5 GHz
Physical Implementation	Columns throughout device
Number of Ports	Dual port (independent read and write)
Port Access	Synchronous
Contention Behavior	Read data undetermined; write successful

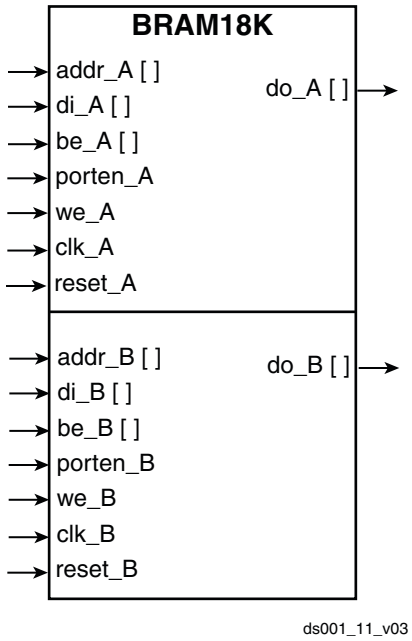


Figure 12: *Block RAM*

Organization

The organization of each block RAM port can be independently configured (the available organizations are listed in **Table 3**).

Note: *Access from opposite ports are not required to have the same organization; however, the number of total memory bits on each port must be the same.*

Multi-Port Features

Each port provides the following signals:

- Data in (up to 36)
- Data out (up to 36)
- Address (up to 14)
- Byte enable (4)
- Write enable
- Port enable
- Clock
- Reset (restore output latch to default state)

Error Correction

The 36-bit bus width provides the bit overhead for user implementation of parity or Error Correction Codes (ECC). Of course, these overhead bits can be used for other purposes as well: tagging, various control functions, etc.

Initialization and Reset

Initial content of the block RAMs is loaded during device configuration. On reset, the RAM contents are unchanged.

The initial state of the RAM read outputs is also loaded during device configuration. Unlike the RAM content, this default output state is restored on reset.

Logic RAM

Each RLB includes a 128-bit block of logic RAM (LRAM), organized as 16 words of 8 bits each. Access is through two independent 8-bit ports: one synchronous read port and one synchronous write port.

Table 4: *Logic RAM Key Features*

Feature	Value
Logic RAM size	128 bits
Organization	16 x 8
Performance	1.5 GHz
Physical Implementation	One block per RLB
Number of Ports	Dual port (one read, one write)
Port Access	Synchronous
Contention Behavior	Read data undetermined; write successful

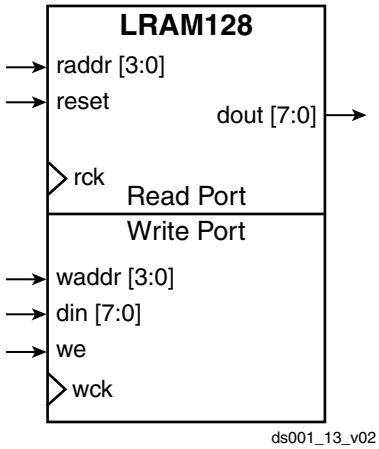


Figure 13: *Logic RAM*

Multipliers

Basic Features

Each Speedster device features multiple instances of multipliers deployed in vertical columns. The key features (per multiplier) are summarized in **Table 5**, and illustrated in **Figure 14** and **Figure 15**.

Each multiplier uses two's complement signed arithmetic.

Table 5: *Multiplier Features*

Feature	Value
Arithmetic Type	Two's complement (signed)
Performance	1.5 GHz
Multiplier Size	18 x 18
Dual Multiplier Mode	Two 9 x 9

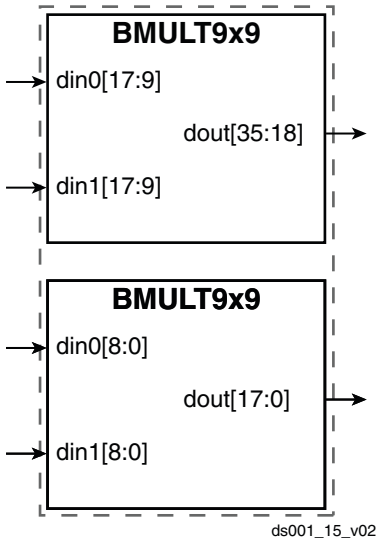


Figure 15: *Multiplier (Dual Mode)*

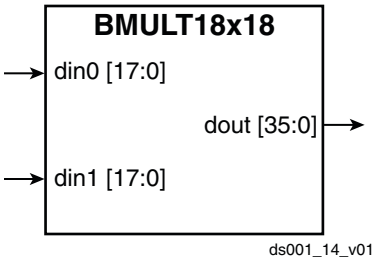


Figure 14: *Multiplier (Single Mode)*

Programmable I/Os

I/O Types: Summary

Speedster device I/Os come in five categories, as shown in **Table 6**.

Table 6: *I/O Types*

Full Name	Description	Count
Programmable I/O – Base Feature	• User programmable • Complies with wide range of I/O standards • Low to medium bit rates	Device/package dependent
Programmable I/O – Extended Feature	• User programmable • Complies with wide range of I/O standards • Low to medium bit rates • DLLs for input and output delay adjustments as required for advanced memory and datapath interfaces	12 × N where N = byte-lane count (device/package dependent)
SerDes I/O	• User programmable • Complies with wide range of SerDes-based standards • High bit rates	18 pins for a block of four SerDes (a Quad) composed of 16 data pins: (4 pins/lane × 4 lanes) + 2 reference clock pins (shared by 4 lanes)
Clock I/O	These I/O have the same capabilities as the Programmable I/O – Base Feature pins, with an additional capability of connecting to the **"Global Clock Generator"** in the corresponding corner.	24
Dedicated I/O	Reserved for device configuration and test	23
Power / Ground	Core power; I/O power; ground	Device/package dependent

Programmable I/Os: Supported Standards

Each programmable I/O can be configured to conform to any of a large number of I/O standards, both single-ended and differential, as summarized in **Table 7**, page 16. Each I/O can operate as an input, an output, or a bidirectional I/O (**Figure 16**). Of course, a differential signal consumes two I/Os, whereas a single-ended signal consumes only one.

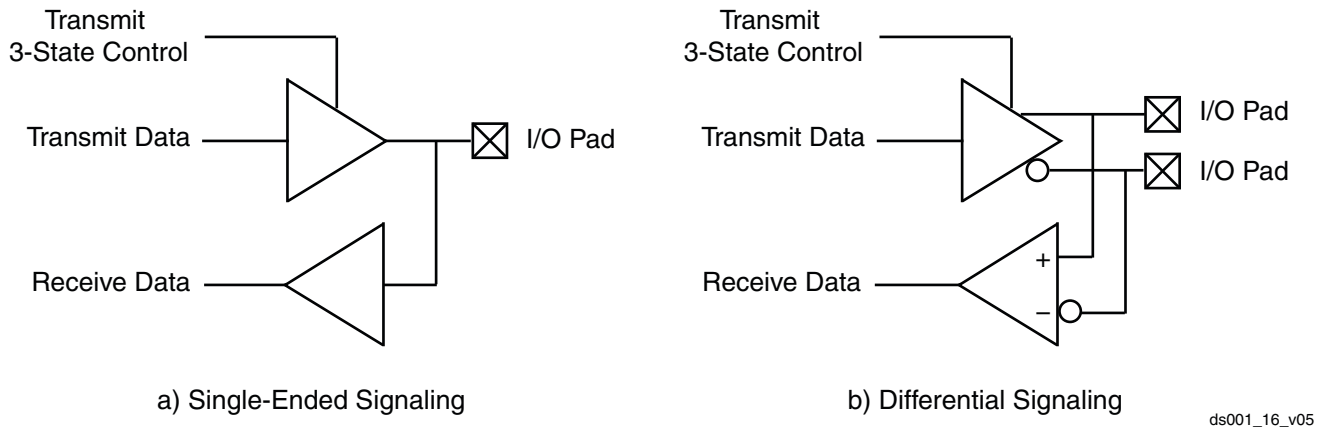


Figure 16: *Programmable I/Os*

Table 7: *Programmable I/O: Supported Standards*

Type		Volts	Class	Interface Applications and Standards		
				Standard	Max Clock Rate (MHz)	Max Data Rate (Mbps)
Single-Ended Differential	LVTTL	3.3V	–	• General Purpose • SDR and ZBT SDRAM	200	200
	LVCMOS	3.3V	–	General Purpose	200	200
	LVCMOS	2.5V	–		200	200
	LVCMOS	1.8V	–		200	200
	LVCMOS	1.5V	–		200	200
	HSTL	1.8V	Class I	QDR II SRAM / RLDRAM II	533	1066
	HSTL	1.8V	Class II		533	1066
	HSTL	1.5V	Class I	Memory and Switch Fabric	533	1066
	HSTL	1.5V	Class II		533	1066
	SSTL	2.5V	Class I	DDR SDRAM / RLDRAM II	200	400
	SSTL	2.5V	Class II		200	400
	SSTL	1.8V	Class I	DDR2 SDRAM / FCRAM II	400	800
	SSTL	1.8V	Class II		400	800
	SSTL	1.5V	Class II	DDR3 SDRAM	533	1066
	LVDS	2.5V	–	SPI4.2, SFI4.1	500	1000
	LDT	1.2V	–		400	800
	Differential HSTL	1.8V	Class I	QDRII SRAM / RLDRAM II	533	1066
	Differential HSTL	1.8V	Class II		533	1066
	Differential HSTL	1.5V	Class I	Memory and Switch Fabric	533	1066
	Differential HSTL	1.5V	Class II		533	1066
	Differential SSTL	1.8V	Class II	DDR 2 SDRAM	533	1066
	Differential SSTL	1.5V	Class II		533	1066
	Differential LVPECL (input only)	2.5V	–		500	

Programmable I/O Grouping: Banks and Byte Lanes

Programmable I/Os are deployed in banks. All I/Os within a bank must share:

- The same V_{DDO}
- The same V_{REF}
- The same R_{REF}s (used for controlled-impedance I/Os, as described in **"Programmable I/O Features (Common to All Banks),"** on page 19).

Figure 17 shows a conceptual floorplan of a device with ten banks. Clearly, the number of banks varies from device to device.

There are two bank types: Base Feature (BF) and Extended Feature (EF). BF banks are deployed on the bottom and top device edges and carry a variable I/O count. The BF banks are denoted as (BNW, BNE, BSW, and BSE). EF banks are deployed on the left and right device edges with 96 I/Os per bank, organized as eight byte lanes (12 I/Os each). Certain EF banks are available that have two sets of V_{DDO} and V_{REF} supplies, enabling the support for a by-72 DDR function while still allowing the other half of the EF bank to be powered for different V_{DDO} and V_{REF} levels. The bank only has a single compensation controller, but the half bank can be configured to select the bank's compensation controller or the adjacent bank's compensation controller (**Figure 18**, page 18).

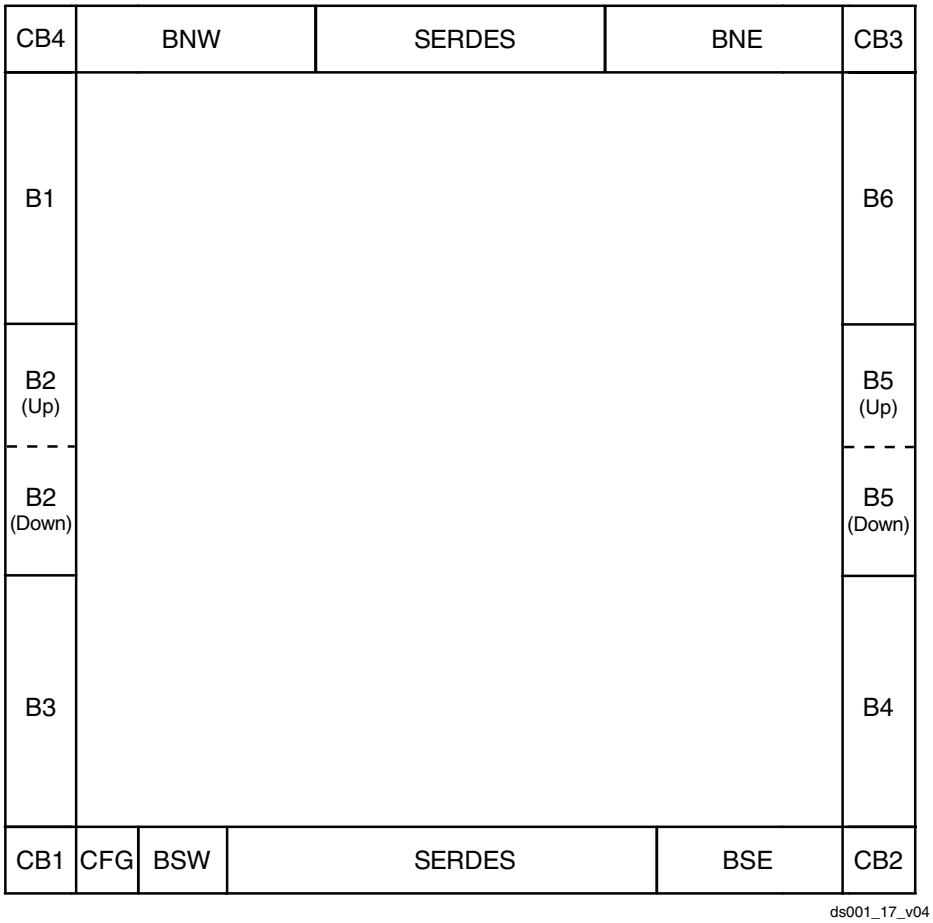
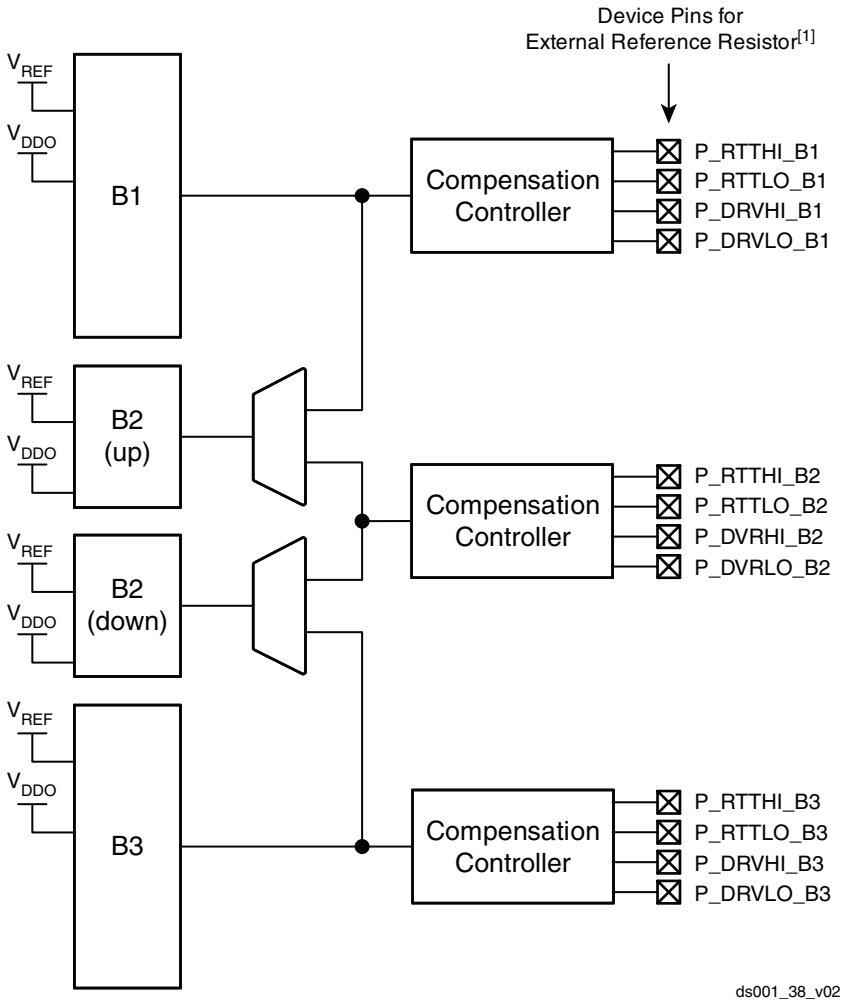


Figure 17: *I/O Banks (Bn = Bank #n; CBn = Clock Bank #n; CFG = Dedicated Configuration Bank)*



Notes:

1. See **Table 38**, page 38 for a complete description.
2. The same structure exists on the opposite side of the device for banks B4, B5, and B6. In that context B1 = B6, B2 = B5, and B3 = B4.

Figure 18: *Partially Splittable EF Banks*

Programmable I/O Features (Common to All Banks)

Both Basic and Extended Feature I/O types support the electrical specifications listed in **Table 7**, page 16, and the standards listed **Table 8**, page 23. In addition, further programmability is provided:

- Slew-rate control (LVTTL and LVCMOS)
- Drive-strength control (LVTTL and LVCMOS)
- 3-state control with pull-up/pull-down option
- Schmitt trigger option on the inputs
- Reference voltage V_{REF} (shared throughout an I/O bank)
- Impedance options
  - Differential termination option (100Ω)
  - Controlled impedance options
    - Output series impedance (R-value shared throughout an I/O bank)
    - Differential or single-ended input termination impedance (R-value shared throughout an I/O bank)

Resistance values for the controlled impedance features are set by external resistors tied to special pins designated within each bank for this purpose.

DDR Flip-Flops (All Banks)

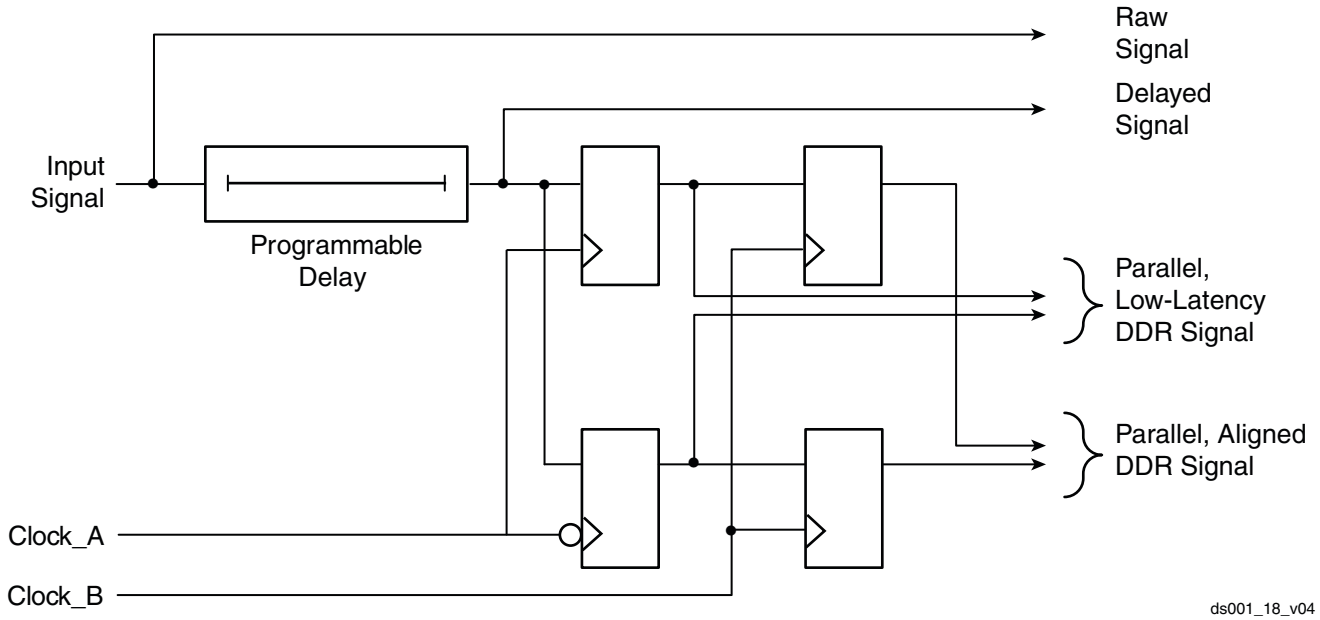
In order to support complex high-speed interfaces such as DDR2 and DDR3 SDRAM memories, a mechanism is needed to translate between the DDR clock domain and a single-edge clock domain. For this purpose, each I/O site includes flip-flops used as follows:

- Input (positive clock-edge)
- Input (negative clock-edge; DDR option)
- Output (positive clock-edge)
- Output (negative clock-edge; DDR option)
- Output 3-state (positive clock-edge)
- Output 3-state (negative clock-edge; DDR option)

In addition, there are extra resynchronization flip-flops to allow data busses crossing the core/frame boundary to share a common clock (as opposed to incoming DDR data, which, after capture, use staggered clocks):

- Input (resync for positive clock data)
- Input (resync for negative clock data)
- Output (resync for positive clock data)
- Output (resync for negative clock data)

Figure 19 and **Figure 20**, page 20 illustrate the use of these flip-flops for inputs for EF and BF banks; **Figure 21**, page 21 and **Figure 22**, page 22 show their use for outputs in EF and BF banks.



Notes:

1. Clock_A and Clock_B can share the same clock source.

Figure 19: *EF Bank Input Support Logic (Slave Delay and Flip-Flops)*

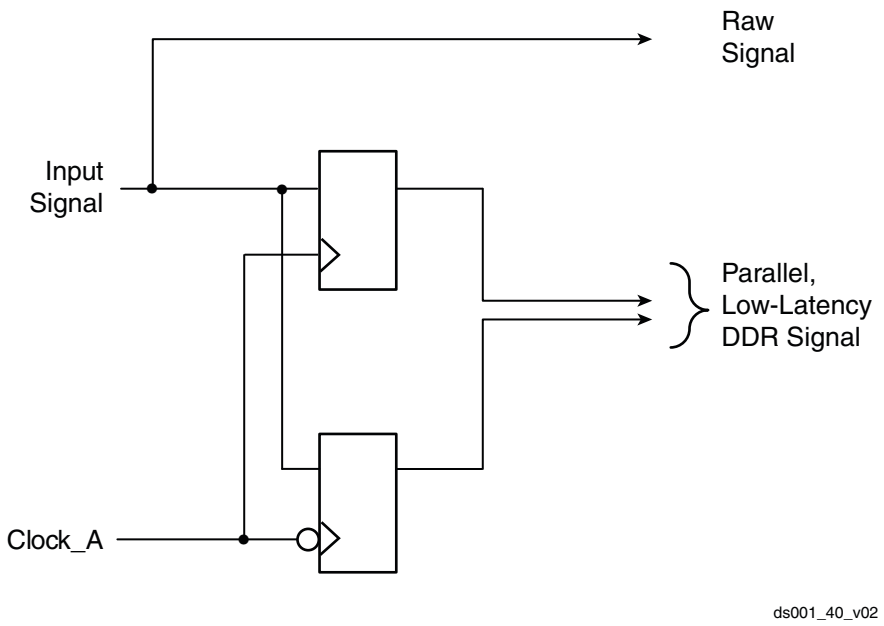


Figure 20: *BF Bank Input Logic*

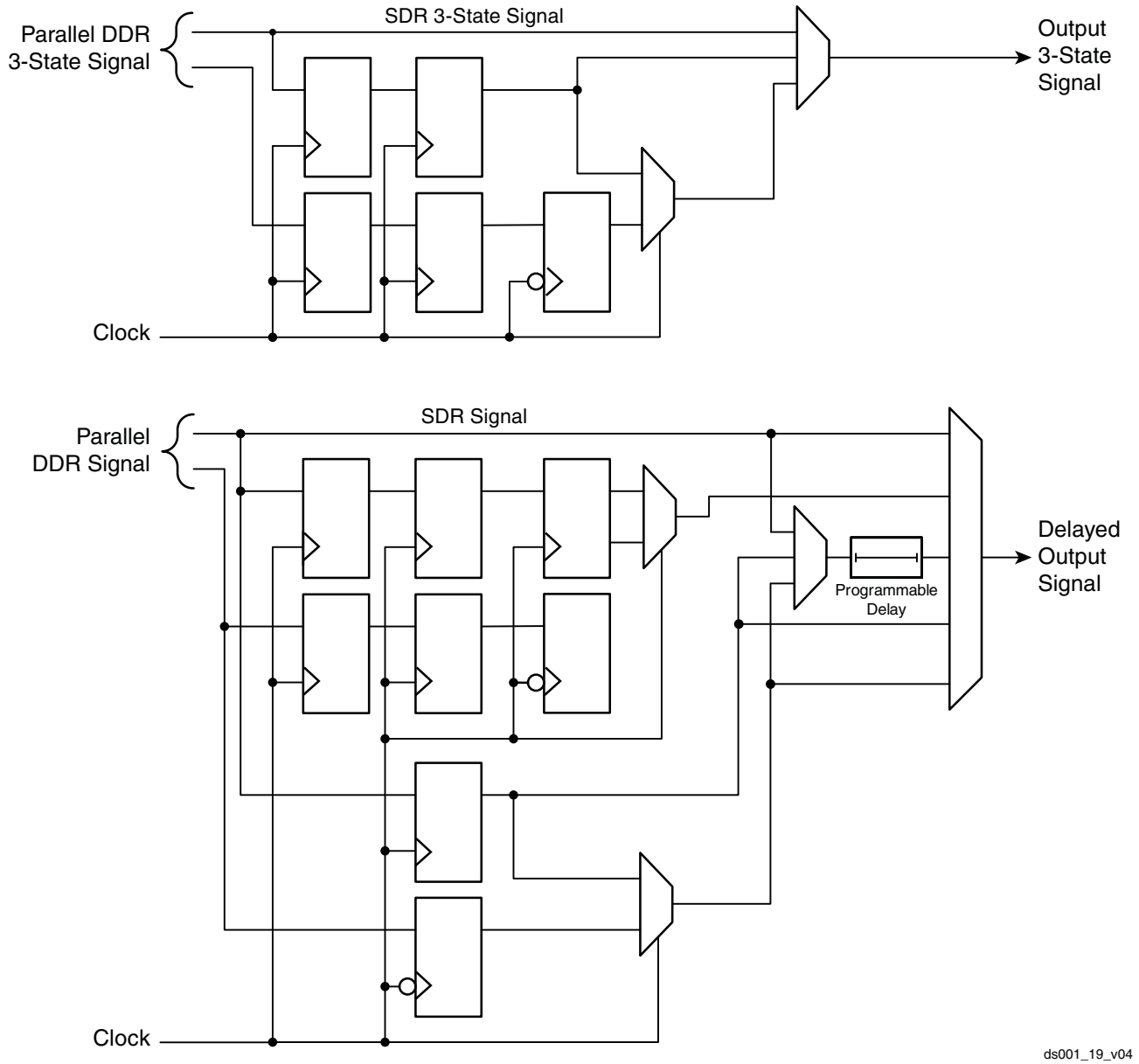


Figure 21: *EF Bank Output Support Logic (Slave Delay and Flip-Flops)*

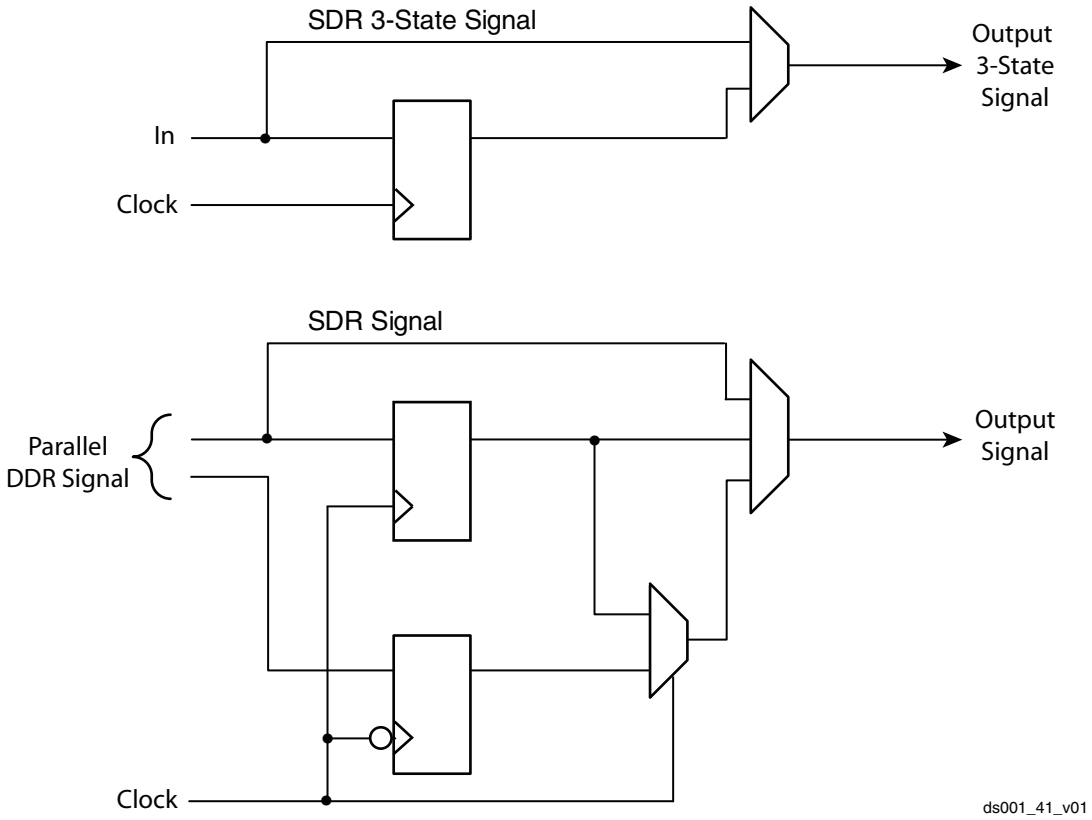


Figure 22: *BF Bank Output Logic*

Programmable I/O Support Logic

While individual I/Os are supported for control, and other general purpose uses, a key requirement for FPGA design is the ability to support the prevalent datapath and memory-interface bus standards. The key supported standards are listed in **Table 8**.

Support for these key interfaces requires compliance to I/O standards, as detailed in the previous sections. There are additional support structures required in order to implement these interfaces, especially at the specified bit rates.

For example, the DDR2 interface requires that the DQS (strobe) input be delayed by 90° before it is used to clock in receive data. This delay can be implemented by a DLL, which determines the appropriate delay, and then communicates it to the relevant input. The interface also requires that the input incorporates a delay line controlled by the DLL.

As a second example, the SPI4.2 interface requires both bit-level and word-level deskewing. Bit-level alignment (aligning the sampling clock-edge to the center of the data eye) requires a programmable delay for each data input, as well as a control mechanism. The DLL provides this control mechanism.

Programmable I/O Delay Lines (EF Banks Only)

Corresponding to each I/O is a programmable multi-tap delay line that can be used either for input or output. These delay lines are also illustrated in **Figure 19**, page 19 and **Figure 21**, page 21.

Common uses for the delay line are:

- **DDR2 interface**: to adjust, under the control of a DLL, the phase of the DQS signal (90° offset from DQ).
- **SPI4 interface:** to adjust, under the control of a deskew circuit, the phase of each input data lane, centering the sample clock in the data eye.

For purposes of determining the appropriate delay settings, the delay lines are typically slaved to a DLL master. Each byte-lane has its own master DLL.

Clock I/Os

Six dedicated clock inputs are provided in the corners of each Speedster device (24 clock inputs per device). These can be used in differential or single-ended mode for up to three differential clocks or up to six single-ended clocks per corner. Clocks in a single corner can be configured in the following combination of modes:

- Three differential
- Two differential plus two single-ended
- One differential plus four single-ended
- Six single-ended

Note: *Clocks are used only in the S-frame and Boundary Elements (SACs and ASCs) and are not used in the logic fabric.*

These clocks are derived from clock inputs either:

- Directly
- Indirectly, via a PLL
- Indirectly, via a DLL-controlled delay line

Configuration and Test I/Os

For a description of the operation of the configuration and test I/Os, see **"Clocking and Reset Resources."**

Table 8: *Key I/O Standards*

Specification/Standard		Speedster Device Support	BF	EF
Standard I/O Datapath Standards	GPIO	200 Mbps	✓	✓
	SPI4.2 (LVDS)	1000 Mbps		✓
	SFI4.1 (LVDS)	622 Mbps		✓
	XSBI (LVDS)	644 Mbps		✓
Standard I/O Memory Interface Standards	SDR SDRAM (SSTL 3.3V)	200 Mbps	✓	✓
	QDR SRAM (HSTL 1.5V)	400 Mbps		✓
	QDRII SRAM (HSTL 1.5V)	800 Mbps		✓
	RLDRAMII (HSTL 1.8V)	1066 Mbps		✓
	DDR1 SDRAM (SSTL 2.5V)	400 Mbps		✓
	DDR2 SDRAM (SSTL 1.8V)	800 Mbps		✓
	DDR3 SDRAM (SSTL 1.5V)	1066 Mbps		✓

Temperature Sensor

A temperature sensing diode is located in the lower left corner of the die, near the configuration logic. The anode and cathode for the internal temperature sensing diode are connected to two dedicated pins (TEMP_DIODE_P and TEMP_DIODE_N).

In a typical application, the user's circuitry can monitor temperature to use the result as a decision criterion, for example:

- Selectively disabling circuits to reduce power consumption.
- Delay enabling selected circuits until a specified condition is reached.

DC and Switching Characteristics

Recommended Operating Conditions

Table 9: *Recommended Operating Conditions*[1]

Symbol	Description	Commercial		Industrial		Units
		Min	Max	Min	Max	
T_J	Junction temperature	0	85	–40	100	°C
V_{DDL}	1.0V Internal supply for picoPIPE fabric	0.95	1.05	0.95	1.05	V
V_{DD}	1.0V Low voltage supply for S-Frame	0.95	1.05	0.95	1.05	V
PLL_V_{DDA}	1.0V Analog supply for PLL	0.95	1.05	0.95	1.05	V
V_{DDHA_10G}[2]	2.5V Analog supply for 10.3Gbps SerDes	2.375	2.625	2.375	2.625	V
V_{DDA_10G}[3]	1.0V Analog supply for 10.3Gbps SerDes	0.95	1.05	0.95	1.05	V
V_{DDT_10G}[4]	Transmit driver supply for 10.3Gbps SerDes	1.0	1.2	1.0	1.2	V
V_{DDHA_5G}[2]	2.5V Analog supply for 5Gbps SerDes	2.375	2.625	2.375	2.625	V
V_{DDA_5G}[3]	1.0V Analog supply for 5Gbps SerDes	0.95	1.05	0.95	1.05	V
V_{DDO_JTAG}	Supply voltage for JTAG interface	2.5	3.3	2.5	3.3	V
V_{DDO_CFG}	Supply voltage for configuration bank	2.5	3.3	2.5	3.3	V
V_{DDQ}[5]	2.5V Supply voltage for eFuse programming	2.25	2.75	2.25	2.75	V
V_{DDO_CB}	Supply voltage for clock banks	1.14	3.6	1.14	3.6	V
V_{DDO_B}	Supply voltage for I/O banks	1.14	3.6	1.14	3.6	V
$V_{DDO\_B\_DOWN}$	Supply voltage for I/O banks	1.14	3.6	1.14	3.6	V
$V_{DDO\_B\_UP}$	Supply voltage for I/O banks	1.14	3.6	1.14	3.6	V

Notes:

1. All voltages are specified with respect to V_{SS} unless otherwise specified.
2. Should have no more than 50 mV peak-to-peak AC power supply noise superimposed on the 2.5V nominal DC value.
3. Should have no more than 20 mV peak-to-peak AC power supply noise superimposed on the 1.0V nominal DC value.
4. The setting of this supply to 1.2V or 1.0V depends on the interface standard mode that the quad is configured for.
5. This pin should be kept Low except when programming the AES encryption keys.

Absolute Maximum Ratings

Table 10: *Absolute Maximum Ratings*

Symbol	Description	Limits	Units
T_J	Junction temperature	125	°C
T_{STG}	Storage Temperature		°C
V_{DDL}	1.0V Internal supply for picoPIPE fabric		V
V_{DD}	1.0V Low voltage supply for S-Frame		V
PLL_V_{DDA}	1.0V Analog supply for PLL		V
V_{DDHA_10G}	2.5V Analog supply for 10.3Gbps SerDes		V
V_{DDA_10G}	1.0V Analog supply for 10.3Gbps SerDes		V
V_{DDT_10G}	Transmit driver supply for 10.3Gbps SerDes		V
V_{DDHA_5G}	2.5V Analog supply for 5Gbps SerDes		V
V_{DDA_5G}	1.0V Analog supply for 5Gbps SerDes		V
V_{DDO_JTAG}	Supply voltage for JTAG interface		V
V_{DDO_CFG}	Supply voltage for configuration bank		V
V_{DDQ}	2.5V Supply voltage for eFuse programming		V
V_{DDO_CB}	Supply voltage for clock banks		V
V_{DDO_B}	Supply voltage for I/O banks		V
$V_{DDO\_B\_DOWN}$	Supply voltage for I/O banks		V
$V_{DDO\_B\_UP}$	Supply voltage for I/O banks		V
V_{IN}	I/O input voltage		V

Notes:

1. Reliability of the device may be affected if exposed to absolute maximum limits for extended period of time.
2. The limits in this table are stress limits only and does not imply functionality of the device.

I/O Electrical Specifications

SSTL3

Table 11: *SSTL3 General Specifications*

Symbol	Description	Min	Nom	Max	Units
V_{DDO}	Output supply voltage relative to GND	1.62	1.8	1.98	V
V_{REF}	Output reference voltage	0.81	0.9	0.99	V
V_{TT}	Termination voltage	0.81	0.9	0.99	V

Table 12: *SSTL3 DC Specifications*

Symbol	Description	Specification		Units
		Min	Max	
$V_{IH(DC)}$	High DC input voltage	V_{REF} + 0.2	V_{DDO} + 0.3	V
$V_{IL(DC)}$	Low DC input voltage	–0.3	V_{REF} – 0.2	V
I_{DD}	Static Supply current			mA
Class I Output Buffer R_T = 50Ω, R_S = 25Ω				
I_{OH}	Output minimum source current(1)	–8		mA
I_{OL}	Output minimum sink current(2)	8		mA
Class II Output Buffer R_T = 25Ω, R_S = 25Ω				
I_{OH}	Output minimum source current(3)	–16		mA
I_{OL}	Output minimum sink current(4)	16		mA

Notes:
1. V_{DDO} = 3.0V, $V_{OUT(MIN)}$ = 1.9V, V_{TT} = 1.3V
2. V_{DDO} = 3.0V, $V_{OUT(MIN)}$ = 2.1V, V_{TT} = 1.3V
3. V_{DDO} = 3.0V, $V_{OUT(MAX)}$) = 0.7V, V_{TT} = 1.3V
4. V_{DDO} = 3.0V, $V_{OUT(MAX)}$ = 0.5V, V_{TT} = 1.3V

Table 13: *SSTL3 AC Specifications*

Symbol	Description	Specification		Units
		Min	Max	
$V_{IH(AC)}$	High AC input voltage	V_{REF} + 0.4		V
$V_{IL(AC)}$	Low AC input voltage		V_{REF} – 0.4	V
Class I Output Buffer R_T = 50Ω, R_S = 25Ω				
$V_{OH(AC)}$	High AC output voltage(1)	V_{TT} + 0.6		V
$V_{OL(AC)}$	Low AC output voltage(1)		V_{TT} – 0.6	V
Class II Output Buffer R_T = 25Ω, R_S = 25Ω				
$V_{OH(AC)}$	High AC output voltage(2)	V_{TT} + 0.8		V
$V_{OL(AC)}$	Low AC output voltage(2)		V_{TT} – 0.8	V

Notes:
1. Tested with R_T = 50Ω, R_S = 25Ω, C_{LOAD} = 30 pF (JESD 8-8 Figure 3.1).
2. Tested with R_T = 25Ω, R_S = 25Ω, C_{LOAD} = 30 pF (JESD 8-8 Figure 3.2).

SSTL2

Table 14: *SSTL2 General Specifications*

Symbol	Description	Min	Nom	Max	Units
V_{DDO}	Output supply voltage relative to GND	2.3	2.5	2.7	V
V_{REF}	Output reference voltage	1.15	1.25	1.35	V
V_{TT}	Termination voltage	1.11	1.25	1.39	V

Table 15: *SSTL2 DC Specifications*

Symbol	Description	Specification		Units
		Min	Max	
$V_{IH(DC)}$	High DC input voltage	V_{REF} + 0.18	V_{DDO} + 0.3	V
$V_{IL(DC)}$	Low DC input voltage	–0.3	V_{REF} – 0.18	V
I_{DD}	Static Supply current			mA
Class I Output Buffer R_T = 50Ω, R_S = 25Ω				
I_{OH}	Output minimum source current(1)	–8.1		mA
I_{OL}	Output minimum sink current(2)	8.1		mA
Class II Output Buffer R_T = 25Ω, R_S = 25Ω				
I_{OH}	Output minimum source current(3)	–16.2		mA
I_{OL}	Output minimum sink current(4)	16.2		mA

Notes:
1. V_{DDO} = 2.3V, $V_{OUT(MIN)}$ = 1.74V, V_{TT} = 1.13V
2. V_{DDO} = 2.3V, $V_{OUT(MIN)}$ = 0.56V, V_{TT} = 1.17V
3. V_{DDO} = 2.3V, $V_{OUT(MAX)}$ = 1.93V, V_{TT} = 1.13V
4. V_{DDO} = 2.3V, $V_{OUT(MAX)}$ = 0.36V, V_{TT} = 1.17V

Table 16: *SSTL2 AC Specifications*

Symbol	Description	Specification		Units
		Min	Max	
$V_{IH(AC)}$	High AC input voltage	V_{REF} + 0.4		V
$V_{IL(AC)}$	Low AC input voltage		V_{REF} – 0.4	V
Class I Output Buffer R_T = 50Ω, R_S = 25Ω				
$V_{OH(AC)}$	High AC output voltage(1)	V_{TT} + 0.57		V
$V_{OL(AC)}$	Low AC output voltage(1)		V_{TT} – 0.57	V
Class II Output Buffer R_T = 25Ω, R_S = 25Ω				
$V_{OH(AC)}$	High AC output voltage(2)	V_{TT} + 0.76		V
$V_{OL(AC)}$	Low AC output voltage(2)		V_{TT} – 0.76	V

Notes:
1. Tested with R_T = 50Ω, R_S = 25Ω, C_{LOAD} = 30 pF (JESD 8-8 Figure 3.1).
2. Tested with R_T = 25Ω, R_S = 25Ω, C_{LOAD} = 30 pF (JESD 8-8 Figure 3.2).

SSTL18

Table 17: *SSTL18 General Specifications*

Symbol	Description	Min	Nom	Max	Units
V_{DDO}	Output supply voltage relative to GND	1.62	1.8	1.98	V
V_{REF}	Output reference voltage	0.81	0.9	0.99	V
V_{TT}	Termination voltage	0.81	0.9	0.99	V

Table 18: *SSTL18 DC Specifications*

Symbol	Description	Specification		Units
		Min	Max	
$V_{IH(DC)}$	High DC input voltage	V_{REF} + 0.125	V_{DDO} + 0.3	V
$V_{IL(DC)}$	Low DC input voltage	–0.3	V_{REF} – 0.125	V
I_{DD}	Static Supply current			mA
Output Buffer R_T = 25Ω, R_S = 20Ω				
I_{OH}	Output minimum source current(1)	–13.4		mA
I_{OL}	Output minimum sink current(1)	13.4		mA

Notes:

1. V_{DDO} = 1.7V, $V_{OUT(MIN)}$ = 833 mV, V_{TT} = 40 mV

Table 19: *SSTL18 AC Specifications*

Symbol	Description	Specification		Units
		Min	Max	
$V_{IH(AC)}$	High AC input voltage	V_{REF} + 0.25		V
$V_{IL(AC)}$	Low AC input voltage		V_{REF} – 0.25	V
Class I Output Buffer R_T = 50Ω, R_S = 25Ω				
$V_{OH(AC)}$	High AC output voltage(1)	V_{TT} + 0.57		V
$V_{OL(AC)}$	Low AC output voltage(1)		V_{TT} – 0.57	V
Class II Output Buffer R_T = 25Ω, R_S = 25Ω				
$V_{OH(AC)}$	High AC output voltage(2)	V_{TT} + 0.76		V
$V_{OL(AC)}$	Low AC output voltage(2)		V_{TT} – 0.76	V

Notes:

1. Tested with R_T = 50Ω, R_S = 20Ω, C_{LOAD} = 5 pF (JESD 8-15 Figure 4).
2. Tested with R_T = 50Ω, R_S = 20Ω, C_{LOAD} = 5 pF (JESD 8-15 Figure 4).

HSTL18

Table 20: *HSTL18 General Specifications*

Symbol	Description	Min	Nom	Max	Units
V_{DDO}	Output supply voltage relative to GND	1.7	1.8	1.9	V
V_{REF}	Output reference voltage	0.8	0.9	1.1	V
V_{TT}(1)	Termination voltage for Class I and II outputs		$V_{DDO}/2$		V

Notes:

1. V_{TT} must track V_{REF} of receiving device.

Table 21: *HSTL18 DC Specifications*

Symbol	Description	Condition	Specification		Units
			Min	Max	
V_{IH}	High input voltage(1)	Single-ended	V_{REF} + 0.1	V_{DDO} + 0.3	V
V_{IL}	Low input voltage(1)	Single-ended	–0.3	V_{REF} – 0.1	V
V_{OH}	High output voltage				
	Class I buffer	I_{OH} = 8 mA	V_{DDO} – 0.4		V
	Class II buffer	I_{OH} = 16 mA	V_{DDO} – 0.4		V
V_{OL}	Low output voltage				
	Class I buffer	I_{OL} = –8 mA		0.4	V
	Class II buffer	I_{OL} = –16 mA		0.4	V
I_{DD}	Static Supply current				mA

Notes:

1. Input buffer is single-ended only.

HSTL15

Table 22: *HSTL15 General Specifications*

Symbol	Description	Min	Nom	Max	Units
V_{DDO}	Output supply voltage relative to GND	1.4	1.5	1.6	V
V_{REF}	Output reference voltage	0.68	0.75	0.9	V
V_{TT}(1)	Termination voltage for Class I and II outputs		$V_{DDO}/2$		V

Notes:

1. V_{TT} must track V_{REF} of receiving device.

Table 23: *HSTL15 DC Specifications*

Symbol	Description	Condition	Specification		Units
			Min	Max	
V_{IH}	High input voltage(1)	Single-ended	V_{REF} + 0.1	V_{DDO} + 0.3	V
V_{IL}	Low input voltage(1)	Single- ended	–0.3	V_{REF} – 0.1	V
V_{OH}	High output voltage				
	Class I buffer	I_{OH} = 8 mA	V_{DDO} – 0.4		V
	Class II buffer	I_{OH} = 16 mA	V_{DDO} – 0.4		V
V_{OL}	Low output voltage				
	Class I buffer	I_{OL} = –8 mA		0.4	V
	Class II buffer	I_{OL} = –16 mA		0.4	V
I_{DD}	Static Supply current				mA

Notes:

1. Input buffer is single-ended only.

LVTTL

Table 24: *LVTTL Supply Voltages*

Symbol	Parameter	Min	Nom	Max	Units
V_{DDO}	Output supply voltage relative to GND	3	3.3	3.6	V

Table 25: *LVTTL DC Specifications*

Symbol	Description	Condition	Specification		Units
			Min	Max	
V_{IH}	Input High Voltage	$V_{OUT} \geq V_{OH}$	2	3.6	V
V_{IL}	Input Low Voltage	$V_{OUT} \leq V_{OL}$	–0.3	0.8	V
V_{OH}	Output High Voltage	$I_{OH} = -4mA$	2.4		V
		$I_{OH} = -6mA$	2.4		V
		$I_{OH} = -8mA$	2.4		V
		$I_{OH} = -12mA$	2.4		V
		$I_{OH} = -16mA$	2.4		V
		$I_{OH} = -20mA$	2.4		V
		$I_{OH} = -24mA$	2.4		V
V_{OL}	Output Low Voltage	$I_{OL} = 4mA$		0.4	V
		$I_{OL} = 6mA$		0.4	V
		$I_{OL} = 8mA$		0.4	V
		$I_{OL} = 12mA$		0.4	V
		$I_{OL} = 16mA$		0.4	V
		$I_{OL} = 20mA$		0.4	V
		$I_{OL} = 24mA$		0.4	V

LVCMOS25

Table 26: *LVCMOS25 Supply Voltages*

Symbol	Parameter	Min	Nom	Max	Units
V_{DDO}	Output supply voltage relative to GND	2.3	2.5	2.7	V

Table 27: *LVCMOS25 DC Specifications*

Symbol	Description	Condition	Specification		Units
			Min	Max	
V_{IH}	Input High Voltage	$V_{OUT} \geq V_{OH}$	1.7	V_{DDO} + 0.3	V
V_{IL}	Input Low Voltage	$V_{OUT} \leq V_{OL}$	–0.3	0.7	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	V_{DDO}(min) – 0.4		V
		I_{OH} = –6mA	V_{DDO}(min) – 0.4		V
		I_{OH} = –8mA	V_{DDO}(min) – 0.4		V
		I_{OH} = –12mA	V_{DDO}(min) – 0.4		V
		I_{OH} = –16mA	V_{DDO}(min) – 0.4		V
		I_{OH} = –20mA	V_{DDO}(min) – 0.4		V
V_{OL}	Output Low Voltage	I_{OL} = 4mA		0.4	V
		I_{OL} = 6mA		0.4	V
		I_{OL} = 8mA		0.4	V
		I_{OL} = 12mA		0.4	V
		I_{OL} = 16mA		0.4	V
		I_{OL} = 20mA		0.4	V

LVCMOS18

Table 28: *LVCMOS18 Supply Voltage*

Symbol	Parameter	Min	Nom	Max	Units
V_{DDO}	Output supply voltage relative to GND	1.65	1.8	1.95	V

Table 29: *LMCMOS18 DC Specifications*

Symbol	Description	Condition	Specification		Units
			Min	Max	
V_{IH}	Input High Voltage	$V_{OUT} \geq V_{OH}$	0.65 V_{DDO}	V_{DDO} + 0.3	V
V_{IL}	Input Low Voltage	$V_{OUT} \leq V_{OL}$	–0.3	0.35 V_{DDO}	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	V_{DDO}(min) – 0.4		V
		I_{OH} = –6mA	V_{DDO}(min) – 0.4		V
		I_{OH} = –8mA	V_{DDO}(min) – 0.4		V
		I_{OH} = –12mA	V_{DDO}(min) – 0.4		V
		I_{OH} = –16mA	V_{DDO}(min) – 0.4		V
V_{OL}	Output Low Voltage	I_{OL} = 4mA		0.4	V
		I_{OL} = 6mA		0.4	V
		I_{OL} = 8mA		0.4	V
		I_{OL} = 12mA		0.4	V
		I_{OL} = 16mA		0.4	V

LVCMOS15

Table 30: *LVCMOS15 Supply Voltages*

Symbol	Parameter	Min	Nom	Max	Units
V_{DDO}	Output supply voltage relative to GND	1.4	1.5	1.6	V

Table 31: *LVCMOS15 DC Specifications*

Symbol	Description	Condition	Specification		Units
			Min	Max	
V_{IH}	Input High Voltage	$V_{OUT} \geq V_{OH}$	0.65 V_{DDO}	V_{DDO} + 0.3	V
V_{IL}	Input Low Voltage	$V_{OUT} \leq V_{OL}$	–0.3	0.35 V_{DDO}	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	V_{DDO}(min) – 0.4		V
		I_{OH} = –6mA	V_{DDO}(min) – 0.4		V
		I_{OH} = –8mA	V_{DDO}(min) – 0.4		V
		I_{OH} = –12mA	V_{DDO}(min) – 0.4		V
		I_{OH} = –16mA	V_{DDO}(min) – 0.4		V
V_{OL}	Output Low Voltage	I_{OL} = 4mA		0.4	V
		I_{OL} = 6mA		0.4	V
		I_{OL} = 8mA		0.4	V
		I_{OL} = 12mA		0.4	V
		I_{OL} = 16mA		0.4	V

LVDS

Table 32: *LVDS Supply Voltages*

Symbol	Description	Min	Max	Units
V_{DDO}	I/O supply voltage	2.5 – 5%	2.5 + 5%	V
V_{DD}	Core supply voltage	1.0	1.2	V

Table 33: *LVDS DC Specifications*

Symbol	Description	Conditions	Min	Max	Units
Receiver					
V_I	Input voltage range, V_{IA}/V_{IB}		0	2.4	V
V_{IDTH}	Input differential threshold		–100	+100	mV
V_{ID}	Input differential voltage range		100	1200	mV
V_{HYST}	Input differential hysteresis (V_{IDTHH}–V_{IDTHL})		–	25	mV
R_{IN}	Receiver diff input impedance	Worst case: SS, 0°C	90	110	Ω
Driver					
V_{OH}	Output voltage High, V_{OA}/V_{OB}	R_{LOAD} = 100Ω ± 1%	–	1.475	V
V_{OL}	Output voltage Low, V_{OA}/V_{OB}		925	–	mV
$\|V_{OD}\|$	Output differential voltage		250	400	mV
V_{OS}	Output offset voltage		1.125	1.375	V
R_O	Output impedance, single ended	V_{CM} = 1.0V and 1.4V	40	140	Ω
ΔR_O	R_O mismatch between A and B		–	10	%
$\Delta \|V_{OD}\|$	Change in $\|V_{OD}\|$ between 0 and 1	R_{LOAD} = 100Ω ± 1%	–	25	mV
$\Delta \|V_{OS}\|$	Change in $\|V_{OS}\|\|$ between 0 and 1		–	25	mV
I_{SA}/I_{SB}	Output Current	Driver shorted to ground	–	40	mA
I_{SAB}	Output Current	Drivers shorted together	–	12	mA
I_{XA}/I_{XB}	Power-off output leakage		–	10	mA
VV_{REF}	Reference supply voltage		–	–	
I_{VREF}	Reference leakage current		–1	1	mA

Table 34: *LVDS AC Specifications*

Symbol	Description	Conditions	Min	Max	Units
Receiver					
T_{PD}	Propagation delay		–	1	ns
T_{SKEW}	Skew tolerable at receiver input to meet T_{SU}/T_{HOLD}		–	600	ps
Driver					
Clock	Clock signal duty cycle		45	55	%
T_{FALL}	V_{OD} fall time, 20–80%	R_{LOAD} = 100Ω ± 1%	300	500	ps
T_{RISE}	V_{OD} rise time, 20–80%		300	500	ps
T_{SKEW1}	$\|TP_{HLA} – TP_{LHB}\|$ or $\|TP_{HLB} – TP_{LHA}\|$, differential skew	Any differential pair on package	–	50	ps
T_{SKEW2}	$\|TP_{DIFF[M]} – TP_{DIFF[N]}\|$ channel-to-channel skew	Any two signals on package	–	100	ps

LVPECL

Table 35: *LVPECL Supply Voltages*

Symbol	Description	Min	Max	Units
V_{DDO}	I/O supply voltage	2.5	3.3	V
V_{DD}	Core supply voltage		1.2	V

Table 36: *LVPECL DC Specifications*

Symbol	Description	Min	Max	Units
Receiver				
V_{IHD}	Differential input High voltage	1.2	V_{DDO}	V
V_{ILD}	Differential input Low voltage	0	V_{DDO} – 0.2	V
V_{ICM}	Input common-mode voltage	0.6	V_{DDO} – 0.1	V
V_{ID}	Input differential voltage range	200	V_{DDO} – 500	mV
R_{IN}	Receiver differential input impedance	90	110	Ω

I/O Leakage

Table 37: *I/O Tri-state Leakage Currents*

Symbol	Description	Condition	Min	Max	Units
I_{OZ}	Off-state Leakage Current(1)	$3.0 \leq V_{DDO} \leq 3.6$			µA
		$2.3 \leq V_{DDO} \leq 2.7$	–6	+6	µA
		$1.62 \leq V_{DDO} \leq 1.986$			µA
		$1.4 \leq V_{DDO} \leq 1.6$			µA
I_{OZK}	Off-state Leakage Current with Bus Keeper enabled(1)	$3.0 \leq V_{DDO} \leq 3.6$			µA
		$2.3 \leq V_{DDO} \leq 2.7$	–32	+32	µA
		$1.62 \leq V_{DDO} \leq 1.986$			µA
		$1.4 \leq V_{DDO} \leq 1.6$			µA

Notes:

1. Includes input leakage current

Compensation and Termination

The EF and CB banks in Speedster devices have compensation controller blocks to provide accurate process, voltage, and temperature compensated driver output and receiver termination impedances. Some I/O standards require termination or compensation resistors for proper operation. **Table 38** lists the external resistor values needed for the driver compensation on DRV_{HI}/DRV_{LO}, and **Table 39** lists the external resistor values for RTT termination compensation on RTT_{HI}/RTT_{LO}.

Note: *The resistor on DRV_{HI}/RTT_{HI} is connected to V_{SS}, and the resistor on DRV_{LO}/RTT_{LO} is connected to V_{DDO}.*

Table 38: *Compensation Resistor Values*

Standard	Resistor Value
HSTL18 Class I	78Ω
HSTL18 Class II	44Ω
DDR3 (SSTL15)	60Ω
DDR2 Class I (SSTL18)	68Ω
DDR2 Class II	38Ω
DDR1 Class I	78Ω
DDR1 Class II	44Ω

Table 39: *Termination Resistor Values(1)*

Resistor Value	Resulting Termination
300Ω	150/75Ω
240Ω	120/60Ω
200Ω	100/50Ω

Notes:

1. The two different values of termination resistance for the same value of external compensation resistor connected to RTT_{HI}/RTT_{LO} is set via a configuration bit.

SerDes

Overview

All members of the Speedster family include embedded SerDes, typically used to implement protocols running at greater than 1 Gbps per lane. Each SerDes can be used for:

- Chip-to-chip signaling
- Backplane signaling
- Line signaling (coax, twisted pair, etc.)

As clocking is embedded in the data stream, the SerDes receiver must extract the clock from the stream. This activity is referred to as clock and data recovery (CDR). For signaling across a backplane (or other impaired medium) at about 5 Gbps or greater, decision feedback equalization (DFE) may be required.

Two SerDes types are found in the Speedster family: a 5G SerDes, and a 10.3G SerDes. The 10.3G SerDes supports all the same features as the 5G SerDes, with the addition of:

- Operation up to 10.375 Gbps per lane
- DFE support for high-speed operation over impaired channels
- Support for coding schemes other than 8B/10B (including un-encoded traffic)
- More complete set of programmable PCS features.

Block diagrams of the transmit and receive sections respectively are shown in **Figure 23** and **Figure 24**.

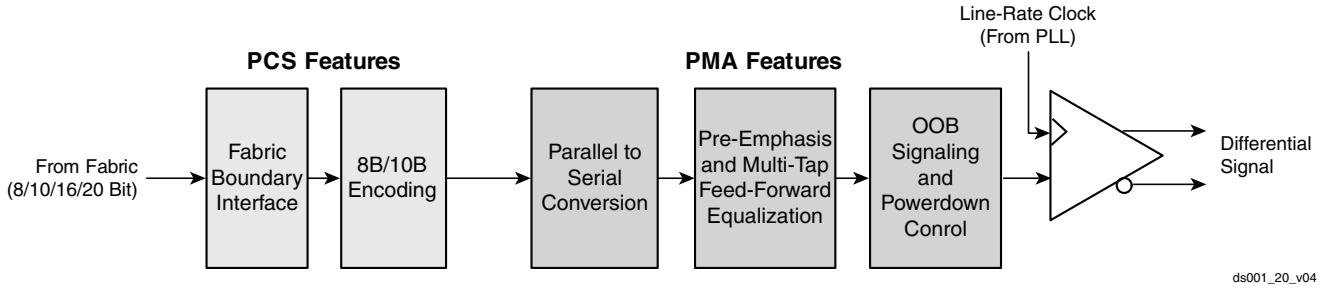


Figure 23: *10.3G SerDes – Transmit Section*

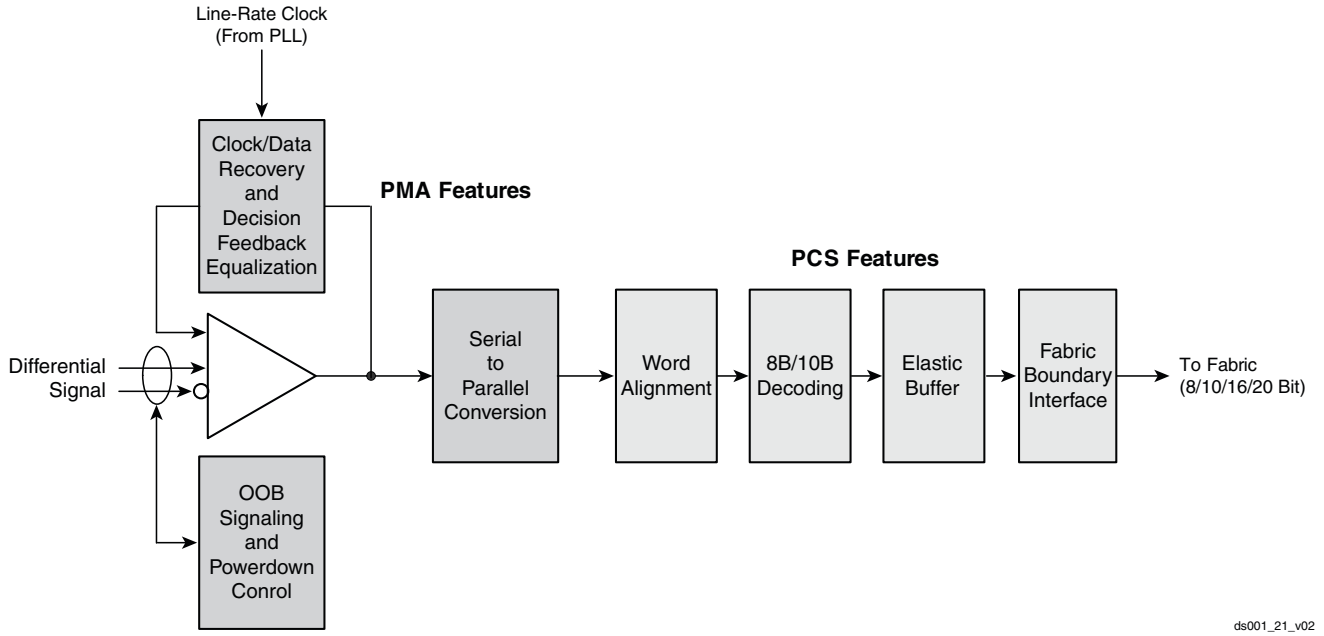


Figure 24: *10.3G SerDes – Receive Section*

Support for Standard Protocols

Table 40 shows which standard protocols are supported. Standards shown with a gray background are supported by both the 5G and 10.3G SerDes. Any listed PCS feature can be bypassed if not needed.

Table 40: *SerDes Supported Standards*

Standard	General		PCS						PMA	
	Number of Lanes	Gbps (Per Lane)	Internal Bus Width (Per Lane)	Coding	Word Alignment	Lane Alignment	Elastic Buffer	Spread Spectrum Clocking	Power-Down States	OOB Signaling
PCIe 1.1	1 / 4 / 8 / 16	2.5	8 / 16	8B / 10B	K28.5	✓	✓	✓	✓	✓
PCIe 2.0	1 / 4 / 8 / 16	2.5 / 5.0	16 / 32	8B / 10B	K28.5	✓	✓	✓	✓	✓
Gigabit Ethernet	1	1.25	8	8B / 10B	K28.5		✓			
SGMII (1)(3)	1	1.25	8	8B / 10B	K28.5		✓			
XAUI	4	3.125	8	8B / 10B	K28.5	✓	✓			
XFI	1	10.375	8	(2)	K28.5					
Fibre Channel – 1	1	1.0625	8 / 16	8B / 10B	K28.5		✓			
Fibre Channel – 2	1	2.125	8 / 16	8B / 10B	K28.5		✓			
Fibre Channel – 4	1	4.25	16 / 32	8B / 10B	K28.5		✓			
Fibre Channel – 8	1	8.5	32	8B / 10B	K28.5		✓			
SATA Gen 1	1	1.5	10	8B / 10B	K28.5			✓	✓	✓
SATA Gen 2	1	3	10	8B / 10B	K28.5			✓	✓	✓
SAS	1	1.5 / 3.0	10	8B / 10B	K28.5			✓	✓	
Interlaken (1)(3)	1–8	3.125 – 6.375	16 / 32	(2)	(2)	(2)	(2)			
CEI6 – SR (1)(3)	1	4.976 – 6.375	32							
CEI6 – LR(1)	1	4.976 – 6.375	32							
SPI–5(1)(3)	19	2.488 – 3.125	8		(2)	(2)				
SFI–5(1)(3)	19	2.488 – 3.125	8		(2)	(2)				
OC48(1)	1	2.488	8		(2)					
Backplane Inter-connect (with DFE)	1–20	1.25 – 10.375	8/16/32	(4)	(4)	(4)	(4)	(4)	(4)	(4)

Notes:

1. 10.3 G SerDes only.
2. Not supported by integrated PCS block (must be implemented in fabric).
3. AC-coupling is supported; DC-coupling is not.
4. Optional.

Clocking and Reset Resources

Global Clock Network

Speedster FPGAs have a hierarchical global clock network running through all I/O banks on all four sides of the device. This network delivers the input or synthesized clock signal to all destinations with balanced delays, resulting in very low skew. The following section describes different global clock sources available in Speedster FPGAs.

Global Clock I/O buffer

Each corner of a Speedster FPGA has six Global Clock I/O buffers (CBs). These buffers can be used as either three differential I/Os or six single-ended I/Os. If these inputs are not used as clock buffers, they can be used as general purpose user I/O buffers.

Global Clock Generator

Each corner of a Speedster FPGA has either two or four Global Clock Generators (GCGs), consisting of a PLL with programmable clock synthesizers at the output. Each of four outputs (**Figure 25**, page 42) can pick any of the eight phases of the output clock. Each PLL output can also dynamically step through the phases sequentially.

One of the four outputs from each PLL in a corner can be routed to any of the six I/Os of the clock bank in that corner. Hence, the output from the PLL can be sent out directly through any I/O of the clock bank in that corner.

Note: *This output has a unique pin designation in the macro library element for the PLL.*

The Clock Generator PLL performance specifications are listed in **Table 41**.

Each PLL output has an additional programmable Output Synthesizer (OS) which can be bypassed. The OS output frequency can be a divided version of the input from 1 (bypassed) to 2,046. There are independent 10-bit count settings available to control the pulse width for the high and low cycle of the clock output. The sum of these two counter settings determines the frequency divisor. In addition, the high cycle on the clock can optionally be extended by one half cycle. This feature is useful when a 50% duty cycle output is desired for an odd divisor.

Each output has an Output Gate (OG) circuit. The OG circuit synchronizes the clock enable (clken) input from the FGPA picoPIPE fabric with the clock output from the OS. This synchronized signal can enable or disable the clock output. This capability can be selectively enabled or disabled individually for each output in the configuration of the Global Clock Generator. The output clock and input of the OS will be phase aligned. The input clock of the Global Clock Generator can come from:

- **"Global Clock I/O buffer"**
- Other Global Clock Generator

Table 41: *Clock Generator PLL Performance Specifications*

Performance Specifications	
Divided reference frequency range	977 KHz – 500 MHz
Divide by 1 output frequency range (VCO output internally divided by 2 for 50% DC)	200 MHz – 1 GHz
Reference divider values	1–64
Feedback divider values	2–512
External feedback divider values	1
Output divider values	1–8
Number of adjustable phase outputs	4
Number of internal phases	16
Internal phase separation	6.25% output cycle
Internal phase accuracy	±2.5% output cycle at 1 GHz
Divide by 1 output multiples of div. reference	2–512
Bandwidth adjustment div. range	1–4096
Feedback signal delay (max)	$\frac{1.5}{\sqrt{1\,\text{GHz} \times F_{REF}}}$
Output duty cycle (nominal tolerance)	50%, ±2%
Static phase error (max)	±1% div. reference cycle
Period jitter (P-P) (max)	±2.5% output cycle
Input-to-output jitter (P-P) (max)	±1.25% div. reference cycle
Power dissipation (nom)	5 mA at 500 MHz (Divide by 1 output)
Reset pulse width (min)	5 us
Reset divide by 1 output frequency range	10 MHz – 100 MHz
Lock time (min allowed)	500 div. reference cycles
Frequency overshoot (full-~/half-~) (max)	40%/50%
Reference input jitter (long-term P-P, max)	2% div. reference cycle
Reference/feedback pulse width (min)	190 ps
Supply voltage (V_{DD}, V_{DDA}) (nominal tolerance)	1.0 V ±10%

The feedback input of a Global Clock Generator (**Figure 26**) receives its inputs from Global Clock Network endpoints, Global Clock Input Buffers and from its own output.

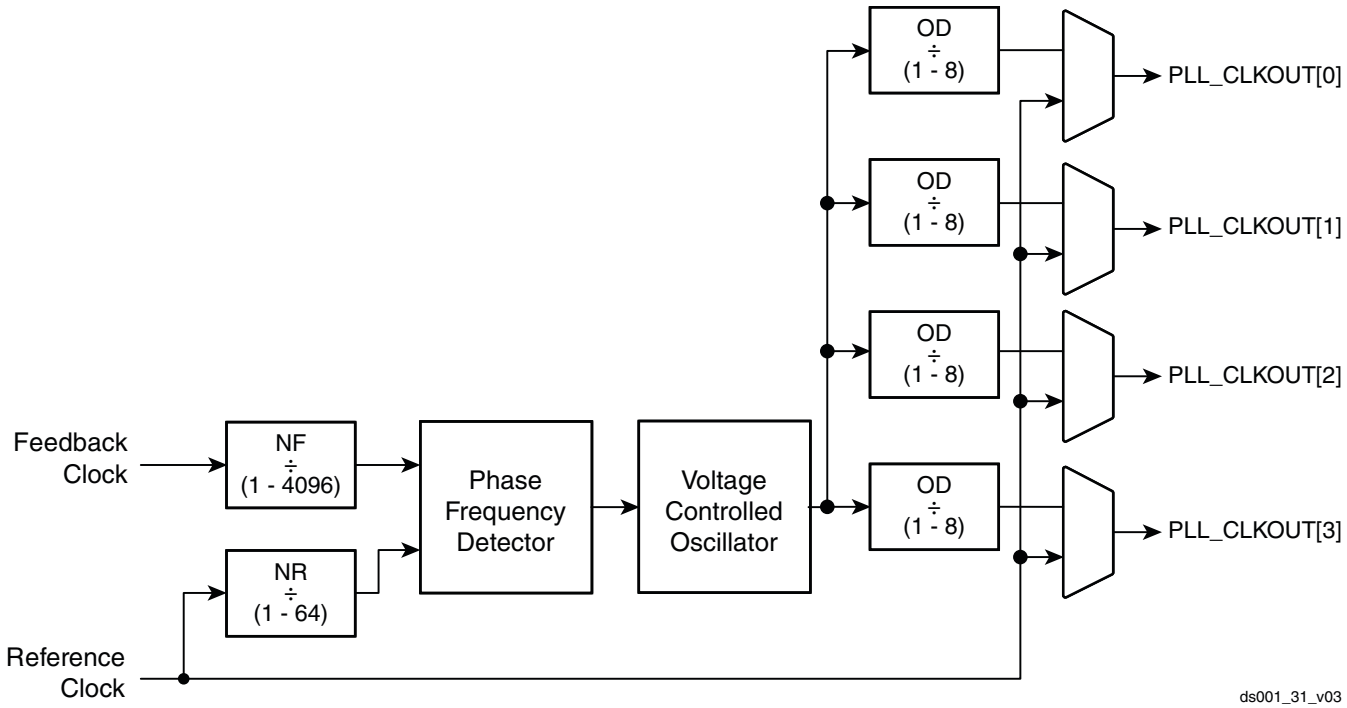


Figure 25: *PLL Block Diagram*

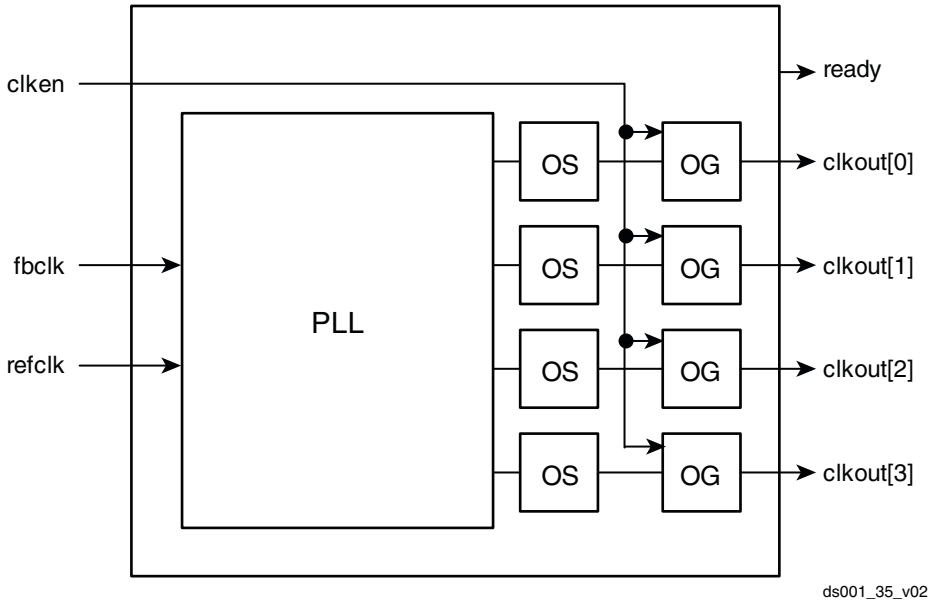


Figure 26: *Global Clock Generator*

Byte-Lane Clock Networks

Separate from the Global Clock Network, each EF I/O Bank in a Speedster FPGA has an independent Byte-Lane Clock Network designed for source-synchronous interfaces.

A byte lane in a Speedster FPGA consists of 12 I/O buffers. Two of these I/O Buffers are clock capable and can be used to receive or send a clock. These buffers can be used as one differential pair for a clock or as two single-ended buffers for two clocks. Each of these received clocks can optionally be delayed using a DLL.

The Byte-Lane Clock Network supports four byte lanes in a repeating fashion. For example, there are three Byte-Lane Clock Networks in an I/O Bank with 12 bytes: byte 0 to 3, byte 4 to 7, and byte 8 to 11.

Each Byte-Lane Clock Network can function as follows:

- Eight by-9 clock networks
- Four by-18 clock network
- One by-36 clock network

Speedster Reset Resources

Reset Input Block

Each corner of a Speedster FPGA has an individual Reset Input Block. This block receives external reset inputs as well as inputs generated internally within the device. External reset inputs are driven by either dedicated clock pads or from I/Os in adjacent banks located in each corner. Internal reset inputs are driven across the asynchronous to synchronous (ASC) boundary after being generated within the core. All resets distributed as part of the global reset network are active-Low.

In addition, the inputs to the Reset Input Block generated either externally or internally are required to be active-Low and glitch free. The input resets can be either asynchronous or synchronous. An asynchronous reset is synchronized for de-assertion to each and every clock domain where it is utilized. A synchronous reset does not need to be synchronized to the same clock domain but is synchronized when used in any other clock domain not synchronous with the current clock domain.

Each reset output generated by the Input Reset Block is synchronized to a selectable clock domain by a reset synchronizer. The clock domain is selected by a clock multiplexer located within a bank physically close to the Input Reset Block, ensuring that the synchronous elements in the device have balanced latency for both the clock and associated reset.

The input to the reset synchronizer is driven by an input reset multiplexer, allowing selection of one of the inputs from the Input Reset Block

Reset Network

The reset outputs of the Input Reset Blocks are distributed to each of the I/O banks and major blocks of the device using a hierarchical reset distribution network. A balanced reset assertion and, more importantly, de-assertion latency is required across the entire device, made possible by pipelining the reset distribution using the clock to which the reset is synchronized. The reset network consists of two hierarchies:

- **"Global Reset Network"**
- **"Bank Reset Network"**

Global Reset Network

Each side of the device has two groups of reset signals running in opposite directions. Each group consists of eight reset signals each, spanning the entire edge of the device in a pipelined manner. The two groups of reset signals are tapped at each I/O bank or logic blocks (such as DDR controller, SERDES, etc.), using a configurable pipeline multiplexer with configurable pipelined latency. The configuration is set for each multiplexer individually to balance the latency for each reset signal across the entire device. The outputs of the pipeline multiplexer are subsequently distributed to the bank reset network.

Bank Reset Network

Each I/O bank receives the outputs of the pipeline multiplexers. For example, the I/O bank at the bottom left of the device (BSW) receives 16 reset inputs, eight from the reset group driven North and eight from the reset group driven South. The 16 reset inputs are distributed across the entire bank and are received by reset multiplexers associated with each clock multiplexer. The reset multiplexers then select the appropriate reset associated with the clock input selected by the corresponding clock multiplexer. There are two-pipeline multiplexers for each reset line to drive across the I/O bank. Each logic block similarly receives the outputs of the pipeline multiplexers and feeds the reset signals into a reset multiplexer present for each clock multiplexer within the block.

Register Initialization

As shown in **Figure 8**, page 8, registers are implemented in SEQs used as CEs with an initial token. The value of the initial token (initialization of registers after configuration) depends on the register type. All registers with preset inputs such as DFFS are powered up high after configuration. All other registers, such as DFFR or DFF, are powered up low after configuration. This behavior is true even if the reset or preset inputs of the registers are tied to inactive levels.

Configuration Interface

The embedded programming and configuration logic is designed to support a variety of programming options. **Figure 27** outlines the basic block diagram of the programming and configuration logic, including additional logic to implement security features. The configuration management unit controls the startup and shutdown sequence from configuration mode to the user mode and back. The configuration management unit includes the provisions for configuring the device with a secure bitstream using a 256-bit Advanced Encryption Standard (AES) algorithm in Cipher Block Chaining (CBC) mode. The device contains a small non-volatile memory for the storage of the required AES key.

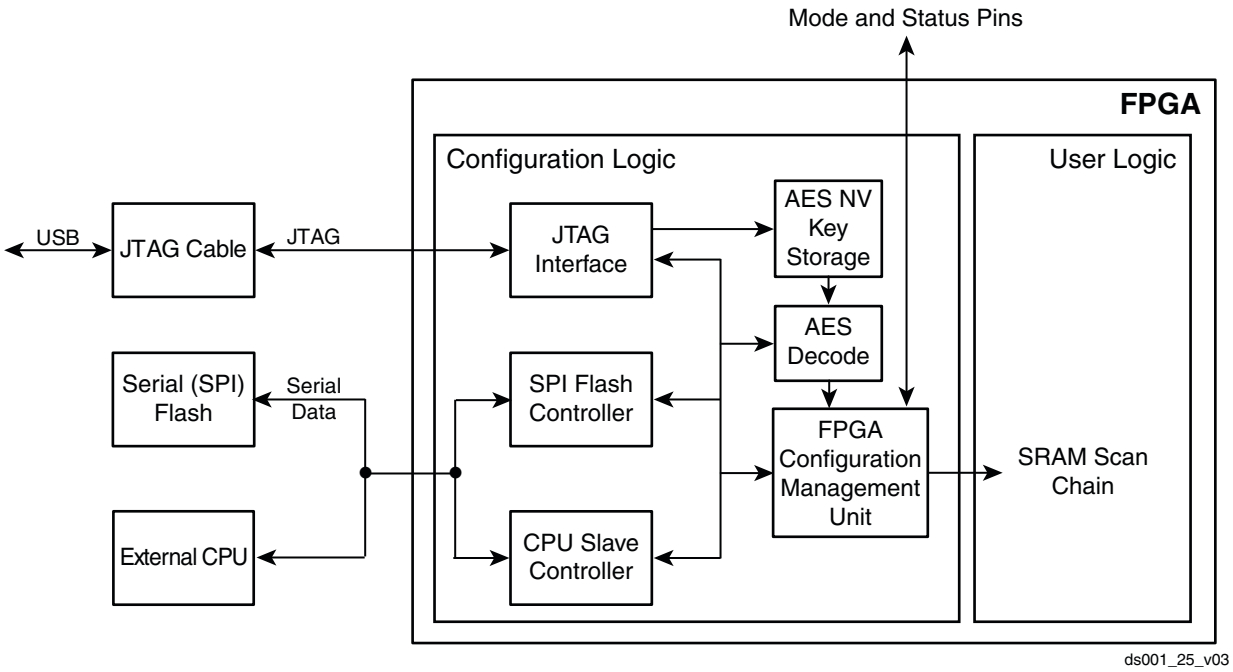


Figure 27: *Configuration Logic Overview*

Supported Programming and Configuration Modes

Several programming and configuration modes are used to support FPGA development and deployment phases. To avoid confusion, the term programming refers to the action of writing a bitstream to flash, so that on the next power-on cycle, the newly written bitstream can be used to configure the FPGA. The term configuration refers to the process of configuring the FPGA to implement the required user functionality.

Note: *The recommended memory space to store the configuration data for the SPD60 is 8 MB.*

The supported programming modes are:

- Serial flash (SPI) programming (SFP)

The supported configuration modes are:

- JTAG FPGA configuration (JFC)
- Serial flash (SPI) FPGA configuration (SFC)
- External CPU FPGA configuration (EFC)
- Multiple Serial Flash (SPI) interfaces (MSF)

Note: *All flash modes listed are master (where an external clock is routed to the flash memory from the FPGA, controlling the configuration timing).*

A simplified diagram showing the supported configuration modes is shown in **Figure 28**, page 45.

JTAG FPGA Configuration (JFC)

The JFC mode allows the FPGA to be configured directly via a JTAG download cable. This mode is used during user-logic development and testing cycles.

Serial Flash Configuration (SFC)

The SFC mode allows serial flash PROMs to be used to configure the FPGA. In this mode the FPGA is the master, and therefore supplies the clock to the PROM.

External CPU FPGA Configuration (EFC)

The EFC mode configures the FPGA from an external CPU after a system power-up cycle. This mode can be used both during user-logic development as well as in a production environment.

Multiple Serial Flash (SPI) Interfaces (MSF)

To reduce programming timing without adding the complexity of a parallel flash controller, a parallel array of four SPI flash devices can be used. A by-four array reduces the data-loading time to approximately 150 ms.

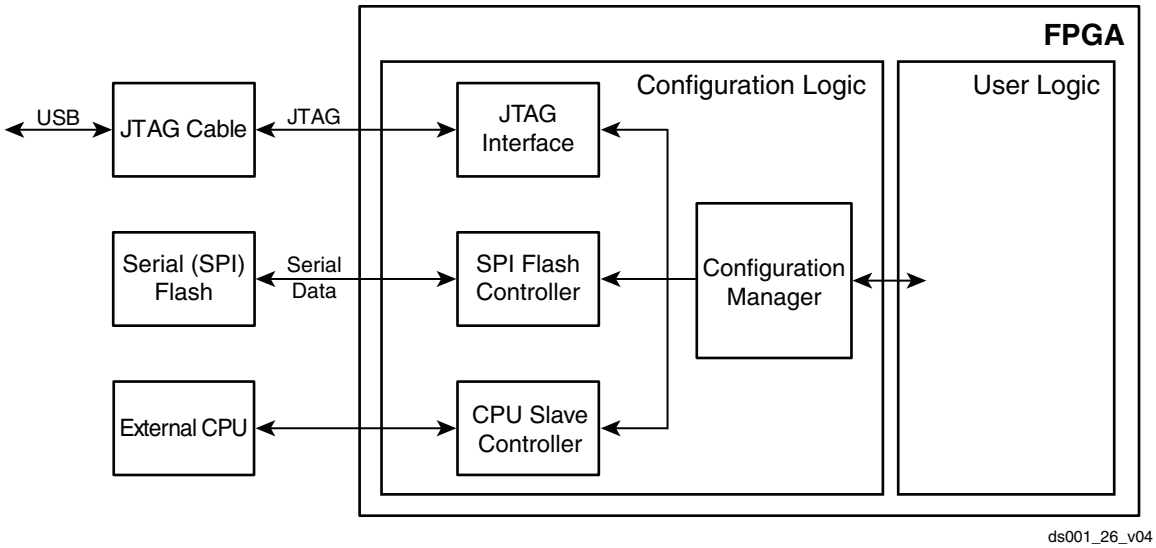


Figure 28: *Simplified Configuration Diagram*

Configuration Interface

"Configuration Bank Pins(3)" in **Table 44**, page 48 describes the FPGA pins used for the various supported configuration modes. Dedicated pins between modes can be shared (Serial Flash by 1, Serial Flash by 4, CPU modes) since the function is determined by the static state selected by the CONFIG_MODESEL[2:0] inputs (**Table 42**). **Figure 29** through **Figure 32**, page 47 illustrate each of the supported configuration interfaces.

Table 42: *Pins Used for Support Configuration Modes*

External Pin Name	EFC	SFC	MSF	JFC
SDI	DQ[0]	Serial data output to flash memory		–
SDO[3]	DQ[1]	–	Input of configuration data from flash	–
SDO[2]	DQ[2]	–	Input of configuration data from flash	–
SDO[1]	DQ[3]	–	Input of configuration data from flash	–
SDO[0]	DQ[4]	Input of configuration data from flash		–
HOLDN	DQ[5]	Hold output to flash		–
CSN[3]	DQ[6]	–	Active-low chip select	–
CSN[2]	DQ[7]	–	Active-low chip select	–
CSN[1]	Unused	–	Active-low chip select	–
CSN[0]	Active-low chip select			–
CPU_CLK	CPU clock	–	–	–
CONFIG_RSTN	Active-low configuration reset			
CONFIG_DONE	Open-drain configuration done output			
CONFIG_STATUS	Open-drain SRAM initialization complete output			
CONFIG_MODESEL[2:0]	Configuration mode select; must be '100'	Configuration mode select; must be '001'	Configuration mode select; must be '010'	Configuration mode select; Don't care
CONFIG_SYSCLK_BYPASS	Bypass configuration system clock. Don't-care	Bypass configuration system clock. Set to '0'		Bypass configuration system clock; Don't care
CONFIG_CLKSEL	Selects configuration clock. set to '0'			Don't care

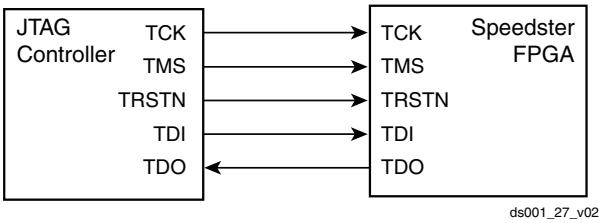


Figure 29: *JTAG Configuration Interface*

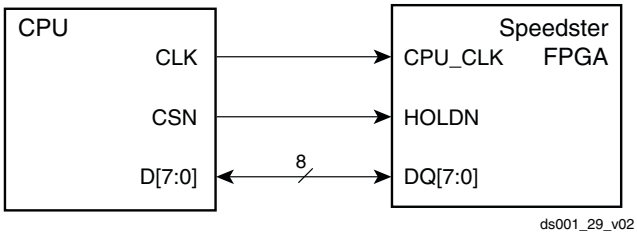


Figure 31: *Slave CPU Configuration Interface*

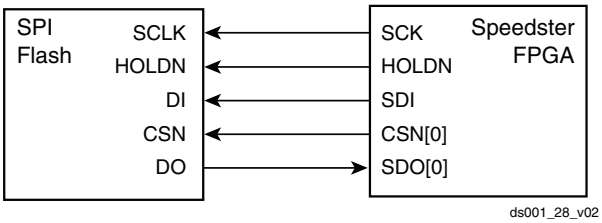


Figure 30: *SPI Flash PROM Configuration Interface*

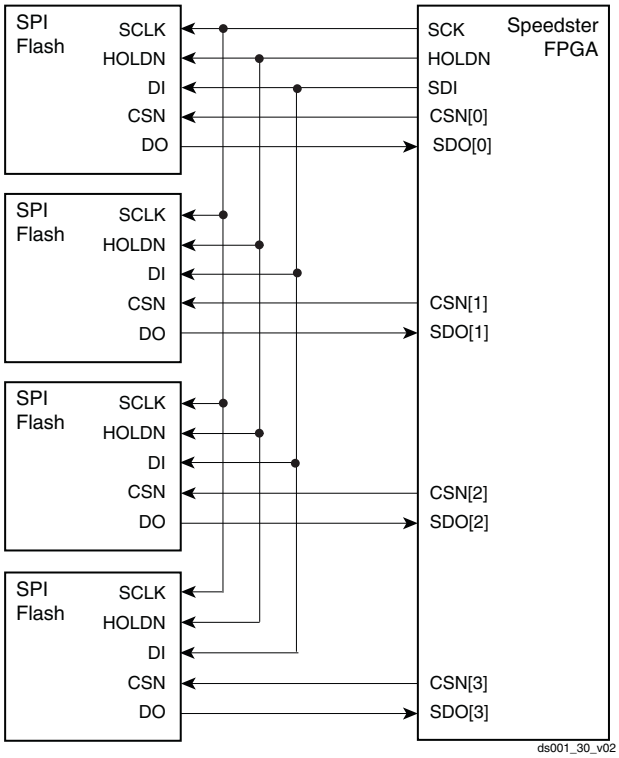


Figure 32: *By-Four SPI Flash Programming*

Figure 33, page 47 shows a simplified block diagram of FPGA configuration control logic. Regardless of the configuration control settings, if the programming hardware is connected to JTAG pins driving the FCU, the configuration clock (CFG_CLK) is automatically driven by TCK. In single or multiple flash configuration mode, if not overridden by JTAG circuitry, users can select between internally generated (SYSCLK) or externally driven configuration clock (CPU_CLK) using CONFIG_SYSCLK_BYPASS pin.

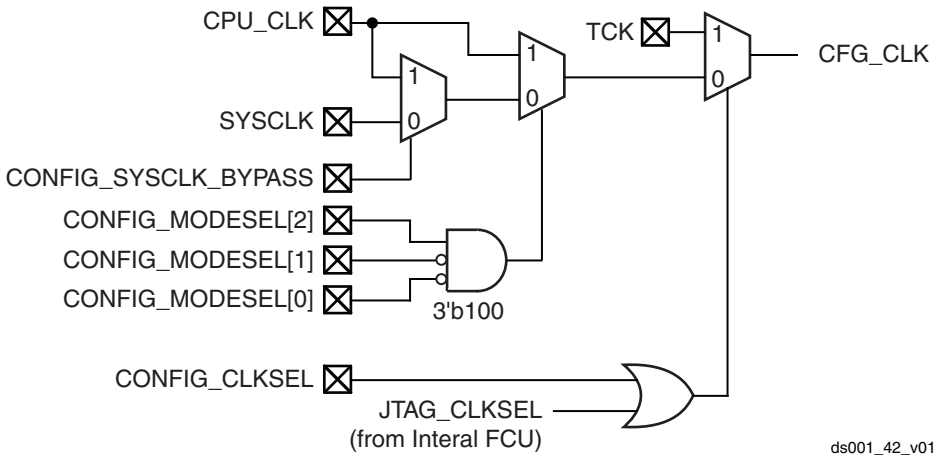


Figure 33: *FPGA Configuration Logic (Simplified View)*

Packaging Options

Speedster FPGAs are available in a variety of package options. Most adjacent family members are available in the same package and are pin-compatible, allowing migration between the members without a board layout change.

The package options are listed in **Table 43**.

Table 43: *Speedster FPGA Packaging*

Package Options	Available User I/O (Including SerDes Channels)			
	SPD30	SPD60	SPD100	SPD180
899 FBGA Package	514	–	–	–
1285 FBGA package	520	712	722	–
1892 FBGA Package	–	904	976	1010

Pin Descriptions

Table 44: *Speedster FPGA Pin Description*

Pin Name	Pin Group	Type	Description
TEMP_DIODE_[P,N]	TEMP	Input	Bias inputs used in conjunction with the temperature sensing diode inside the Speedster device. The P indicates the pin connected to the anode of the diode, while the N indicates the pin connected to the cathode.
SerDes Pins(1)			
VDDHA_10G[q]	10G[q]	Power	Analog supply voltage for the 10.3 Gbps SerDes. There are two V_{DDHA} pins per 10.3 Gbps quad. This pin should be powered even if SerDes is not used.
VDDA_10G[q]	10G[q]	Power	Analog supply voltage for the 10.3 Gbps SerDes. There are four V_{DDA} pins per 10.3 Gbps quad. This pin should be powered even if SerDes is not used.
VDDT_10G[q]	10G[q]	Power	Transmit driver power for the 10.3 Gbps SerDes (1.0V or 1.2V nominal). The setting of this supply to 1.2V or 1.0V depends on the interface standard mode that the quad is configured to operate in. There are 3 V_{DDT} supply pin for each 10.3 Gbps quad. This pin should be powered even if SerDes is not used.
P_10G[q]_REFRES	10G[q]	Input	Reference resistor input for 10.3 Gbps SerDes. Requires a 3 kΩ ±1% accurate off-chip resistor connected from this pad to ground. There is one input for each 10.3 Gbps quad.
P_10G[q]_REFCLK[P,N]	10G[q]	Input	The 10.3 Gbps SerDes reference clock supplied from either a single-ended or differential external source. The reference clock is buffered, used by the clock multiplication unit (CMU) to generate the transmit bit clock and also distributed to the respective data lanes. The requirements on the reference clock vary depending on the standard and data rate used. There is 1 differential pair for each 10.3 Gbps quad.
P_10G[q]_LN[3:0]_RX[P,N]_I	10G[q]	Input	Receive differential inputs to the 10.3 Gbps SerDes. There are four differential pairs per 10.3 Gbps quad.
P_10G[q]_ATEST_O	10G[q]	Output	The 10.3 Gbps SerDes Analog DC test pad used for ATE and bench testing.
P_10G[q]_LN[3:0]_TX[P,N]_O	10G[q]	Output	Transmit differential outputs from the 10.3 Gbps SerDes. There are four differential pairs per 10.3 Gbps quad.

Table 44: *Speedster FPGA Pin Description (Continued)*

Pin Name	Pin Group	Type	Description
VDDHA_5G[q]	5G[q]	Power	Analog supply voltage for the 5 Gbps SerDes. There are two V_{DDHA} pins per 5 Gbps quad. This pin should be powered even if SerDes is not used.
VDDA_5G[q]	5G[q]	Power	Analog supply voltage for the 5 Gbps SerDes. There are seven V_{DDA} pins per 5 Gbps quad. This pin should be powered even if SerDes is not used.
P_5G[q]_REFRES	5G[q]	Input	Reference resistor input for 5 Gbps SerDes. Requires a 3 kΩ ±1% accurate off-chip resistor connected from this pad to ground. There is one input for each 5 Gbps quad.
P_5G[q]_REFCLK[P,N]	5G[q]	Input	The 5 Gbps SerDes reference clock supplied from either a single-ended or differential external source. The reference clock is buffered, used by the clock multiplication unit (CMU) to generate the transmit bit clock and also distributed to the respective data lanes. The requirements on the reference clock vary depending on the standard and data rate used. There is one differential pair for each 5 Gbps quad.
P_5G[q]_LN[3:0]_RX_[P,N]_I	5G[q]	Input	Receive differential inputs to the 5 Gbps SerDes. There are four differential pairs per 5 Gbps quad.
P_5G[q]_LN[3:0]_TX_[P,N]_O	5G[q]	Output	Transmit differential inputs to the 5 Gbps SerDes. There are four differential pairs per 5 Gbps quad.
P_5G[q]_ATEST_O	5G[q]	Output	The 5 Gbps SerDes Analog DC test pad Used for ATE and bench testing.
IEEE 1149.1 JTAG Interface Pins(2)			
VDDO_JTAG	JTAG	Power	Supply voltage powering the I/O buffers for the IEEE 1149.1 JTAG interface. This supply can connected to either 2.5V or 3.3V. The value selected determine the output V_{OH} level on TDO and set the input threshold V_{IL} and V_{IH} values appropriately.
TMS	JTAG	Input	The Test Mode Select (TMS) input controlling the test access port (TAP) controller state machine transitions. This input is captured on the rising edge of the test logic clock (TCK). This dedicated pin is equipped with a pull-up resistor to place the test logic in the Test-Logic-Reset state.
TCK	JTAG	Input	IEEE 1149.1 JTAG interface dedicated test clock used to advance the TAP controller and clock in data on the TDI input and out on the TDO output. The maximum frequency for TCK is 100 MHz.
TDI	JTAG	Input	IEEE1149.1 JTAG interface serial input for instruction and test data. Data is captured on the rising edge of the test logic clock. This dedicated pin is equipped with a pull-up resistor.
TRSTN	JTAG	Input	IEEE 1149.1 JTAG interface asynchronous active-Low reset input used to initialize the TAP controller. This dedicated pin is equipped with a pull-up resistor.
TDO	JTAG	Output	IEEE 1149.1 JTAG serial output for data from the test logic. TDO is set to an inactive drive state (high impedance) when data scanning is not in progress. This pin is equipped with a pull-up resistor. TDO drives out valid data on the falling edge of the TCK input.
Configuration Bank Pins(3)			
VDDO_CFG	CFG	Power	The supply voltage for the I/Os in the configuration bank. This pin should be connected to 2.5 V or 3.3 V
CONFIG_RSTN	CFG	Input	Asynchronous active-Low reset input clearing the configuration memory in the device and the logic in the FPGA configuration unit (FCU). In JTAG mode, pulled up (to V_{DDO_CFG}).

Table 44: *Speedster FPGA Pin Description (Continued)*

Pin Name	Pin Group	Type	Description
CONFIG_SYSCLK_BYPASS	CFG	Input	Pin statically enabling the bypass of the internal SYS_CLK.The default clock for the FPGA configuration unit (FCU) is named SYS_CLK. An on-chip ring oscillator is the source for SYS_CLK. For debug purposes this clock can be bypassed and an external clock supplied. In the bypass mode, this pin can be connected to either the IEEE 1149.1 JTAG input pin for TCK or the CPU_CLK input pin.
CONFIG_CLKSEL	CFG	Input	Pin controlling whether the FCU clock is sourced from the TCK input or the CPU_CLK input when CONFIG_SYSCLK_BYPASS is asserted active-High thus enabling the bypass of the internal SYS_CLK: • When this input is biased to '1', TCK is selected • When this input is biased to '0', CPU_CLK is selected.
CPU_CLK	CFG	Input	Clock Input for the FPGA configuration unit (FCU) when in SYS_CLK bypass mode. This input can be used as the SYS_CLK.
CSN[3:0]	CFG	Input/ Output	**In SPI Mode:** The CSN[3:0] pins are active-Low chip select outputs. In the programming mode, individual serial flash devices are mapped to a linear addressing space. In the SPI x1 configuration mode only the CSN[0] output is used. I**n CPU Mode:** CSN[3] is the bidirectional data bit 6, DQ[6]. CSN[2] is the bidirectional data bit 7. DQ[7]. CSN[1] is not used. CSN[0] is an active-Low chip select input.(7)
CONFIG_MODESEL[2:0]	CFG	Input	Configuration mode selection inputs to define the FPGA configuration unit (FCU) mode of operation: • 001: SPI x1 configuration mode • 010: SPI x4 configuration mode • 100: CPU configuration mode
SDO[3:0]	CFG	Input	Input pins providing data input from the flash device(s). In SPI x4 configuration mode, all 4 SDO inputs are utilized. When in SPI x1 mode, only the SDO[0] input is used to input the configuration data In the CPU mode, these bits serve as the bidirectional data bits 1 through 4 (SDO3=DQ1, SDO2=DQ2, SDO1=DQ3, SDO0=DQ4).(7)
SDI	CFG	Output	In the SPI modes of operation, the serial data output pins for command and programming data to the flash memory. These command and programming commands are sent via control registers writes done via the IEEE 1149.1 JTAG interface. In the CPU mode, this pin is the bidirectional data bit 0, DQ[0].(7).
CONFIG_STATUS	CFG	Open-drain output	Pin asserted active-Low by the FCU should an error be detected during configuration.
CONFIG_DONE	CFG	Input with open-drain or active output	Pin asserted active-Low prior to the completion of device configuration. After the device successfully completes configuration, this pin is either tri-stated or can optionally be driven High. The default behavior is open-drain, tri-stating the pin when the device is properly configured. If a device configuration error occurs, the CONFIG_DONE output for the device remains in active-Low. In the default mode of operation, an external pull-up resistor is needed to take the pin High. The device does not enter the functional mode until this pin is active-High. Holding this pin Low on the board can be used as a method to synchronize the start-up of multiple devices.
SCK	CFG	Output	Serial flash clock output. Default rate is set to 25 MHz. This output clock rate can be lowered by the bitstream during configuration.
HOLDN	CFG	Output	In the SPI mode of operation, the hold signal output for SPI flash devices. In CPU mode, this bit is the bidirectional data bit 5, DQ[5].(7)
PROGRAM_ENABLE	CFG	Input	Pin enabling the programming of the eFuse for the AES encryption keys. This input pin active-High (to the V_{DDO_CFG} voltage level).

Table 44: *Speedster FPGA Pin Description (Continued)*

Pin Name	Pin Group	Type	Description
VDDQ	VDDQ	Input	Supply required for eFuse programming. V_{DDQ} pin should be kept Low except when programming the AES encryption keys.
User Programmable I/O Banks(4)			
VDDO_B[b]	B[b]	Power	Bank I/O supply voltage.
VDDO_B[b]_UP	B[b]	Power	I/O supply voltage pins required for particular type of bank (b=2, 5 for SPD60) allowing for separate V_{DDO} supplies within the bank. VDDO_B[b]_UP supplies the positive and negative I/O pins 0 through 23.(5)
VDDO_B[b]_DOWN	B[b]	Power	I/O supply voltage pins required for particular type of bank (b=2, 5 for SPD60) allowing for separate V_{DDO} supply within the bank. VDDO_B[b]_DOWN supplies the positive and negative I/O pins 24 through 47.(5)
VREF_B[b]	B[b]	Input	Input threshold voltage pins required for particular bank. This pin can be left open if I/O standards in the bank do not require threshold (reference) voltage input.
VREF_B[b]_UP	B[b]	Input	Input threshold voltage pins required for particular type of bank (b=2, 5 for SPD60) allowing for separate V_{REF} supplies within the bank. VREF_B[b]_UP supplies reference voltage for the positive and negative I/O pins 23 through 0. This pin can be left open if I/O standards in the bank do not require threshold (reference) voltage input.(5)
VREF_B[b]_DOWN	B[b]	Input	Input threshold voltage pins required for particular type of bank (b=2, 5 for SPD60) allowing for separate V_{REF} supplies within the bank. VREF_B[b]_DOWN supplies reference voltage for the positive and negative I/O pins 47 through 24. This pin can be left open if I/O standards in the bank do not require threshold (reference) voltage input.(5)
P_RTTLO_B[b]	B[b]	Input	Pins for RTT (receiver termination) compensation. This resistor is used to set impedance to ½ or ¼ of the resistor value. For example, the P_RTTLO pin must be tied to VDDO_B[b] via a 300Ω external resistor for an impedance of 150 or 75Ω.(9)
P_RTTHI_B[b]	B[b]	Input	Pins for RTT (receiver termination) compensation. This resistor is used to set impedance to ½ or ¼ of the resistor value. For example, the P_RTTHI pin must be tied to V_{SS} via a 300Ω external resistor for an impedance of 150 or 75Ω.(9)
P_DRVLO_B[b]	B[b]	Input	These pins are for the driver compensation. The P_DRVLO pin must be tied to VDDO_B[b] via an external resistor.(8)
P_DRVHI_B[b]	B[b]	Input	These pins are for the driver compensation. The P_DRVHI pin must be tied to V_{SS} via an external resistor.(8)
P_D[47:0][P,N]_B[b](4)	B[b]	I/O	These are the general purpose input and output pads available to support either single ended or differential inputs. When used for implementing a differential pair the P represents the positive terminal and N the negative terminal in the interface.
User Programmable Clock Banks(6)			
VDDO_CB[b]	CB[b]	Power	These are I/O supply voltages for a particular clock bank.
VREF_CB[b]	CB[b]	Input	These are input threshold voltage pins required for particular clock bank I/O standards. This pin can be left open if I/O standards in the bank do not require threshold (reference) voltage input.

Table 44: *Speedster FPGA Pin Description (Continued)*

Pin Name	Pin Group	Type	Description
P_RTTLO_CB[b]	CB[b]	Input	Pins for RTT (receiver termination) compensation. This resistor is used to set impedance to ½ or ¼ of the resistor value. For example, the P_RTTLO pin must be tied to VDDO_CB[b] via a 300Ω external resistor for an impedance of 150 or 75Ω.(9)
P_RTTHI_CB[b]	CB[b]	Input	Pins for RTT (receiver termination) compensation. This resistor is used to set impedance to ½ or ¼ of the resistor value. For example, the P_RTTHI pin must be tied to V_{SS} via a 300Ω external resistor for an impedance of 150 or 75Ω.(9)
P_DRVLO_CB[b]	CB[b]	Input	Pins for driver compensation. The P_DRVLO pin must be tied to V_{DDO} via an external resistor.(8)
P_DRVHI_CB[b]	CB[b]	Input	Pins for driver compensation. The P_DRVHI pin must be tied to V_{SS} via an external resistor.(8)
PLL_VDDA[a]_[c]	PLL	Power	The 1.0V ±5% analog supply pins for the PLL. There are 4 in each quadrant. The value of *a* can be either 0 or 1. The value of *c* can be NW for Northwest, NE for Northeast, SW for Southwest, or SE for Southeast.
PLL_VSSA[a]_[c]	PLL	Power	The analog ground pins for the PLL. There are 4 in each quadrant. The value of *a* can be either 0 or 1. The value of *c* can be NW for Northwest, NE for Northeast, SW for Southwest, or SE for Southeast.
P_D[2:0][P,N]_CB[b]	PLL	I/O	Clock buffer inputs available to support up to 6 single-ended inputs or 3 differential inputs. If not used as clock buffers, these pins can be used as user I/O buffers. When used for implementing a differential pair, the P represents the positive terminal and N the negative terminal in the interface.
Power Supplies			
VDD	VDD	Power	Supply for low-voltage devices in the S-Frame
VDDL	VDD	Power	Supply for the picoPIPE FPGA fabric.
VSS	VSS	Power	Ground pins for the device.
Other			
NB	NB		There is no solder ball at this grid location on the package
N/C	N/C		There is no connection to the solder ball at this package grid location

Notes:

1. The q in the pin name and pin group is variable indicating the specific quad to which the pin is associated (for example q can equal A, B, etc.).
2. The device can always be configured through the JTAG interface without regard to the settings on the CONFIG_MODESEL[2:0] bits described in **"Configuration Bank Pins(3)."**
3. Several of the pins in this section are multifunction pins whose functions depend on the configuration mode selected through the CONFIG_MODESEL[2:0] inputs.
4. The variable b in the pin name and pin group indicates the specific bank; possible values of b for EF banks are 1,3,4,6 and for BF banks NW, NE, SW, and SE.
5. See **Page 17** for a more detailed discussion of this special type of bank.
6. The variable b in the pin name and pin group indicates the specific bank; possible values of are 1, 2, 3, 4.
7. An overview of the dual function assignment of these pins is shown in **Table 42**, page 46.
8. The resistor value for this input is dependent on the I/O standard. See **Table 38**, page 38.
9. See **Table 39**, page 38.

Pinouts

1892-Pin Fine Ball Grid Array (FG1892)

Table 45: *FG1892 Pin Listing for SPD60*

Pin	Pin Name	Group	DDR123 Hard Controller (x8)	x8/x9 DQ–QS	x16/x18 DQ–QS	x32/x36 DQ–QS
A1	NB	NB	–	–	–	–
A2	NB	NB	–	–	–	–
A3	N/C	–	–	–	–	–
A4	N/C	–	–	–	–	–
A5	N/C	–	–	–	–	–
A6	N/C	–	–	–	–	–
A7	NB	NB	–	–	–	–
A8	NB	NB	–	–	–	–
A9	N/C	–	–	–	–	–
A10	N/C	–	–	–	–	–
A11	P_5GB_LN3_RXN_I	5GB	–	–	–	–
A12	P_5GB_LN3_RXP_I	5GB	–	–	–	–
A13	NB	NB	–	–	–	–
A14	NB	NB	–	–	–	–
A15	P_5GB_LN2_RXN_I	5GB	–	–	–	–
A16	P_5GB_LN2_RXP_I	5GB	–	–	–	–
A17	P_5GB_LN1_RXN_I	5GB	–	–	–	–
A18	P_5GB_LN1_RXP_I	5GB	–	–	–	–
A19	NB	NB	–	–	–	–
A20	NB	NB	–	–	–	–
A21	P_5GB_LN0_RXN_I	5GB	–	–	–	–
A22	P_5GB_LN0_RXP_I	5GB	–	–	–	–
A23	P_5GA_LN3_RXN_I	5GA	–	–	–	–
A24	P_5GA_LN3_RXP_I	5GA	–	–	–	–
A25	NB	NB	–	–	–	–
A26	NB	NB	–	–	–	–
A27	P_5GA_LN2_RXN_I	5GA	–	–	–	–
A28	P_5GA_LN2_RXP_I	5GA	–	–	–	–
A29	P_5GA_LN1_RXN_I	5GA	–	–	–	–
A30	P_5GA_LN1_RXP_I	5GA	–	–	–	–
A31	NB	NB	–	–	–	–
A32	NB	NB	–	–	–	–
A33	P_5GA_LN0_RXN_I	5GA	–	–	–	–
A34	P_5GA_LN0_RXP_I	5GA	–	–	–	–
A35	N/C	–	–	–	–	–
A36	N/C	–	–	–	–	–
A37	NB	NB	–	–	–	–
A38	NB	NB	–	–	–	–
A39	N/C	–	–	–	–	–
A40	N/C	–	–	–	–	–

Table 45: *FG1892 Pin Listing for SPD60*

Pin	Pin Name	Group	DDR123 Hard Controller (x8)	x8/x9 DQ–QS	x16/x18 DQ–QS	x32/x36 DQ–QS
A41	N/C	–	–	–	–	–
A42	N/C	–	–	–	–	–
A43	NB	NB	–	–	–	–
A44	NB	NB	–	–	–	–
AA1	P_D27N_B5	B5	DQSN8	DQSN11	DQ5	DQ2
AA2	P_D27P_B5	B5	DQSP8	DQSP11	DQ5	DQ2
AA3	VSS	VSS	–	–	–	–
AA4	VDDO_B5_DOWN	B5	–	–	–	–
AA5	P_D36N_B5	B5	RESERVED	DQ9	DQ4	DQ2
AA6	P_D37N_B5	B5	DQ6	DQ9	DQ4	DQ2
AA7	P_D17P_B5	B5	DM	DQ10	DQ5	DQ2
AA8	P_D16P_B5	B5	DQ7	DQ10	DQ5	DQ2
AA9	VDDO_B5_UP	B5	–	–	–	–
AA10	P_D11P_B5	B5	DM	DQ9	DQ4	DQ2
AA11	P_D10P_B5	B5	DQ6	DQ9	DQ4	DQ2
AA12	P_DRVHI_B5	B5	–	–	–	–
AA13	VREF_B6	B6	–	–	–	–
AA14	VDD	VDD	–	–	–	–
AA15	VSS	VSS	–	–	–	–
AA16	VDDL	VDD	–	–	–	–
AA17	VSS	VSS	–	–	–	–
AA18	VDD	VDD	–	–	–	–
AA19	VSS	VSS	–	–	–	–
AA20	VDDL	VDD	–	–	–	–
AA21	VSS	VSS	–	–	–	–
AA22	VDD	VDD	–	–	–	–
AA23	VSS	VSS	–	–	–	–
AA24	VDDL	VDD	–	–	–	–
AA25	VSS	VSS	–	–	–	–
AA26	VDD	VDD	–	–	–	–
AA27	VSS	VSS	–	–	–	–
AA28	VDDL	VDD	–	–	–	–
AA29	VSS	VSS	–	–	–	–
AA30	VDD	VDD	–	–	–	–
AA31	VSS	VSS	–	–	–	–
AA32	VREF_B1	B1	–	–	–	–
AA33	P_DRVHI_B2	B2	–	–	–	–
AA34	P_D10P_B2	B2	DQ6	DQ9	DQ4	DQ2
AA35	P_D11P_B2	B2	DM	DQ9	DQ4	DQ2
AA36	VDDO_B2_UP	B2	–	–	–	–
AA37	P_D16P_B2	B2	DQ7	DQ10	DQ5	DQ2
AA38	P_D17P_B2	B2	DM	DQ10	DQ5	DQ2
AA39	P_D37N_B2	B2	DQ6	DQ9	DQ4	DQ2
AA40	P_D36N_B2	B2	RESERVED	DQ9	DQ4	DQ2

Table 45: *FG1892 Pin Listing for SPD60*

Pin	Pin Name	Group	DDR123 Hard Controller (x8)	x8/x9 DQ–QS	x16/x18 DQ–QS	x32/x36 DQ–QS
AA41	VDDO_B2_DOWN	B2	–	–	–	–
AA42	VSS	VSS	–	–	–	–
AA43	P_D27N_B2	B2	DQSN8	DQSN11	DQ5	DQ2
AA44	P_D27P_B2	B2	DQSP8	DQSP11	DQ5	DQ2
AB1	P_D28N_B5	B5	DQ8	DQ11	DQ5	DQ2
AB2	P_D28P_B5	B5	DQ8	DQ11	DQ5	DQ2
AB3	P_D29N_B5	B5	DQ8	DQ11	DQ5	DQ2
AB4	P_D29P_B5	B5	DQ8	DQ11	DQ5	DQ2
AB5	P_D36P_B5	B5	DM	DQ9	DQ4	DQ2
AB6	P_D37P_B5	B5	DQ6	DQ9	DQ4	DQ2
AB7	P_D17N_B5	B5	RESERVED	DQ10	DQ5	DQ2
AB8	P_D16N_B5	B5	DQ7	DQ10	DQ5	DQ2
AB9	VSS	VSS	–	–	–	–
AB10	P_D11N_B5	B5	RESERVED	DQ9	DQ4	DQ2
AB11	P_D10N_B5	B5	DQ6	DQ9	DQ4	DQ2
AB12	VSS	VSS	–	–	–	–
AB13	VREF_B5_UP	B5	–	–	–	–
AB14	VSS	VSS	–	–	–	–
AB15	VDD	VDD	–	–	–	–
AB16	VSS	VSS	–	–	–	–
AB17	VDDL	VDD	–	–	–	–
AB18	VSS	VSS	–	–	–	–
AB19	VDD	VDD	–	–	–	–
AB20	VSS	VSS	–	–	–	–
AB21	VDDL	VDD	–	–	–	–
AB22	VSS	VSS	–	–	–	–
AB23	VDD	VDD	–	–	–	–
AB24	VSS	VSS	–	–	–	–
AB25	VDDL	VDD	–	–	–	–
AB26	VSS	VSS	–	–	–	–
AB27	VDD	VDD	–	–	–	–
AB28	VSS	VSS	–	–	–	–
AB29	VDDL	VDD	–	–	–	–
AB30	VSS	VSS	–	–	–	–
AB31	VDD	VDD	–	–	–	–
AB32	VREF_B2_UP	B2	–	–	–	–
AB33	VSS	VSS	–	–	–	–
AB34	P_D10N_B2	B2	DQ6	DQ9	DQ4	DQ2
AB35	P_D11N_B2	B2	RESERVED	DQ9	DQ4	DQ2
AB36	VSS	VSS	–	–	–	–
AB37	P_D16N_B2	B2	DQ7	DQ10	DQ5	DQ2
AB38	P_D17N_B2	B2	RESERVED	DQ10	DQ5	DQ2
AB39	P_D37P_B2	B2	DQ6	DQ9	DQ4	DQ2
AB40	P_D36P_B2	B2	DM	DQ9	DQ4	DQ2

Table 45: *FG1892 Pin Listing for SPD60*

Pin	Pin Name	Group	DDR123 Hard Controller (x8)	x8/x9 DQ–QS	x16/x18 DQ–QS	x32/x36 DQ–QS
AB41	P_D29P_B2	B2	DQ8	DQ11	DQ5	DQ2
AB42	P_D29N_B2	B2	DQ8	DQ11	DQ5	DQ2
AB43	P_D28N_B2	B2	DQ8	DQ11	DQ5	DQ2
AB44	P_D28P_B2	B2	DQ8	DQ11	DQ5	DQ2
AC1	P_D30N_B5	B5	RESERVED	DQ10	DQ5	DQ2
AC2	P_D30P_B5	B5	DM	DQ10	DQ5	DQ2
AC3	P_D31N_B5	B5	DQ7	DQ10	DQ5	DQ2
AC4	P_D31P_B5	B5	DQ7	DQ10	DQ5	DQ2
AC5	P_D38N_B5	B5	DQ6	DQ9	DQ4	DQ2
AC6	VSS	VSS	–	–	–	–
AC7	P_D42N_B5	B5	RESERVED	DQ8	DQ4	DQ2
AC8	P_D43N_B5	B5	DQ5	DQ8	DQ4	DQ2
AC9	VSS	VSS	–	–	–	–
AC10	P_D47N_B4	B4	DDDR_RAS_N	DQ7	DQ3	DQ1
AC11	P_D46N_B4	B4	DDR_WE_N	DQ7	DQ3	DQ1
AC12	P_RTTLO_B5	B5	–	–	–	–
AC13	VREF_B5_UP	B5	–	–	–	–
AC14	VDD	VDD	–	–	–	–
AC15	VSS	VSS	–	–	–	–
AC16	VDDL	VDD	–	–	–	–
AC17	VSS	VSS	–	–	–	–
AC18	VDD	VDD	–	–	–	–
AC19	VSS	VSS	–	–	–	–
AC20	VDDL	VDD	–	–	–	–
AC21	VSS	VSS	–	–	–	–
AC22	VDD	VDD	–	–	–	–
AC23	VSS	VSS	–	–	–	–
AC24	VDDL	VDD	–	–	–	–
AC25	VSS	VSS	–	–	–	–
AC26	VDD	VDD	–	–	–	–
AC27	VSS	VSS	–	–	–	–
AC28	VDDL	VDD	–	–	–	–
AC29	VSS	VSS	–	–	–	–
AC30	VDD	VDD	–	–	–	–
AC31	VSS	VSS	–	–	–	–
AC32	VREF_B2_UP	B2	–	–	–	–
AC33	P_RTTLO_B2	B2	–	–	–	–
AC34	P_D46N_B3	B3	DDR_WE_N	DQ7	DQ3	DQ1
AC35	P_D47N_B3	B3	DDDR_RAS_N	DQ7	DQ3	DQ1
AC36	VSS	VSS	–	–	–	–
AC37	P_D43N_B2	B2	DQ5	DQ8	DQ4	DQ2
AC38	P_D42N_B2	B2	RESERVED	DQ8	DQ4	DQ2
AC39	VSS	VSS	–	–	–	–
AC40	P_D38N_B2	B2	DQ6	DQ9	DQ4	DQ2

Table 45: *FG1892 Pin Listing for SPD60*

Pin	Pin Name	Group	DDR123 Hard Controller (x8)	x8/x9 DQ–QS	x16/x18 DQ–QS	x32/x36 DQ–QS
AC41	P_D31P_B2	B2	DQ7	DQ10	DQ5	DQ2
AC42	P_D31N_B2	B2	DQ7	DQ10	DQ5	DQ2
AC43	P_D30N_B2	B2	RESERVED	DQ10	DQ5	DQ2
AC44	P_D30P_B2	B2	DM	DQ10	DQ5	DQ2
AD1	P_D32N_B5	B5	DQ7	DQ10	DQ5	DQ2
AD2	P_D32P_B5	B5	DQ7	DQ10	DQ5	DQ2
AD3	VDDO_B5_DOWN	B5	–	–	–	–
AD4	VSS	VSS	–	–	–	–
AD5	P_D38P_B5	B5	DQ6	DQ9	DQ4	DQ2
AD6	VDDO_B5_DOWN	B5	–	–	–	–
AD7	P_D42P_B5	B5	DM	DQ8	DQ4	DQ2
AD8	P_D43P_B5	B5	DQ5	DQ8	DQ4	DQ2
AD9	VDDO_B5_DOWN	B5	–	–	–	–
AD10	P_D47P_B4	B4	DDR_CAS_N	DQ7	DQ3	DQ1
AD11	P_D46P_B4	B4	DDR_BA[2]	DQ7	DQ3	DQ1
AD12	VDDO_B4	B4	–	–	–	–
AD13	VREF_B5_DOWN	B5	–	–	–	–
AD14	VSS	VSS	–	–	–	–
AD15	VDD	VDD	–	–	–	–
AD16	VSS	VSS	–	–	–	–
AD17	VDDL	VDD	–	–	–	–
AD18	VSS	VSS	–	–	–	–
AD19	VDD	VDD	–	–	–	–
AD20	VSS	VSS	–	–	–	–
AD21	VDDL	VDD	–	–	–	–
AD22	VSS	VSS	–	–	–	–
AD23	VDD	VDD	–	–	–	–
AD24	VSS	VSS	–	–	–	–
AD25	VDDL	VDD	–	–	–	–
AD26	VSS	VSS	–	–	–	–
AD27	VDD	VDD	–	–	–	–
AD28	VSS	VSS	–	–	–	–
AD29	VDDL	VDD	–	–	–	–
AD30	VSS	VSS	–	–	–	–
AD31	VDD	VDD	–	–	–	–
AD32	VREF_B2_DOWN	B2	–	–	–	–
AD33	VDDO_B3	B3	–	–	–	–
AD34	P_D46P_B3	B3	DDR_BA[2]	DQ7	DQ3	DQ1
AD35	P_D47P_B3	B3	DDR_CAS_N	DQ7	DQ3	DQ1
AD36	VDDO_B2_DOWN	B2	–	–	–	–
AD37	P_D43P_B2	B2	DQ5	DQ8	DQ4	DQ2
AD38	P_D42P_B2	B2	DM	DQ8	DQ4	DQ2
AD39	VDDO_B2_DOWN	B2	–	–	–	–
AD40	P_D38P_B2	B2	DQ6	DQ9	DQ4	DQ2

Table 45: *FG1892 Pin Listing for SPD60*

Pin	Pin Name	Group	DDR123 Hard Controller (x8)	x8/x9 DQ–QS	x16/x18 DQ–QS	x32/x36 DQ–QS
AD41	VSS	VSS	–	–	–	–
AD42	VDDO_B2_DOWN	B2	–	–	–	–
AD43	P_D32N_B2	B2	DQ7	DQ10	DQ5	DQ2
AD44	P_D32P_B2	B2	DQ7	DQ10	DQ5	DQ2
AE1	P_D33N_B5	B5	DQSN7	DQSN10	DQSN5	DQ2
AE2	P_D33P_B5	B5	DQSP7	DQSP10	DQSP5	DQ2
AE3	P_D34N_B5	B5	DQ7	DQ10	DQ5	DQ2
AE4	P_D34P_B5	B5	DQ7	DQ10	DQ5	DQ2
AE5	P_D39N_B5	B5	DQSN6	DQSN9	DQ4	DQSN2
AE6	P_D40N_B5	B5	DQ6	DQ9	DQ4	DQ2
AE7	P_D44N_B5	B5	DQ5	DQ8	DQ4	DQ2
AE8	P_D46N_B5	B5	DQ5	DQ8	DQ4	DQ2
AE9	N/C	–	–	–	–	–
AE10	P_D45N_B4	B4	DDR_BA[1]	DQ7	DQ3	DQ1
AE11	P_D43N_B4	B4	DDR_A[13]	DQ7	DQ3	DQ1
AE12	VSS	VSS	–	–	–	–
AE13	VREF_B5_DOWN	B5	–	–	–	–
AE14	VDD	VDD	–	–	–	–
AE15	VSS	VSS	–	–	–	–
AE16	VDDL	VDD	–	–	–	–
AE17	VSS	VSS	–	–	–	–
AE18	VDD	VDD	–	–	–	–
AE19	VSS	VSS	–	–	–	–
AE20	VDDL	VDD	–	–	–	–
AE21	VSS	VSS	–	–	–	–
AE22	VDD	VDD	–	–	–	–
AE23	VSS	VSS	–	–	–	–
AE24	VDDL	VDD	–	–	–	–
AE25	VSS	VSS	–	–	–	–
AE26	VDD	VDD	–	–	–	–
AE27	VSS	VSS	–	–	–	–
AE28	VDDL	VDD	–	–	–	–
AE29	VSS	VSS	–	–	–	–
AE30	VDD	VDD	–	–	–	–
AE31	VSS	VSS	–	–	–	–
AE32	VREF_B2_DOWN	B2	–	–	–	–
AE33	VSS	VSS	–	–	–	–
AE34	P_D43N_B3	B3	DDR_A[13]	DQ7	DQ3	DQ1
AE35	P_D45N_B3	B3	DDR_BA[1]	DQ7	DQ3	DQ1
AE36	N/C	–	–	–	–	–
AE37	P_D46N_B2	B2	DQ5	DQ8	DQ4	DQ2
AE38	P_D44N_B2	B2	DQ5	DQ8	DQ4	DQ2
AE39	P_D40N_B2	B2	DQ6	DQ9	DQ4	DQ2
AE40	P_D39N_B2	B2	DQSN6	DQSN9	DQ4	DQSN2

Table 45: *FG1892 Pin Listing for SPD60*

Pin	Pin Name	Group	DDR123 Hard Controller (x8)	x8/x9 DQ–QS	x16/x18 DQ–QS	x32/x36 DQ–QS
AE41	P_D34P_B2	B2	DQ7	DQ10	DQ5	DQ2
AE42	P_D34N_B2	B2	DQ7	DQ10	DQ5	DQ2
AE43	P_D33N_B2	B2	DQSN7	DQSN10	DQSN5	DQ2
AE44	P_D33P_B2	B2	DQSP7	DQSP10	DQSP5	DQ2
AF1	P_D41N_B4	B4	DDR_A[9]	DQ6	DQ3	DQ1
AF2	P_D41P_B4	B4	DDR_A[8]	DQ6	DQ3	DQ1
AF3	P_D35N_B5	B5	DQ7	DQ10	DQ5	DQ2
AF4	P_D35P_B5	B5	DQ7	DQ10	DQ5	DQ2
AF5	P_D39P_B5	B5	DQSP6	DQSP9	DQ4	DQSP2
AF6	P_D40P_B5	B5	DQ6	DQ9	DQ4	DQ2
AF7	P_D44P_B5	B5	DQ5	DQ8	DQ4	DQ2
AF8	P_D46P_B5	B5	DQ5	DQ8	DQ4	DQ2
AF9	N/C	–	–	–	–	–
AF10	P_D45P_B4	B4	DDR_BA[0]	DQ7	DQ3	DQ1
AF11	P_D43P_B4	B4	DDR_A[12]	DQ7	DQ3	DQ1
AF12	P_RTTHI_B5	B5	–	–	–	–
AF13	VREF_B4	B4	–	–	–	–
AF14	VSS	VSS	–	–	–	–
AF15	VDD	VDD	–	–	–	–
AF16	VSS	VSS	–	–	–	–
AF17	VDDL	VDD	–	–	–	–
AF18	VSS	VSS	–	–	–	–
AF19	VDD	VDD	–	–	–	–
AF20	VSS	VSS	–	–	–	–
AF21	VDDL	VDD	–	–	–	–
AF22	VSS	VSS	–	–	–	–
AF23	VDD	VDD	–	–	–	–
AF24	VSS	VSS	–	–	–	–
AF25	VDDL	VDD	–	–	–	–
AF26	VSS	VSS	–	–	–	–
AF27	VDD	VDD	–	–	–	–
AF28	VSS	VSS	–	–	–	–
AF29	VDDL	VDD	–	–	–	–
AF30	VSS	VSS	–	–	–	–
AF31	VDD	VDD	–	–	–	–
AF32	VREF_B3	B3	–	–	–	–
AF33	P_RTTHI_B2	B2	–	–	–	–
AF34	P_D43P_B3	B3	DDR_A[12]	DQ7	DQ3	DQ1
AF35	P_D45P_B3	B3	DDR_BA[0]	DQ7	DQ3	DQ1
AF36	N/C	–	–	–	–	–
AF37	P_D46P_B2	B2	DQ5	DQ8	DQ4	DQ2
AF38	P_D44P_B2	B2	DQ5	DQ8	DQ4	DQ2
AF39	P_D40P_B2	B2	DQ6	DQ9	DQ4	DQ2
AF40	P_D39P_B2	B2	DQSP6	DQSP9	DQ4	DQSP2

Table 45: *FG1892 Pin Listing for SPD60*

Pin	Pin Name	Group	DDR123 Hard Controller (x8)	x8/x9 DQ–QS	x16/x18 DQ–QS	x32/x36 DQ–QS
AF41	P_D35P_B2	B2	DQ7	DQ10	DQ5	DQ2
AF42	P_D35N_B2	B2	DQ7	DQ10	DQ5	DQ2
AF43	P_D41N_B3	B3	DDR_A[9]	DQ6	DQ3	DQ1
AF44	P_D41P_B3	B3	DDR_A[8]	DQ6	DQ3	DQ1
AG1	P_D40N_B4	B4	DDR_A[7]	DQ6	DQ3	DQ1
AG2	P_D40P_B4	B4	DDR_A[6]	DQ6	DQ3	DQ1
AG3	P_D39N_B4	B4	DDR_A[5]	DQ6	DQ3	DQ1
AG4	P_D39P_B4	B4	DDR_A[4]	DQ6	DQ3	DQ1
AG5	P_D41N_B5	B5	DQ6	DQ9	DQ4	DQ2
AG6	VSS	VSS	–	–	–	–
AG7	P_D45N_B5	B5	DQSN5	DQSN8	DQSN4	DQ2
AG8	P_D47N_B5	B5	DQ5	DQ8	DQ4	DQ2
AG9	VSS	VSS	–	–	–	–
AG10	P_D44N_B4	B4	DDR_CLKN[2]	DQSN7	DQ3	DQ1
AG11	P_D42N_B4	B4	DDR_A[11]	DQ7	DQ3	DQ1
AG12	VDDO_B4	B4	–	–	–	–
AG13	VREF_B4	B4	–	–	–	–
AG14	VDD	VDD	–	–	–	–
AG15	VSS	VSS	–	–	–	–
AG16	VDDL	VDD	–	–	–	–
AG17	VSS	VSS	–	–	–	–
AG18	VDD	VDD	–	–	–	–
AG19	VSS	VSS	–	–	–	–
AG20	VDDL	VDD	–	–	–	–
AG21	VSS	VSS	–	–	–	–
AG22	VDD	VDD	–	–	–	–
AG23	VSS	VSS	–	–	–	–
AG24	VDDL	VDD	–	–	–	–
AG25	VSS	VSS	–	–	–	–
AG26	VDD	VDD	–	–	–	–
AG27	VSS	VSS	–	–	–	–
AG28	VDDL	VDD	–	–	–	–
AG29	VSS	VSS	–	–	–	–
AG30	VDD	VDD	–	–	–	–
AG31	VSS	VSS	–	–	–	–
AG32	VREF_B3	B3	–	–	–	–
AG33	VDDO_B3	B3	–	–	–	–
AG34	P_D42N_B3	B3	DDR_A[11]	DQ7	DQ3	DQ1
AG35	P_D44N_B3	B3	DDR_CLKN[2]	DQSN7	DQ3	DQ1
AG36	VSS	VSS	–	–	–	–
AG37	P_D47N_B2	B2	DQ5	DQ8	DQ4	DQ2
AG38	P_D45N_B2	B2	DQSN5	DQSN8	DQSN4	DQ2
AG39	VSS	VSS	–	–	–	–
AG40	P_D41N_B2	B2	DQ6	DQ9	DQ4	DQ2

Table 45: *FG1892 Pin Listing for SPD60*

Pin	Pin Name	Group	DDR123 Hard Controller (x8)	x8/x9 DQ–QS	x16/x18 DQ–QS	x32/x36 DQ–QS
AG41	P_D39P_B3	B3	DDR_A[4]	DQ6	DQ3	DQ1
AG42	P_D39N_B3	B3	DDR_A[5]	DQ6	DQ3	DQ1
AG43	P_D40N_B3	B3	DDR_A[7]	DQ6	DQ3	DQ1
AG44	P_D40P_B3	B3	DDR_A[6]	DQ6	DQ3	DQ1
AH1	P_D38N_B4	B4	DDR_CLKN[1]	DQSN6	DQSN3	DQ1
AH2	P_D38P_B4	B4	DDR_CLKP[1]	DQSP6	DQSP3	DQ1
AH3	VDDO_B4	B4	–	–	–	–
AH4	VSS	VSS	–	–	–	–
AH5	P_D41P_B5	B5	DQ6	DQ9	DQ4	DQ2
AH6	VDDO_B4	B4	–	–	–	–
AH7	P_D45P_B5	B5	DQSP5	DQSP8	DQSP4	DQ2
AH8	P_D47P_B5	B5	DQ5	DQ8	DQ4	DQ2
AH9	VDDO_B4	B4	–	–	–	–
AH10	P_D44P_B4	B4	DDR_CLKP[2]	DQSP7	DQ3	DQ1
AH11	P_D42P_B4	B4	DDR_A[10]	DQ7	DQ3	DQ1
AH12	VSS	VSS	–	–	–	–
AH13	VDDL	VDD	–	–	–	–
AH14	PLL_VSSA0_SE	PLL_SE	–	–	–	–
AH15	VDD	VDD	–	–	–	–
AH16	VSS	VSS	–	–	–	–
AH17	VDDL	VDD	–	–	–	–
AH18	VSS	VSS	–	–	–	–
AH19	VDD	VDD	–	–	–	–
AH20	VSS	VSS	–	–	–	–
AH21	VDDL	VDD	–	–	–	–
AH22	VSS	VSS	–	–	–	–
AH23	VDD	VDD	–	–	–	–
AH24	VSS	VSS	–	–	–	–
AH25	VDDL	VDD	–	–	–	–
AH26	VSS	VSS	–	–	–	–
AH27	VDD	VDD	–	–	–	–
AH28	VSS	VSS	–	–	–	–
AH29	VDDL	VDD	–	–	–	–
AH30	VSS	VSS	–	–	–	–
AH31	PLL_VSSA0_SW	PLL_SW	–	–	–	–
AH32	VDDL	VDD	–	–	–	–
AH33	VSS	VSS	–	–	–	–
AH34	P_D42P_B3	B3	DDR_A[10]	DQ7	DQ3	DQ1
AH35	P_D44P_B3	B3	DDR_CLKP[2]	DQSP7	DQ3	DQ1
AH36	VDDO_B3	B3	–	–	–	–
AH37	P_D47P_B2	B2	DQ5	DQ8	DQ4	DQ2
AH38	P_D45P_B2	B2	DQSP5	DQSP8	DQSP4	DQ2
AH39	VDDO_B3	B3	–	–	–	–
AH40	P_D41P_B2	B2	DQ6	DQ9	DQ4	DQ2

Table 45: *FG1892 Pin Listing for SPD60*

Pin	Pin Name	Group	DDR123 Hard Controller (x8)	x8/x9 DQ–QS	x16/x18 DQ–QS	x32/x36 DQ–QS
AH41	VSS	VSS	–	–	–	–
AH42	VDDO_B3	B3	–	–	–	–
AH43	P_D38N_B3	B3	DDR_CLKN[1]	DQSN6	DQSN3	DQ1
AH44	P_D38P_B3	B3	DDR_CLKP[1]	DQSP6	DQSP3	DQ1
AJ1	P_D37N_B4	B4	DDR_A[3]	DQ6	DQ3	DQ1
AJ2	P_D37P_B4	B4	DDR_A[2]	DQ6	DQ3	DQ1
AJ3	P_D36N_B4	B4	DDR_A[1]	DQ6	DQ3	DQ1
AJ4	P_D36P_B4	B4	DDR_A[0]	DQ6	DQ3	DQ1
AJ5	P_D29N_B4	B4	RESERVED	DQ4	DQ2	DQ1
AJ6	P_D28N_B4	B4	DQ4	DQ4	DQ2	DQ1
AJ7	P_D23N_B4	B4	RESERVED	DQ3	DQ1	DQ0
AJ8	P_D22N_B4	B4	DQ3	DQ3	DQ1	DQ0
AJ9	N/C	–	–	–	–	–
AJ10	P_D17N_B4	B4	RESERVED	DQ2	DQ1	DQ0
AJ11	P_D16N_B4	B4	DQ2	DQ2	DQ1	DQ0
AJ12	VDDO_B4	B4	–	–	–	–
AJ13	VSS	VSS	–	–	–	–
AJ14	PLL_VDDA0_SE	PLL_SE	–	–	–	–
AJ15	VSS	VSS	–	–	–	–
AJ16	VDDL	VDD	–	–	–	–
AJ17	VSS	VSS	–	–	–	–
AJ18	VDD	VDD	–	–	–	–
AJ19	VSS	VSS	–	–	–	–
AJ20	VDDL	VDD	–	–	–	–
AJ21	VSS	VSS	–	–	–	–
AJ22	VDD	VDD	–	–	–	–
AJ23	VSS	VSS	–	–	–	–
AJ24	VDDL	VDD	–	–	–	–
AJ25	VSS	VSS	–	–	–	–
AJ26	VDD	VDD	–	–	–	–
AJ27	VSS	VSS	–	–	–	–
AJ28	VDDL	VDD	–	–	–	–
AJ29	VSS	VSS	–	–	–	–
AJ30	VDD	VDD	–	–	–	–
AJ31	PLL_VDDA0_SW	PLL_SW	–	–	–	–
AJ32	VSS	VSS	–	–	–	–
AJ33	VDDO_B3	B3	–	–	–	–
AJ34	P_D16N_B3	B3	DQ2	DQ2	DQ1	DQ0
AJ35	P_D17N_B3	B3	RESERVED	DQ2	DQ1	DQ0
AJ36	N/C	–	–	–	–	–
AJ37	P_D22N_B3	B3	DQ3	DQ3	DQ1	DQ0
AJ38	P_D23N_B3	B3	RESERVED	DQ3	DQ1	DQ0
AJ39	P_D28N_B3	B3	DQ4	DQ4	DQ2	DQ1
AJ40	P_D29N_B3	B3	RESERVED	DQ4	DQ2	DQ1

Table 45: *FG1892 Pin Listing for SPD60*

Pin	Pin Name	Group	DDR123 Hard Controller (x8)	x8/x9 DQ–QS	x16/x18 DQ–QS	x32/x36 DQ–QS
AJ41	P_D36P_B3	B3	DDR_A[0]	DQ6	DQ3	DQ1
AJ42	P_D36N_B3	B3	DDR_A[1]	DQ6	DQ3	DQ1
AJ43	P_D37N_B3	B3	DDR_A[3]	DQ6	DQ3	DQ1
AJ44	P_D37P_B3	B3	DDR_A[2]	DQ6	DQ3	DQ1
AK1	P_D35N_B4	B4	DDR_A[15]	DQ5	DQ2	DQ1
AK2	P_D35P_B4	B4	DDR_A[14]	DQ5	DQ2	DQ1
AK3	P_D34N_B4	B4	–	DQ5	DQ2	DQ1
AK4	P_D34P_B4	B4	RESET	DQ5	DQ2	DQ1
AK5	P_D29P_B4	B4	DM	DQ4	DQ2	DQ1
AK6	P_D28P_B4	B4	DQ4	DQ4	DQ2	DQ1
AK7	P_D23P_B4	B4	DM	DQ3	DQ1	DQ0
AK8	P_D22P_B4	B4	DQ3	DQ3	DQ1	DQ0
AK9	N/C	–	–	–	–	–
AK10	P_D17P_B4	B4	DM	DQ2	DQ1	DQ0
AK11	P_D16P_B4	B4	DQ2	DQ2	DQ1	DQ0
AK12	N/C	–	–	–	–	–
AK13	VDDL	VDD	–	–	–	–
AK14	PLL_VDDA1_SE	PLL_SE	–	–	–	–
AK15	PLL_VSSA0_SE	PLL_SE	–	–	–	–
AK16	VSS	VSS	–	–	–	–
AK17	VDDL	VDD	–	–	–	–
AK18	VSS	VSS	–	–	–	–
AK19	VDD	VDD	–	–	–	–
AK20	VSS	VSS	–	–	–	–
AK21	VDDL	VDD	–	–	–	–
AK22	VSS	VSS	–	–	–	–
AK23	VDD	VDD	–	–	–	–
AK24	VSS	VSS	–	–	–	–
AK25	VDDL	VDD	–	–	–	–
AK26	VSS	VSS	–	–	–	–
AK27	VDD	VDD	–	–	–	–
AK28	VSS	VSS	–	–	–	–
AK29	VDDL	VDD	–	–	–	–
AK30	PLL_VSSA0_SW	PLL_SW	–	–	–	–
AK31	PLL_VDDA1_SW	PLL_SW	–	–	–	–
AK32	VDDL	VDD	–	–	–	–
AK33	N/C	–	–	–	–	–
AK34	P_D16P_B3	B3	DQ2	DQ2	DQ1	DQ0
AK35	P_D17P_B3	B3	DM	DQ2	DQ1	DQ0
AK36	N/C	–	–	–	–	–
AK37	P_D22P_B3	B3	DQ3	DQ3	DQ1	DQ0
AK38	P_D23P_B3	B3	DM	DQ3	DQ1	DQ0
AK39	P_D28P_B3	B3	DQ4	DQ4	DQ2	DQ1
AK40	P_D29P_B3	B3	DM	DQ4	DQ2	DQ1

Table 45: *FG1892 Pin Listing for SPD60*

Pin	Pin Name	Group	DDR123 Hard Controller (x8)	x8/x9 DQ–QS	x16/x18 DQ–QS	x32/x36 DQ–QS
AK41	P_D34P_B3	B3	RESET	DQ5	DQ2	DQ1
AK42	P_D34N_B3	B3	–	DQ5	DQ2	DQ1
AK43	P_D35N_B3	B3	DDR_A[15]	DQ5	DQ2	DQ1
AK44	P_D35P_B3	B3	DDR_A[14]	DQ5	DQ2	DQ1
AL1	P_D32N_B4	B4	DDR_CLKN[0]	DQSN5	DQ2	DQSN1
AL2	P_D32P_B4	B4	DDR_CLKP[0]	DQSP5	DQ2	DQSP1
AL3	P_D33N_B4	B4	ODT[1]	DQ5	DQ2	DQ1
AL4	P_D33P_B4	B4	ODT[0]	DQ5	DQ2	DQ1
AL5	P_D26N_B4	B4	DQSN4	DQSN4	DQSN2	DQ1
AL6	P_D25N_B4	B4	DQ4	DQ4	DQ2	DQ1
AL7	P_D20N_B4	B4	DQSN3	DQSN3	DQ1	DQ0
AL8	P_D19N_B4	B4	DQ3	DQ3	DQ1	DQ0
AL9	VSS	VSS	–	–	–	–
AL10	P_D14N_B4	B4	DQSN2	DQSN2	DQSN1	DQ0
AL11	P_D13N_B4	B4	DQ2	DQ2	DQ1	DQ0
AL12	VSS	VSS	–	–	–	–
AL13	VSS	VSS	–	–	–	–
AL14	PLL_VSSA1_SE	PLL_SE	–	–	–	–
AL15	PLL_VDDA0_SE	PLL_SE	–	–	–	–
AL16	PLL_VSSA1_SE	PLL_SE	–	–	–	–
AL17	PLL_VDDA1_SE	PLL_SE	–	–	–	–
AL18	VDD	VDD	–	–	–	–
AL19	VSS	VSS	–	–	–	–
AL20	VDDL	VDD	–	–	–	–
AL21	VSS	VSS	–	–	–	–
AL22	VDD	VDD	–	–	–	–
AL23	VSS	VSS	–	–	–	–
AL24	VDDL	VDD	–	–	–	–
AL25	VSS	VSS	–	–	–	–
AL26	VDD	VDD	–	–	–	–
AL27	VSS	VSS	–	–	–	–
AL28	PLL_VDDA1_SW	PLL_SW	–	–	–	–
AL29	PLL_VSSA1_SW	PLL_SW	–	–	–	–
AL30	PLL_VDDA0_SW	PLL_SW	–	–	–	–
AL31	PLL_VSSA1_SW	PLL_SW	–	–	–	–
AL32	VSS	VSS	–	–	–	–
AL33	VSS	VSS	–	–	–	–
AL34	P_D13N_B3	B3	DQ2	DQ2	DQ1	DQ0
AL35	P_D14N_B3	B3	DQSN2	DQSN2	DQSN1	DQ0
AL36	VSS	VSS	–	–	–	–
AL37	P_D19N_B3	B3	DQ3	DQ3	DQ1	DQ0
AL38	P_D20N_B3	B3	DQSN3	DQSN3	DQ1	DQ0
AL39	P_D25N_B3	B3	DQ4	DQ4	DQ2	DQ1
AL40	P_D26N_B3	B3	DQSN4	DQSN4	DQSN2	DQ1

Table 45: *FG1892 Pin Listing for SPD60*

Pin	Pin Name	Group	DDR123 Hard Controller (x8)	x8/x9 DQ–QS	x16/x18 DQ–QS	x32/x36 DQ–QS
AL41	P_D33P_B3	B3	ODT[0]	DQ5	DQ2	DQ1
AL42	P_D33N_B3	B3	ODT[1]	DQ5	DQ2	DQ1
AL43	P_D32P_B3	B3	DDR_CLKP[0]	DQSP5	DQ2	DQSP1
AL44	P_D32N_B3	B3	DDR_CLKN[0]	DQSN5	DQ2	DQSN1
AM1	P_D31N_B4	B4	CKE[1]	DQ5	DQ2	DQ1
AM2	P_D31P_B4	B4	CKE[0]	DQ5	DQ2	DQ1
AM3	VDDO_B4	B4	–	–	–	–
AM4	VSS	VSS	–	–	–	–
AM5	P_D26P_B4	B4	DQSP4	DQSP4	DQSP2	DQ1
AM6	P_D25P_B4	B4	DQ4	DQ4	DQ2	DQ1
AM7	P_D20P_B4	B4	DQSP3	DQSP3	DQ1	DQ0
AM8	P_D19P_B4	B4	DQ3	DQ3	DQ1	DQ0
AM9	VDDO_B4	B4	–	–	–	–
AM10	P_D14P_B4	B4	DQSP2	DQSP2	DQSP1	DQ0
AM11	P_D13P_B4	B4	DQ2	DQ2	DQ1	DQ0
AM12	VDDO_B4	B4	–	–	–	–
AM13	VDDA_10GE	10GE	–	–	–	–
AM14	VDDA_10GE	10GE	–	–	–	–
AM15	VDDA_10GE	10GE	–	–	–	–
AM16	VDDA_10GE	10GE	–	–	–	–
AM17	VDDA_10GD	10GD	–	–	–	–
AM18	VDDA_10GD	10GD	–	–	–	–
AM19	VDDA_10GD	10GD	–	–	–	–
AM20	VDDA_10GD	10GD	–	–	–	–
AM21	VDDA_10GC	10GC	–	–	–	–
AM22	VDDA_10GC	10GC	–	–	–	–
AM23	VDDA_10GC	10GC	–	–	–	–
AM24	VDDA_10GC	10GC	–	–	–	–
AM25	VDDA_10GB	10GB	–	–	–	–
AM26	VDDA_10GB	10GB	–	–	–	–
AM27	VDDA_10GB	10GB	–	–	–	–
AM28	VDDA_10GB	10GB	–	–	–	–
AM29	VDDA_10GA	10GA	–	–	–	–
AM30	VDDA_10GA	10GA	–	–	–	–
AM31	VDDA_10GA	10GA	–	–	–	–
AM32	VDDA_10GA	10GA	–	–	–	–
AM33	VDDO_B3	B3	–	–	–	–
AM34	P_D13P_B3	B3	DQ2	DQ2	DQ1	DQ0
AM35	P_D14P_B3	B3	DQSP2	DQSP2	DQSP1	DQ0
AM36	VDDO_B3	B3	–	–	–	–
AM37	P_D19P_B3	B3	DQ3	DQ3	DQ1	DQ0
AM38	P_D20P_B3	B3	DQSP3	DQSP3	DQ1	DQ0
AM39	P_D25P_B3	B3	DQ4	DQ4	DQ2	DQ1
AM40	P_D26P_B3	B3	DQSP4	DQSP4	DQSP2	DQ1

Table 45: *FG1892 Pin Listing for SPD60*

Pin	Pin Name	Group	DDR123 Hard Controller (x8)	x8/x9 DQ–QS	x16/x18 DQ–QS	x32/x36 DQ–QS
AM41	VSS	VSS	–	–	–	–
AM42	VDDO_B3	B3	–	–	–	–
AM43	P_D31N_B3	B3	CKE[1]	DQ5	DQ2	DQ1
AM44	P_D31P_B3	B3	CKE[0]	DQ5	DQ2	DQ1
AN1	VSS	VSS	–	–	–	–
AN2	VSS	VSS	–	–	–	–
AN3	P_D30N_B4	B4	CS_N[1]	DQ5	DQ2	DQ1
AN4	P_D30P_B4	B4	CS_N[0]	DQ5	DQ2	DQ1
AN5	P_D27N_B4	B4	DQ4	DQ4	DQ2	DQ1
AN6	P_D24N_B4	B4	DQ4	DQ4	DQ2	DQ1
AN7	P_D21N_B4	B4	DQ3	DQ3	DQ1	DQ0
AN8	P_D18N_B4	B4	DQ3	DQ3	DQ1	DQ0
AN9	N/C	–	–	–	–	–
AN10	P_D15N_B4	B4	DQ2	DQ2	DQ1	DQ0
AN11	P_D12N_B4	B4	DQ2	DQ2	DQ1	DQ0
AN12	VREF_CB2	CB2	–	–	–	–
AN13	VREF_CB2	CB2	–	–	–	–
AN14	VDDO_CB2	CB2	–	–	–	–
AN15	VREF_BSE	BSE	–	–	–	–
AN16	VDDO_BSE	BSE	–	–	–	–
AN17	VSS	VSS	–	–	–	–
AN18	VREF_BSE	BSE	–	–	–	–
AN19	VSS	VSS	–	–	–	–
AN20	N/C	–	–	–	–	–
AN21	VSS	VSS	–	–	–	–
AN22	VDDO_BSE	BSE	–	–	–	–
AN23	VDDO_BSW	BSW	–	–	–	–
AN24	VSS	VSS	–	–	–	–
AN25	N/C	–	–	–	–	–
AN26	VSS	VSS	–	–	–	–
AN27	VREF_BSW	BSW	–	–	–	–
AN28	VSS	VSS	–	–	–	–
AN29	VDDO_BSW	BSW	–	–	–	–
AN30	VREF_BSW	BSW	–	–	–	–
AN31	VREF_CB1	CB1	–	–	–	–
AN32	VDDO_CB1	CB1	–	–	–	–
AN33	VREF_CB1	CB1	–	–	–	–
AN34	P_D12N_B3	B3	DQ2	DQ2	DQ1	DQ0
AN35	P_D15N_B3	B3	DQ2	DQ2	DQ1	DQ0
AN36	N/C	–	–	–	–	–
AN37	P_D18N_B3	B3	DQ3	DQ3	DQ1	DQ0
AN38	P_D21N_B3	B3	DQ3	DQ3	DQ1	DQ0
AN39	P_D24N_B3	B3	DQ4	DQ4	DQ2	DQ1
AN40	P_D27N_B3	B3	DQ4	DQ4	DQ2	DQ1

Table 45: *FG1892 Pin Listing for SPD60*

Pin	Pin Name	Group	DDR123 Hard Controller (x8)	x8/x9 DQ–QS	x16/x18 DQ–QS	x32/x36 DQ–QS
AN41	P_D30P_B3	B3	CS_N[0]	DQ5	DQ2	DQ1
AN42	P_D30N_B3	B3	CS_N[1]	DQ5	DQ2	DQ1
AN43	VSS	VSS	–	–	–	–
AN44	VSS	VSS	–	–	–	–
AP1	P_10GE_LN3_RXN_I	10GE	–	–	–	–
AP2	VSS	VSS	–	–	–	–
AP3	VDDHA_10GE	10GE	–	–	–	–
AP4	VDDO_B4	B4	–	–	–	–
AP5	P_D27P_B4	B4	DQ4	DQ4	DQ2	DQ1
AP6	P_D24P_B4	B4	DQ4	DQ4	DQ2	DQ1
AP7	P_D21P_B4	B4	DQ3	DQ3	DQ1	DQ0
AP8	P_D18P_B4	B4	DQ3	DQ3	DQ1	DQ0
AP9	VSS	VSS	–	–	–	–
AP10	P_D15P_B4	B4	DQ2	DQ2	DQ1	DQ0
AP11	P_D12P_B4	B4	DQ2	DQ2	DQ1	DQ0
AP12	P_D0P_CB2	CB2	–	–	–	–
AP13	P_D0N_CB2	CB2	–	–	–	–
AP14	VDDO_BSE	BSE	–	–	–	–
AP15	P_D0P_BSE(1)	BSE	–	–	–	–
AP16	P_D0N_BSE(1)	BSE	–	–	–	–
AP17	P_D6P_BSE	BSE	–	–	–	–
AP18	P_D6N_BSE	BSE	–	–	–	–
AP19	N/C	–	–	–	–	–
AP20	N/C	–	–	–	–	–
AP21	N/C	–	–	–	–	–
AP22	N/C	–	–	–	–	–
AP23	N/C	–	–	–	–	–
AP24	N/C	–	–	–	–	–
AP25	N/C	–	–	–	–	–
AP26	N/C	–	–	–	–	–
AP27	N/C	–	–	–	–	–
AP28	N/C	–	–	–	–	–
AP29	P_D0N_BSW(1)	BSW	–	–	–	–
AP30	P_D0P_BSW(1)	BSW	–	–	–	–
AP31	VDDO_BSW	BSW	–	–	–	–
AP32	P_D0N_CB1	CB1	–	–	–	–
AP33	P_D0P_CB1	CB1	–	–	–	–
AP34	P_D12P_B3	B3	DQ2	DQ2	DQ1	DQ0
AP35	P_D15P_B3	B3	DQ2	DQ2	DQ1	DQ0
AP36	N/C	–	–	–	–	–
AP37	P_D18P_B3	B3	DQ3	DQ3	DQ1	DQ0
AP38	P_D21P_B3	B3	DQ3	DQ3	DQ1	DQ0
AP39	P_D24P_B3	B3	DQ4	DQ4	DQ2	DQ1

Table 45: *FG1892 Pin Listing for SPD60*

Pin	Pin Name	Group	DDR123 Hard Controller (x8)	x8/x9 DQ–QS	x16/x18 DQ–QS	x32/x36 DQ–QS
AP40	P_D27P_B3	B3	DQ4	DQ4	DQ2	DQ1
AP41	VDDO_B3	B3	–	–	–	–
AP42	VDDHA_10GA	10GA	–	–	–	–
AP43	VSS	VSS	–	–	–	–
AP44	P_10GA_LN0_RXP_I	10GA	–	–	–	–
AR1	P_10GE_LN3_RXP_I	10GE	–	–	–	–
AR2	P_10GE_LN3_TXP_O	10GE	–	–	–	–
AR3	P_10GE_REFRES_I	10GE	–	–	–	–
AR4	VSS	VSS	–	–	–	–
AR5	P_D11N_B4	B4	RESERVED	DQ1	DQ0	DQ0
AR6	P_D8N_B4	B4	DQSN1	DQSN1	DQ0	DQSN0
AR7	P_D9N_B4	B4	DQ1	DQ1	DQ0	DQ0
AR8	VSS	VSS	–	–	–	–
AR9	P_D5N_B4	B4	RESERVED	DQ0	DQ0	DQ0
AR10	P_D2N_B4	B4	DQSN0	DQSN0	DQSN0	DQ0
AR11	P_D4N_B4	B4	DQ0	DQ0	DQ0	DQ0
AR12	VDDO_CB2	CB2	–	–	–	–
AR13	P_D1P_CB2	CB2	–	–	–	–
AR14	P_D1N_CB2	CB2	–	–	–	–
AR15	VSS	VSS	–	–	–	–
AR16	P_D5P_BSE	BSE	–	–	–	–
AR17	P_D5N_BSE	BSE	–	–	–	–
AR18	VDDO_BSE	BSE	–	–	–	–
AR19	P_D7P_BSE	BSE	–	–	–	–
AR20	P_D7N_BSE	BSE	–	–	–	–
AR21	N/C	–	–	–	–	–
AR22	N/C	–	–	–	–	–
AR23	N/C	–	–	–	–	–
AR24	N/C	–	–	–	–	–
AR25	TDI	JTAG	–	–	–	–
AR26	VDDO_JTAG	JTAG	–	–	–	–
AR27	VDDO_BSW	BSW	–	–	–	–
AR28	P_D1N_BSW(1)	BSW	–	–	–	–
AR29	P_D1P_BSW(1)	BSW	–	–	–	–
AR30	VSS	VSS	–	–	–	–
AR31	P_D1N_CB1	CB1	–	–	–	–
AR32	P_D1P_CB1	CB1	–	–	–	–
AR33	VDDO_CB1	CB1	–	–	–	–
AR34	P_D4N_B3	B3	DQ0	DQ0	DQ0	DQ0
AR35	P_D2N_B3	B3	DQSN0	DQSN0	DQSN0	DQ0
AR36	P_D5N_B3	B3	RESERVED	DQ0	DQ0	DQ0
AR37	VSS	VSS	–	–	–	–
AR38	P_D9N_B3	B3	DQ1	DQ1	DQ0	DQ0

Table 45: *FG1892 Pin Listing for SPD60*

Pin	Pin Name	Group	DDR123 Hard Controller (x8)	x8/x9 DQ–QS	x16/x18 DQ–QS	x32/x36 DQ–QS
AR39	P_D8N_B3	B3	DQSN1	DQSN1	DQ0	DQSN0
AR40	P_D11N_B3	B3	RESERVED	DQ1	DQ0	DQ0
AR41	VSS	VSS	–	–	–	–
AR42	P_10GA_REFRES_I	10GA	–	–	–	–
AR43	P_10GA_LN0_TXN_O	10GA	–	–	–	–
AR44	P_10GA_LN0_RXN_I	10GA	–	–	–	–
AT1	NB	NB	–	–	–	–
AT2	P_10GE_LN3_TXN_O	10GE	–	–	–	–
AT3	VDDT_10GE	10GE	–	–	–	–
AT4	VSS	VSS	–	–	–	–
AT5	P_D11P_B4	B4	DM	DQ1	DQ0	DQ0
AT6	P_D8P_B4	B4	DQSP1	DQSP1	DQ0	DQSP0
AT7	P_D9P_B4	B4	DQ1	DQ1	DQ0	DQ0
AT8	VDDO_B4	B4	–	–	–	–
AT9	P_D5P_B4	B4	DM	DQ0	DQ0	DQ0
AT10	P_D2P_B4	B4	DQSP0	DQSP0	DQSP0	DQ0
AT11	P_D4P_B4	B4	DQ0	DQ0	DQ0	DQ0
AT12	P_D2P_CB2	CB2	–	–	–	–
AT13	P_D2N_CB2	CB2	–	–	–	–
AT14	P_D1P_BSE(1)	BSE	–	–	–	–
AT15	P_D1N_BSE(1)	BSE	–	–	–	–
AT16	P_D4P_BSE	BSE	–	–	–	–
AT17	P_D4N_BSE	BSE	–	–	–	–
AT18	P_D8P_BSE	BSE	–	–	–	–
AT19	P_D8N_BSE	BSE	–	–	–	–
AT20	N/C	–	–	–	–	–
AT21	VDDO_BSE	BSE	–	–	–	–
AT22	N/C	–	–	–	–	–
AT23	N/C	–	–	–	–	–
AT24	VDDO_BSW	BSW	–	–	–	–
AT25	TCK	JTAG	–	–	–	–
AT26	TEMP_DIODE_P	TEMP	–	–	–	–
AT27	CONFIG_SYSCLK_BYPASS	CFG	–	–	–	–
AT28	SDO3	CFG	–	–	–	–
AT29	CSN2	CFG	–	–	–	–
AT30	P_D2N_BSW	BSW	–	–	–	–
AT31	P_D2P_BSW	BSW	–	–	–	–
AT32	P_D2N_CB1	CB1	–	–	–	–
AT33	P_D2P_CB1	CB1	–	–	–	–
AT34	P_D4P_B3	B3	DQ0	DQ0	DQ0	DQ0
AT35	P_D2P_B3	B3	DQSP0	DQSP0	DQSP0	DQ0
AT36	P_D5P_B3	B3	DM	DQ0	DQ0	DQ0
AT37	VDDO_B3	B3	–	–	–	–

Table 45: *FG1892 Pin Listing for SPD60*

Pin	Pin Name	Group	DDR123 Hard Controller (x8)	x8/x9 DQ–QS	x16/x18 DQ–QS	x32/x36 DQ–QS
AT38	P_D9P_B3	B3	DQ1	DQ1	DQ0	DQ0
AT39	P_D8P_B3	B3	DQSP1	DQSP1	DQ0	DQSP0
AT40	P_D11P_B3	B3	DM	DQ1	DQ0	DQ0
AT41	VSS	VSS	–	–	–	–
AT42	VDDT_10GA	10GA	–	–	–	–
AT43	P_10GA_LN0_TXP_O	10GA	–	–	–	–
AT44	NB	NB	–	–	–	–
AU1	NB	NB	–	–	–	–
AU2	P_10GE_LN2_TXP_O	10GE	–	–	–	–
AU3	P_10GE_ATEST_O	10GE	–	–	–	–
AU4	VSS	VSS	–	–	–	–
AU5	P_D10N_B4	B4	DQ1	DQ1	DQ0	DQ0
AU6	P_D7N_B4	B4	DQ1	DQ1	DQ0	DQ0
AU7	P_D6N_B4	B4	DQ1	DQ1	DQ0	DQ0
AU8	N/C	–	–	–	–	–
AU9	P_D3N_B4	B4	DQ0	DQ0	DQ0	DQ0
AU10	P_D1N_B4	B4	DQ0	DQ0	DQ0	DQ0
AU11	P_D0N_B4	B4	DQ0	DQ0	DQ0	DQ0
AU12	VDDO_B4	B4	–	–	–	–
AU13	N/C	–	–	–	–	–
AU14	VSS	VSS	–	–	–	–
AU15	P_D2P_BSE	BSE	–	–	–	–
AU16	P_D2N_BSE	BSE	–	–	–	–
AU17	P_D3P_BSE	BSE	–	–	–	–
AU18	P_D3N_BSE	BSE	–	–	–	–
AU19	VDDO_BSE	BSE	–	–	–	–
AU20	N/C	–	–	–	–	–
AU21	N/C	–	–	–	–	–
AU22	N/C	–	–	–	–	–
AU23	N/C	–	–	–	–	–
AU24	N/C	–	–	–	–	–
AU25	TRSTN	JTAG	–	–	–	–
AU26	TEMP_DIODE_N	TEMP	–	–	–	–
AU27	VSS	VSS	–	–	–	–
AU28	SDI	CFG	–	–	–	–
AU29	CONFIG_RSTN	CFG	–	–	–	–
AU30	VDDO_CFG	CFG	–	–	–	–
AU31	CSN3	CFG	–	–	–	–
AU32	CONFIG_STATUS	CFG	–	–	–	–
AU33	VDDO_B3	B3	–	–	–	–
AU34	P_D0N_B3	B3	DQ0	DQ0	DQ0	DQ0
AU35	P_D1N_B3	B3	DQ0	DQ0	DQ0	DQ0
AU36	P_D3N_B3	B3	DQ0	DQ0	DQ0	DQ0
AU37	N/C	–	–	–	–	–

Table 45: *FG1892 Pin Listing for SPD60*

Pin	Pin Name	Group	DDR123 Hard Controller (x8)	x8/x9 DQ–QS	x16/x18 DQ–QS	x32/x36 DQ–QS
AU38	P_D6N_B3	B3	DQ1	DQ1	DQ0	DQ0
AU39	P_D7N_B3	B3	DQ1	DQ1	DQ0	DQ0
AU40	P_D10N_B3	B3	DQ1	DQ1	DQ0	DQ0
AU41	VSS	VSS	–	–	–	–
AU42	P_10GA_ATEST_O	10GA	–	–	–	–
AU43	P_10GA_LN1_TXN_O	10GA	–	–	–	–
AU44	NB	NB	–	–	–	–
AV1	P_10GE_LN2_RXN_I	10GE	–	–	–	–
AV2	P_10GE_LN2_TXN_O	10GE	–	–	–	–
AV3	VDDT_10GE	10GE	–	–	–	–
AV4	VSS	VSS	–	–	–	–
AV5	P_D10P_B4	B4	DQ1	DQ1	DQ0	DQ0
AV6	P_D7P_B4	B4	DQ1	DQ1	DQ0	DQ0
AV7	P_D6P_B4	B4	DQ1	DQ1	DQ0	DQ0
AV8	N/C	–	–	–	–	–
AV9	P_D3P_B4	B4	DQ0	DQ0	DQ0	DQ0
AV10	P_D1P_B4	B4	DQ0	DQ0	DQ0	DQ0
AV11	P_D0P_B4	B4	DQ0	DQ0	DQ0	DQ0
AV12	N/C	–	–	–	–	–
AV13	N/C	–	–	–	–	–
AV14	N/C	–	–	–	–	–
AV15	VDDO_BSE	BSE	–	–	–	–
AV16	N/C	–	–	–	–	–
AV17	N/C	–	–	–	–	–
AV18	VSS	VSS	–	–	–	–
AV19	N/C	–	–	–	–	–
AV20	N/C	–	–	–	–	–
AV21	N/C	–	–	–	–	–
AV22	N/C	–	–	–	–	–
AV23	N/C	–	–	–	–	–
AV24	N/C	–	–	–	–	–
AV25	VDDO_JTAG	JTAG	–	–	–	–
AV26	TMS	JTAG	–	–	–	–
AV27	CONFIG_CLKSEL	CFG	–	–	–	–
AV28	SDO2	CFG	–	–	–	–
AV29	VSS	VSS	–	–	–	–
AV30	HOLDN	CFG	–	–	–	–
AV31	CONFIG_MODESEL2	CFG	–	–	–	–
AV32	VDDO_CFG	CFG	–	–	–	–
AV33	CONFIG_MODESEL1	CFG	–	–	–	–
AV34	P_D0P_B3	B3	DQ0	DQ0	DQ0	DQ0
AV35	P_D1P_B3	B3	DQ0	DQ0	DQ0	DQ0
AV36	P_D3P_B3	B3	DQ0	DQ0	DQ0	DQ0
AV37	N/C	–	–	–	–	–

Table 45: *FG1892 Pin Listing for SPD60*

Pin	Pin Name	Group	DDR123 Hard Controller (x8)	x8/x9 DQ–QS	x16/x18 DQ–QS	x32/x36 DQ–QS
AV38	P_D6P_B3	B3	DQ1	DQ1	DQ0	DQ0
AV39	P_D7P_B3	B3	DQ1	DQ1	DQ0	DQ0
AV40	P_D10P_B3	B3	DQ1	DQ1	DQ0	DQ0
AV41	VSS	VSS	–	–	–	–
AV42	VDDT_10GA	10GA	–	–	–	–
AV43	P_10GA_LN1_TXP_O	10GA	–	–	–	–
AV44	P_10GA_LN1_RXP_I	10GA	–	–	–	–
AW1	P_10GE_LN2_RXP_I	10GE	–	–	–	–
AW2	VSS	VSS	–	–	–	–
AW3	P_10GE_REFCLKP_I	10GE	–	–	–	–
AW4	VSS	VSS	–	–	–	–
AW5	VDDO_B4	B4	–	–	–	–
AW6	N/C	–	–	–	–	–
AW7	VDDO_B4	B4	–	–	–	–
AW8	VSS	VSS	–	–	–	–
AW9	P_RTTLO_CB2	CB2	–	–	–	–
AW10	P_RTTHI_CB2	CB2	–	–	–	–
AW11	VSS	VSS	–	–	–	–
AW12	N/C	–	–	–	–	–
AW13	N/C	–	–	–	–	–
AW14	N/C	–	–	–	–	–
AW15	N/C	–	–	–	–	–
AW16	N/C	–	–	–	–	–
AW17	N/C	–	–	–	–	–
AW18	N/C	–	–	–	–	–
AW19	N/C	–	–	–	–	–
AW20	N/C	–	–	–	–	–
AW21	VSS	VSS	–	–	–	–
AW22	N/C	–	–	–	–	–
AW23	N/C	–	–	–	–	–
AW24	N/C	–	–	–	–	–
AW25	N/C	–	–	–	–	–
AW26	TDO	JTAG	–	–	–	–
AW27	CPU_CLK	CFG	–	–	–	–
AW28	SCK	CFG	–	–	–	–
AW29	VDDO_CFG	CFG	–	–	–	–
AW30	CSN0	CFG	–	–	–	–
AW31	SDO0	CFG	–	–	–	–
AW32	CONFIG_DONE	CFG	–	–	–	–
AW33	PROGRAM_ENABLE0	CFG	–	–	–	–
AW34	VSS	VSS	–	–	–	–
AW35	P_RTTHI_CB1	CB1	–	–	–	–
AW36	P_RTTLO_CB1	CB1	–	–	–	–
AW37	VSS	VSS	–	–	–	–

Table 45: *FG1892 Pin Listing for SPD60*

Pin	Pin Name	Group	DDR123 Hard Controller (x8)	x8/x9 DQ–QS	x16/x18 DQ–QS	x32/x36 DQ–QS
AW38	VDDO_B3	B3	–	–	–	–
AW39	N/C	–	–	–	–	–
AW40	VDDO_B3	B3	–	–	–	–
AW41	VSS	VSS	–	–	–	–
AW42	P_10GA_REFCLKP_I	10GA	–	–	–	–
AW43	VSS	VSS	–	–	–	–
AW44	P_10GA_LN1_RXN_I	10GA	–	–	–	–
AY1	P_10GE_LN1_RXN_I	10GE	–	–	–	–
AY2	VSS	VSS	–	–	–	–
AY3	P_10GE_REFCLKN_I	10GE	–	–	–	–
AY4	VSS	VSS	–	–	–	–
AY5	P_RTTLO_B4	B4	–	–	–	–
AY6	P_DRVLO_B4	B4	–	–	–	–
AY7	N/C	–	–	–	–	–
AY8	N/C	–	–	–	–	–
AY9	P_DRVLO_CB2	CB2	–	–	–	–
AY10	P_DRVHI_CB2	CB2	–	–	–	–
AY11	N/C	–	–	–	–	–
AY12	N/C	–	–	–	–	–
AY13	N/C	–	–	–	–	–
AY14	N/C	–	–	–	–	–
AY15	N/C	–	–	–	–	–
AY16	N/C	–	–	–	–	–
AY17	N/C	–	–	–	–	–
AY18	N/C	–	–	–	–	–
AY19	N/C	–	–	–	–	–
AY20	N/C	–	–	–	–	–
AY21	N/C	–	–	–	–	–
AY22	N/C	–	–	–	–	–
AY23	N/C	–	–	–	–	–
AY24	N/C	–	–	–	–	–
AY25	N/C	–	–	–	–	–
AY26	N/C	–	–	–	–	–
AY27	N/C	–	–	–	–	–
AY28	CSN1	CFG	–	–	–	–
AY29	SDO1	CFG	–	–	–	–
AY30	N/C	–	–	–	–	–
AY31	VSS	VSS	–	–	–	–
AY32	CONFIG_MODESEL0	CFG	–	–	–	–
AY33	VDDQ0	VDD	–	–	–	–
AY34	VSS	VSS	–	–	–	–
AY35	P_DRVHI_CB1	CB1	–	–	–	–
AY36	P_DRVLO_CB1	CB1	–	–	–	–
AY37	N/C	–	–	–	–	–

Table 45: *FG1892 Pin Listing for SPD60*

Pin	Pin Name	Group	DDR123 Hard Controller (x8)	x8/x9 DQ–QS	x16/x18 DQ–QS	x32/x36 DQ–QS
AY38	N/C	–	–	–	–	–
AY39	P_DRVLO_B3	B3	–	–	–	–
AY40	P_RTTLO_B3	B3	–	–	–	–
AY41	VSS	VSS	–	–	–	–
AY42	P_10GA_REFCLKN_I	10GA	–	–	–	–
AY43	VSS	VSS	–	–	–	–
AY44	P_10GA_LN2_RXP_I	10GA	–	–	–	–
B1	NB	NB	–	–	–	–
B2	N/C	–	–	–	–	–
B3	N/C	–	–	–	–	–
B4	VSS	VSS	–	–	–	–
B5	VSS	VSS	–	–	–	–
B6	N/C	–	–	–	–	–
B7	N/C	–	–	–	–	–
B8	N/C	–	–	–	–	–
B9	N/C	–	–	–	–	–
B10	VSS	VSS	–	–	–	–
B11	VSS	VSS	–	–	–	–
B12	P_5GB_LN3_TXN_O	5GB	–	–	–	–
B13	P_5GB_LN3_TXP_O	5GB	–	–	–	–
B14	P_5GB_LN2_TXN_O	5GB	–	–	–	–
B15	P_5GB_LN2_TXP_O	5GB	–	–	–	–
B16	VSS	VSS	–	–	–	–
B17	VSS	VSS	–	–	–	–
B18	P_5GB_LN1_TXN_O	5GB	–	–	–	–
B19	P_5GB_LN1_TXP_O	5GB	–	–	–	–
B20	P_5GB_LN0_TXN_O	5GB	–	–	–	–
B21	P_5GB_LN0_TXP_O	5GB	–	–	–	–
B22	VSS	VSS	–	–	–	–
B23	VSS	VSS	–	–	–	–
B24	P_5GA_LN3_TXN_O	5GA	–	–	–	–
B25	P_5GA_LN3_TXP_O	5GA	–	–	–	–
B26	P_5GA_LN2_TXN_O	5GA	–	–	–	–
B27	P_5GA_LN2_TXP_O	5GA	–	–	–	–
B28	VSS	VSS	–	–	–	–
B29	VSS	VSS	–	–	–	–
B30	P_5GA_LN1_TXN_O	5GA	–	–	–	–
B31	P_5GA_LN1_TXP_O	5GA	–	–	–	–
B32	P_5GA_LN0_TXN_O	5GA	–	–	–	–
B33	P_5GA_LN0_TXP_O	5GA	–	–	–	–
B34	VSS	VSS	–	–	–	–
B35	VSS	VSS	–	–	–	–
B36	N/C	–	–	–	–	–
B37	N/C	–	–	–	–	–

Table 45: *FG1892 Pin Listing for SPD60*

Pin	Pin Name	Group	DDR123 Hard Controller (x8)	x8/x9 DQ–QS	x16/x18 DQ–QS	x32/x36 DQ–QS
B38	N/C	–	–	–	–	–
B39	N/C	–	–	–	–	–
B40	VSS	VSS	–	–	–	–
B41	VSS	VSS	–	–	–	–
B42	N/C	–	–	–	–	–
B43	N/C	–	–	–	–	–
B44	NB	NB	–	–	–	–
BA1	P_10GE_LN1_RXP_I	10GE	–	–	–	–
BA2	P_10GE_LN1_TXP_O	10GE	–	–	–	–
BA3	VDDHA_10GE	10GE	–	–	–	–
BA4	VSS	VSS	–	–	–	–
BA5	P_RTTHI_B4	B4	–	–	–	–
BA6	P_DRVHI_B4	B4	–	–	–	–
BA7	N/C	–	–	–	–	–
BA8	VSS	VSS	–	–	–	–
BA9	VSS	VSS	–	–	–	–
BA10	VSS	VSS	–	–	–	–
BA11	VSS	VSS	–	–	–	–
BA12	VSS	VSS	–	–	–	–
BA13	VSS	VSS	–	–	–	–
BA14	VDDO_BSE	BSE	–	–	–	–
BA15	N/C	–	–	–	–	–
BA16	N/C	–	–	–	–	–
BA17	N/C	–	–	–	–	–
BA18	VDDO_BSE	BSE	–	–	–	–
BA19	N/C	–	–	–	–	–
BA20	VSS	VSS	–	–	–	–
BA21	VSS	VSS	–	–	–	–
BA22	VSS	VSS	–	–	–	–
BA23	VSS	VSS	–	–	–	–
BA24	VSS	VSS	–	–	–	–
BA25	VSS	VSS	–	–	–	–
BA26	N/C	–	–	–	–	–
BA27	VDDO_BSW	BSW	–	–	–	–
BA28	N/C	–	–	–	–	–
BA29	N/C	–	–	–	–	–
BA30	N/C	–	–	–	–	–
BA31	N/C	–	–	–	–	–
BA32	VSS	VSS	–	–	–	–
BA33	VSS	VSS	–	–	–	–
BA34	VSS	VSS	–	–	–	–
BA35	VSS	VSS	–	–	–	–
BA36	VSS	VSS	–	–	–	–
BA37	VSS	VSS	–	–	–	–

Table 45: *FG1892 Pin Listing for SPD60*

Pin	Pin Name	Group	DDR123 Hard Controller (x8)	x8/x9 DQ–QS	x16/x18 DQ–QS	x32/x36 DQ–QS
BA38	N/C	–	–	–	–	–
BA39	P_DRVHI_B3	B3	–	–	–	–
BA40	P_RTTHI_B3	B3	–	–	–	–
BA41	VSS	VSS	–	–	–	–
BA42	VDDHA_10GA	10GA	–	–	–	–
BA43	P_10GA_LN2_TXN_O	10GA	–	–	–	–
BA44	P_10GA_LN2_RXN_I	10GA	–	–	–	–
BB1	NB	NB	–	–	–	–
BB2	P_10GE_LN1_TXN_O	10GE	–	–	–	–
BB3	VDDT_10GE	10GE	–	–	–	–
BB4	VSS	VSS	–	–	–	–
BB5	VSS	VSS	–	–	–	–
BB6	VDDT_10GD	10GD	–	–	–	–
BB7	VDDHA_10GD	10GD	–	–	–	–
BB8	P_10GD_ATEST_O	10GD	–	–	–	–
BB9	VDDT_10GD	10GD	–	–	–	–
BB10	P_10GD_REFCLKN_I	10GD	–	–	–	–
BB11	P_10GD_REFCLKP_I	10GD	–	–	–	–
BB12	VDDT_10GD	10GD	–	–	–	–
BB13	P_10GD_REFRES_I	10GD	–	–	–	–
BB14	VDDHA_10GD	10GD	–	–	–	–
BB15	VSS	VSS	–	–	–	–
BB16	VSS	VSS	–	–	–	–
BB17	VSS	VSS	–	–	–	–
BB18	VDDT_10GC	10GC	–	–	–	–
BB19	VDDHA_10GC	10GC	–	–	–	–
BB20	P_10GC_ATEST_O	10GC	–	–	–	–
BB21	VDDT_10GC	10GC	–	–	–	–
BB22	P_10GC_REFCLKN_I	10GC	–	–	–	–
BB23	P_10GC_REFCLKP_I	10GC	–	–	–	–
BB24	VDDT_10GC	10GC	–	–	–	–
BB25	P_10GC_REFRES_I	10GC	–	–	–	–
BB26	VDDHA_10GC	10GC	–	–	–	–
BB27	VSS	VSS	–	–	–	–
BB28	VSS	VSS	–	–	–	–
BB29	VSS	VSS	–	–	–	–
BB30	VDDT_10GB	10GB	–	–	–	–
BB31	VDDHA_10GB	10GB	–	–	–	–
BB32	P_10GB_ATEST_O	10GB	–	–	–	–
BB33	VDDT_10GB	10GB	–	–	–	–
BB34	P_10GB_REFCLKN_I	10GB	–	–	–	–
BB35	P_10GB_REFCLKP_I	10GB	–	–	–	–
BB36	VDDT_10GB	10GB	–	–	–	–
BB37	P_10GB_REFRES_I	10GB	–	–	–	–

Table 45: *FG1892 Pin Listing for SPD60*

Pin	Pin Name	Group	DDR123 Hard Controller (x8)	x8/x9 DQ–QS	x16/x18 DQ–QS	x32/x36 DQ–QS
BB38	VDDHA_10GB	10GB	–	–	–	–
BB39	VSS	VSS	–	–	–	–
BB40	VSS	VSS	–	–	–	–
BB41	VSS	VSS	–	–	–	–
BB42	VDDT_10GA	10GA	–	–	–	–
BB43	P_10GA_LN2_TXP_O	10GA	–	–	–	–
BB44	NB	NB	–	–	–	–
BC1	NB	NB	–	–	–	–
BC2	P_10GE_LN0_TXP_O	10GE	–	–	–	–
BC3	P_10GE_LN0_TXN_O	10GE	–	–	–	–
BC4	VSS	VSS	–	–	–	–
BC5	VSS	VSS	–	–	–	–
BC6	P_10GD_LN3_TXP_O	10GD	–	–	–	–
BC7	P_10GD_LN3_TXN_O	10GD	–	–	–	–
BC8	P_10GD_LN2_TXP_O	10GD	–	–	–	–
BC9	P_10GD_LN2_TXN_O	10GD	–	–	–	–
BC10	VSS	VSS	–	–	–	–
BC11	VSS	VSS	–	–	–	–
BC12	P_10GD_LN1_TXP_O	10GD	–	–	–	–
BC13	P_10GD_LN1_TXN_O	10GD	–	–	–	–
BC14	P_10GD_LN0_TXP_O	10GD	–	–	–	–
BC15	P_10GD_LN0_TXN_O	10GD	–	–	–	–
BC16	VSS	VSS	–	–	–	–
BC17	VSS	VSS	–	–	–	–
BC18	P_10GC_LN3_TXP_O	10GC	–	–	–	–
BC19	P_10GC_LN3_TXN_O	10GC	–	–	–	–
BC20	P_10GC_LN2_TXP_O	10GC	–	–	–	–
BC21	P_10GC_LN2_TXN_O	10GC	–	–	–	–
BC22	VSS	VSS	–	–	–	–
BC23	VSS	VSS	–	–	–	–
BC24	P_10GC_LN1_TXP_O	10GC	–	–	–	–
BC25	P_10GC_LN1_TXN_O	10GC	–	–	–	–
BC26	P_10GC_LN0_TXP_O	10GC	–	–	–	–
BC27	P_10GC_LN0_TXN_O	10GC	–	–	–	–
BC28	VSS	VSS	–	–	–	–
BC29	VSS	VSS	–	–	–	–
BC30	P_10GB_LN3_TXP_O	10GB	–	–	–	–
BC31	P_10GB_LN3_TXN_O	10GB	–	–	–	–
BC32	P_10GB_LN2_TXP_O	10GB	–	–	–	–
BC33	P_10GB_LN2_TXN_O	10GB	–	–	–	–
BC34	VSS	VSS	–	–	–	–
BC35	VSS	VSS	–	–	–	–
BC36	P_10GB_LN1_TXP_O	10GB	–	–	–	–
BC37	P_10GB_LN1_TXN_O	10GB	–	–	–	–

Table 45: *FG1892 Pin Listing for SPD60*

Pin	Pin Name	Group	DDR123 Hard Controller (x8)	x8/x9 DQ–QS	x16/x18 DQ–QS	x32/x36 DQ–QS
BC38	P_10GB_LN0_TXP_O	10GB	–	–	–	–
BC39	P_10GB_LN0_TXN_O	10GB	–	–	–	–
BC40	VSS	VSS	–	–	–	–
BC41	VSS	VSS	–	–	–	–
BC42	P_10GA_LN3_TXP_O	10GA	–	–	–	–
BC43	P_10GA_LN3_TXN_O	10GA	–	–	–	–
BC44	NB	NB	–	–	–	–
BD1	NB	NB	–	–	–	–
BD2	NB	NB	–	–	–	–
BD3	P_10GE_LN0_RXN_I	10GE	–	–	–	–
BD4	P_10GE_LN0_RXP_I	10GE	–	–	–	–
BD5	P_10GD_LN3_RXN_I	10GD	–	–	–	–
BD6	P_10GD_LN3_RXP_I	10GD	–	–	–	–
BD7	NB	NB	–	–	–	–
BD8	NB	NB	–	–	–	–
BD9	P_10GD_LN2_RXN_I	10GD	–	–	–	–
BD10	P_10GD_LN2_RXP_I	10GD	–	–	–	–
BD11	P_10GD_LN1_RXN_I	10GD	–	–	–	–
BD12	P_10GD_LN1_RXP_I	10GD	–	–	–	–
BD13	NB	NB	–	–	–	–
BD14	NB	NB	–	–	–	–
BD15	P_10GD_LN0_RXN_I	10GD	–	–	–	–
BD16	P_10GD_LN0_RXP_I	10GD	–	–	–	–
BD17	P_10GC_LN3_RXN_I	10GC	–	–	–	–
BD18	P_10GC_LN3_RXP_I	10GC	–	–	–	–
BD19	NB	NB	–	–	–	–
BD20	NB	NB	–	–	–	–
BD21	P_10GC_LN2_RXN_I	10GC	–	–	–	–
BD22	P_10GC_LN2_RXP_I	10GC	–	–	–	–
BD23	P_10GC_LN1_RXN_I	10GC	–	–	–	–
BD24	P_10GC_LN1_RXP_I	10GC	–	–	–	–
BD25	NB	NB	–	–	–	–
BD26	NB	NB	–	–	–	–
BD27	P_10GC_LN0_RXN_I	10GC	–	–	–	–
BD28	P_10GC_LN0_RXP_I	10GC	–	–	–	–
BD29	P_10GB_LN3_RXN_I	10GB	–	–	–	–
BD30	P_10GB_LN3_RXP_I	10GB	–	–	–	–
BD31	NB	NB	–	–	–	–
BD32	NB	NB	–	–	–	–
BD33	P_10GB_LN2_RXN_I	10GB	–	–	–	–
BD34	P_10GB_LN2_RXP_I	10GB	–	–	–	–
BD35	P_10GB_LN1_RXN_I	10GB	–	–	–	–
BD36	P_10GB_LN1_RXP_I	10GB	–	–	–	–
BD37	NB	NB	–	–	–	–

Table 45: *FG1892 Pin Listing for SPD60*

Pin	Pin Name	Group	DDR123 Hard Controller (x8)	x8/x9 DQ–QS	x16/x18 DQ–QS	x32/x36 DQ–QS
BD38	NB	NB	–	–	–	–
BD39	P_10GB_LN0_RXN_I	10GB	–	–	–	–
BD40	P_10GB_LN0_RXP_I	10GB	–	–	–	–
BD41	P_10GA_LN3_RXN_I	10GA	–	–	–	–
BD42	P_10GA_LN3_RXP_I	10GA	–	–	–	–
BD43	NB	NB	–	–	–	–
BD44	NB	NB	–	–	–	–
C1	NB	NB	–	–	–	–
C2	N/C	–	–	–	–	–
C3	N/C	–	–	–	–	–
C4	N/C	–	–	–	–	–
C5	N/C	–	–	–	–	–
C6	N/C	–	–	–	–	–
C7	N/C	–	–	–	–	–
C8	N/C	–	–	–	–	–
C9	N/C	–	–	–	–	–
C10	N/C	–	–	–	–	–
C11	N/C	–	–	–	–	–
C12	VDDA_5GB	5GB	–	–	–	–
C13	VDDHA_5GB	5GB	–	–	–	–
C14	P_5GB_ATEST_O	5GB	–	–	–	–
C15	VDDA_5GB	5GB	–	–	–	–
C16	P_5GB_REFCLKN	5GB	–	–	–	–
C17	P_5GB_REFCLKP	5GB	–	–	–	–
C18	VDDA_5GB	5GB	–	–	–	–
C19	P_5GB_REFRES	5GB	–	–	–	–
C20	VDDHA_5GB	5GB	–	–	–	–
C21	VSS	VSS	–	–	–	–
C22	VSS	VSS	–	–	–	–
C23	VSS	VSS	–	–	–	–
C24	VDDA_5GA	5GA	–	–	–	–
C25	VDDHA_5GA	5GA	–	–	–	–
C26	P_5GA_ATEST_O	5GA	–	–	–	–
C27	VDDA_5GA	5GA	–	–	–	–
C28	P_5GA_REFCLKN	5GA	–	–	–	–
C29	P_5GA_REFCLKP	5GA	–	–	–	–
C30	VDDA_5GA	5GA	–	–	–	–
C31	P_5GA_REFRES	5GA	–	–	–	–
C32	VDDHA_5GA	5GA	–	–	–	–
C33	VSS	VSS	–	–	–	–
C34	N/C	–	–	–	–	–
C35	N/C	–	–	–	–	–
C36	N/C	–	–	–	–	–
C37	N/C	–	–	–	–	–

Table 45: *FG1892 Pin Listing for SPD60*

Pin	Pin Name	Group	DDR123 Hard Controller (x8)	x8/x9 DQ–QS	x16/x18 DQ–QS	x32/x36 DQ–QS
C38	N/C	–	–	–	–	–
C39	N/C	–	–	–	–	–
C40	N/C	–	–	–	–	–
C41	N/C	–	–	–	–	–
C42	N/C	–	–	–	–	–
C43	N/C	–	–	–	–	–
C44	NB	NB	–	–	–	–
D1	N/C	–	–	–	–	–
D2	N/C	–	–	–	–	–
D3	VSS	VSS	–	–	–	–
D4	VSS	VSS	–	–	–	–
D5	VSS	VSS	–	–	–	–
D6	VSS	VSS	–	–	–	–
D7	VSS	VSS	–	–	–	–
D8	N/C	–	–	–	–	–
D9	P_DRVLO_CB3	CB3	–	–	–	–
D10	P_DRVHI_CB3	CB3	–	–	–	–
D11	VDDO_BNE	BNE	–	–	–	–
D12	P_D0P_BNE(1)	BNE	–	–	–	–
D13	P_D0N_BNE(1)	BNE	–	–	–	–
D14	VDDO_BNE	BNE	–	–	–	–
D15	VSS	VSS	–	–	–	–
D16	VSS	VSS	–	–	–	–
D17	VSS	VSS	–	–	–	–
D18	VSS	VSS	–	–	–	–
D19	VSS	VSS	–	–	–	–
D20	VDDO_BNE	BNE	–	–	–	–
D21	P_D38P_BNE	BNE	–	–	–	–
D22	P_D38N_BNE	BNE	–	–	–	–
D23	P_D38N_BNW	BNW	–	–	–	–
D24	P_D38P_BNW	BNW	–	–	–	–
D25	VDDO_BNW	BNW	–	–	–	–
D26	VSS	VSS	–	–	–	–
D27	VSS	VSS	–	–	–	–
D28	VSS	VSS	–	–	–	–
D29	VSS	VSS	–	–	–	–
D30	VSS	VSS	–	–	–	–
D31	VDDO_BNW	BNW	–	–	–	–
D32	P_D0N_BNW(1)	BNW	–	–	–	–
D33	P_D0P_BNW(1)	BNW	–	–	–	–
D34	VDDO_BNW	BNW	–	–	–	–
D35	P_DRVHI_CB4	CB4	–	–	–	–
D36	P_DRVLO_CB4	CB4	–	–	–	–

Table 45: *FG1892 Pin Listing for SPD60*

Pin	Pin Name	Group	DDR123 Hard Controller (x8)	x8/x9 DQ–QS	x16/x18 DQ–QS	x32/x36 DQ–QS
D37	N/C	–	–	–	–	–
D38	VSS	VSS	–	–	–	–
D39	VSS	VSS	–	–	–	–
D40	VSS	VSS	–	–	–	–
D41	VSS	VSS	–	–	–	–
D42	VSS	VSS	–	–	–	–
D43	N/C	–	–	–	–	–
D44	N/C	–	–	–	–	–
E1	N/C	–	–	–	–	–
E2	VSS	VSS	–	–	–	–
E3	VSS	VSS	–	–	–	–
E4	VDDO_B6	B6	–	–	–	–
E5	VSS	VSS	–	–	–	–
E6	VDDO_B6	B6	–	–	–	–
E7	P_D7P_B6	B6	DQ1	DQ1	DQ0	DQ0
E8	P_D6P_B6	B6	DQ1	DQ1	DQ0	DQ0
E9	VDDO_B6	B6	–	–	–	–
E10	P_D1P_B6	B6	DQ0	DQ0	DQ0	DQ0
E11	P_D0P_B6	B6	DQ0	DQ0	DQ0	DQ0
E12	P_D1P_BNE(1)	BNE	–	–	–	–
E13	P_D1N_BNE(1)	BNE	–	–	–	–
E14	VSS	VSS	–	–	–	–
E15	P_D14P_BNE	BNE	–	–	–	–
E16	P_D14N_BNE	BNE	–	–	–	–
E17	VDDO_BNE	BNE	–	–	–	–
E18	P_D29P_BNE	BNE	–	–	–	–
E19	P_D29N_BNE	BNE	–	–	–	–
E20	VSS	VSS	–	–	–	–
E21	P_D37P_BNE	BNE	–	–	–	–
E22	VDDO_BNE	BNE	–	–	–	–
E23	VDDO_BNW	BNW	–	–	–	–
E24	P_D37P_BNW	BNW	–	–	–	–
E25	VSS	VSS	–	–	–	–
E26	P_D29N_BNW	BNW	–	–	–	–
E27	P_D29P_BNW	BNW	–	–	–	–
E28	VDDO_BNW	BNW	–	–	–	–
E29	P_D14N_BNW	BNW	–	–	–	–
E30	P_D14P_BNW	BNW	–	–	–	–
E31	VSS	VSS	–	–	–	–
E32	P_D1N_BNW(1)	BNW	–	–	–	–
E33	P_D1P_BNW(1)	BNW	–	–	–	–
E34	P_D0P_B1	B1	DQ0	DQ0	DQ0	DQ0
E35	P_D1P_B1	B1	DQ0	DQ0	DQ0	DQ0

Table 45: *FG1892 Pin Listing for SPD60*

Pin	Pin Name	Group	DDR123 Hard Controller (x8)	x8/x9 DQ–QS	x16/x18 DQ–QS	x32/x36 DQ–QS
E36	VDDO_B1	B1	–	–	–	–
E37	P_D6P_B1	B1	DQ1	DQ1	DQ0	DQ0
E38	P_D7P_B1	B1	DQ1	DQ1	DQ0	DQ0
E39	VDDO_B1	B1	–	–	–	–
E40	VSS	VSS	–	–	–	–
E41	VDDO_B1	B1	–	–	–	–
E42	VSS	VSS	–	–	–	–
E43	VSS	VSS	–	–	–	–
E44	N/C	–	–	–	–	–
F1	VSS	VSS	–	–	–	–
F2	VSS	VSS	–	–	–	–
F3	P_D12P_B6	B6	DQ2	DQ2	DQ1	DQ0
F4	P_D12N_B6	B6	DQ2	DQ2	DQ1	DQ0
F5	P_D13P_B6	B6	DQ2	DQ2	DQ1	DQ0
F6	P_D24P_B6	B6	DQ4	DQ4	DQ2	DQ1
F7	P_D7N_B6	B6	DQ1	DQ1	DQ0	DQ0
F8	P_D6N_B6	B6	DQ1	DQ1	DQ0	DQ0
F9	VSS	VSS	–	–	–	–
F10	P_D1N_B6	B6	DQ0	DQ0	DQ0	DQ0
F11	P_D0N_B6	B6	DQ0	DQ0	DQ0	DQ0
F12	P_D2P_BNE	BNE	–	–	–	–
F13	P_D2N_BNE	BNE	–	–	–	–
F14	P_D13P_BNE	BNE	–	–	–	–
F15	P_D13N_BNE	BNE	–	–	–	–
F16	P_D15P_BNE	BNE	–	–	–	–
F17	P_D15N_BNE	BNE	–	–	–	–
F18	P_D28P_BNE	BNE	–	–	–	–
F19	P_D28N_BNE	BNE	–	–	–	–
F20	P_D36P_BNE	BNE	–	–	–	–
F21	P_D37N_BNE	BNE	–	–	–	–
F22	P_D39P_BNE	BNE	–	–	–	–
F23	P_D39P_BNW	BNW	–	–	–	–
F24	P_D37N_BNW	BNW	–	–	–	–
F25	P_D36P_BNW	BNW	–	–	–	–
F26	P_D28N_BNW	BNW	–	–	–	–
F27	P_D28P_BNW	BNW	–	–	–	–
F28	P_D15N_BNW	BNW	–	–	–	–
F29	P_D15P_BNW	BNW	–	–	–	–
F30	P_D13N_BNW	BNW	–	–	–	–
F31	P_D13P_BNW	BNW	–	–	–	–
F32	P_D2N_BNW	BNW	–	–	–	–
F33	P_D2P_BNW	BNW	–	–	–	–
F34	P_D0N_B1	B1	DQ0	DQ0	DQ0	DQ0
F35	P_D1N_B1	B1	DQ0	DQ0	DQ0	DQ0

Table 45: *FG1892 Pin Listing for SPD60*

Pin	Pin Name	Group	DDR123 Hard Controller (x8)	x8/x9 DQ–QS	x16/x18 DQ–QS	x32/x36 DQ–QS
F36	VSS	VSS	–	–	–	–
F37	P_D6N_B1	B1	DQ1	DQ1	DQ0	DQ0
F38	P_D7N_B1	B1	DQ1	DQ1	DQ0	DQ0
F39	P_D24P_B1	B1	DQ4	DQ4	DQ2	DQ1
F40	P_D13P_B1	B1	DQ2	DQ2	DQ1	DQ0
F41	P_D12N_B1	B1	DQ2	DQ2	DQ1	DQ0
F42	P_D12P_B1	B1	DQ2	DQ2	DQ1	DQ0
F43	VSS	VSS	–	–	–	–
F44	VSS	VSS	–	–	–	–
G1	P_D15P_B6	B6	DQ2	DQ2	DQ1	DQ0
G2	P_D15N_B6	B6	DQ2	DQ2	DQ1	DQ0
G3	P_D14P_B6	B6	DQSP2	DQSP2	DQSP1	DQ0
G4	P_D14N_B6	B6	DQSN2	DQSN2	DQSN1	DQ0
G5	P_D13N_B6	B6	DQ2	DQ2	DQ1	DQ0
G6	P_D24N_B6	B6	DQ4	DQ4	DQ2	DQ1
G7	P_D8P_B6	B6	DQSP1	DQSP1	DQ0	DQSP0
G8	P_D9P_B6	B6	DQ1	DQ1	DQ0	DQ0
G9	P_RTTLO_B6	B6	–	–	–	–
G10	P_D2P_B6	B6	DQSP0	DQSP0	DQSP0	DQ0
G11	P_D3P_B6	B6	DQ0	DQ0	DQ0	DQ0
G12	P_D3P_BNE	BNE	–	–	–	–
G13	P_D3N_BNE	BNE	–	–	–	–
G14	P_D12P_BNE	BNE	–	–	–	–
G15	P_D12N_BNE	BNE	–	–	–	–
G16	P_D16P_BNE	BNE	–	–	–	–
G17	P_D16N_BNE	BNE	–	–	–	–
G18	P_D27P_BNE	BNE	–	–	–	–
G19	P_D27N_BNE	BNE	–	–	–	–
G20	P_D36N_BNE	BNE	–	–	–	–
G21	P_D35P_BNE	BNE	–	–	–	–
G22	P_D39N_BNE	BNE	–	–	–	–
G23	P_D39N_BNW	BNW	–	–	–	–
G24	P_D35P_BNW	BNW	–	–	–	–
G25	P_D36N_BNW	BNW	–	–	–	–
G26	P_D27N_BNW	BNW	–	–	–	–
G27	P_D27P_BNW	BNW	–	–	–	–
G28	P_D16N_BNW	BNW	–	–	–	–
G29	P_D16P_BNW	BNW	–	–	–	–
G30	P_D12N_BNW	BNW	–	–	–	–
G31	P_D12P_BNW	BNW	–	–	–	–
G32	P_D3N_BNW	BNW	–	–	–	–
G33	P_D3P_BNW	BNW	–	–	–	–
G34	P_D3P_B1	B1	DQ0	DQ0	DQ0	DQ0
G35	P_D2P_B1	B1	DQSP0	DQSP0	DQSP0	DQ0

Table 45: *FG1892 Pin Listing for SPD60*

Pin	Pin Name	Group	DDR123 Hard Controller (x8)	x8/x9 DQ–QS	x16/x18 DQ–QS	x32/x36 DQ–QS
G36	P_RTTLO_B1	B1	–	–	–	–
G37	P_D9P_B1	B1	DQ1	DQ1	DQ0	DQ0
G38	P_D8P_B1	B1	DQSP1	DQSP1	DQ0	DQSP0
G39	P_D24N_B1	B1	DQ4	DQ4	DQ2	DQ1
G40	P_D13N_B1	B1	DQ2	DQ2	DQ1	DQ0
G41	P_D14N_B1	B1	DQSN2	DQSN2	DQSN1	DQ0
G42	P_D14P_B1	B1	DQSP2	DQSP2	DQSP1	DQ0
G43	P_D15P_B1	B1	DQ2	DQ2	DQ1	DQ0
G44	P_D15N_B1	B1	DQ2	DQ2	DQ1	DQ0
H1	P_D17P_B6	B6	DM	DQ2	DQ1	DQ0
H2	P_D17N_B6	B6	RESERVED	DQ2	DQ1	DQ0
H3	P_D16P_B6	B6	DQ2	DQ2	DQ1	DQ0
H4	P_D16N_B6	B6	DQ2	DQ2	DQ1	DQ0
H5	P_D25P_B6	B6	DQ4	DQ4	DQ2	DQ1
H6	P_D26P_B6	B6	DQSP4	DQSP4	DQSP2	DQ1
H7	P_D8N_B6	B6	DQSN1	DQSN1	DQ0	DQSN0
H8	P_D9N_B6	B6	DQ1	DQ1	DQ0	DQ0
H9	P_RTTHI_B6	B6	–	–	–	–
H10	P_D2N_B6	B6	DQSN0	DQSN0	DQSN0	DQ0
H11	P_D3N_B6	B6	DQ0	DQ0	DQ0	DQ0
H12	P_D4P_BNE	BNE	–	–	–	–
H13	P_D4N_BNE	BNE	–	–	–	–
H14	VDDO_BNE	BNE	–	–	–	–
H15	P_D17P_BNE	BNE	–	–	–	–
H16	P_D17N_BNE	BNE	–	–	–	–
H17	VSS	VSS	–	–	–	–
H18	P_D26P_BNE	BNE	–	–	–	–
H19	P_D26N_BNE	BNE	–	–	–	–
H20	VDDO_BNE	BNE	–	–	–	–
H21	P_D35N_BNE	BNE	–	–	–	–
H22	VSS	VSS	–	–	–	–
H23	VSS	VSS	–	–	–	–
H24	P_D35N_BNW	BNW	–	–	–	–
H25	VDDO_BNW	BNW	–	–	–	–
H26	P_D26N_BNW	BNW	–	–	–	–
H27	P_D26P_BNW	BNW	–	–	–	–
H28	VSS	VSS	–	–	–	–
H29	P_D17N_BNW	BNW	–	–	–	–
H30	P_D17P_BNW	BNW	–	–	–	–
H31	VDDO_BNW	BNW	–	–	–	–
H32	P_D4N_BNW	BNW	–	–	–	–
H33	P_D4P_BNW	BNW	–	–	–	–
H34	P_D3N_B1	B1	DQ0	DQ0	DQ0	DQ0
H35	P_D2N_B1	B1	DQSN0	DQSN0	DQSN0	DQ0

Table 45: *FG1892 Pin Listing for SPD60*

Pin	Pin Name	Group	DDR123 Hard Controller (x8)	x8/x9 DQ–QS	x16/x18 DQ–QS	x32/x36 DQ–QS
H36	P_RTTHI_B1	B1	–	–	–	–
H37	P_D9N_B1	B1	DQ1	DQ1	DQ0	DQ0
H38	P_D8N_B1	B1	DQSN1	DQSN1	DQ0	DQSN0
H39	P_D26P_B1	B1	DQSP4	DQSP4	DQSP2	DQ1
H40	P_D25P_B1	B1	DQ4	DQ4	DQ2	DQ1
H41	P_D16N_B1	B1	DQ2	DQ2	DQ1	DQ0
H42	P_D16P_B1	B1	DQ2	DQ2	DQ1	DQ0
H43	P_D17P_B1	B1	DM	DQ2	DQ1	DQ0
H44	P_D17N_B1	B1	RESERVED	DQ2	DQ1	DQ0
J1	P_D18P_B6	B6	DQ3	DQ3	DQ1	DQ0
J2	P_D18N_B6	B6	DQ3	DQ3	DQ1	DQ0
J3	VDDO_B6	B6	–	–	–	–
J4	VSS	VSS	–	–	–	–
J5	P_D25N_B6	B6	DQ4	DQ4	DQ2	DQ1
J6	P_D26N_B6	B6	DQSN4	DQSN4	DQSN2	DQ1
J7	P_D10P_B6	B6	DQ1	DQ1	DQ0	DQ0
J8	P_D11P_B6	B6	DM	DQ1	DQ0	DQ0
J9	VDDO_B6	B6	–	–	–	–
J10	P_D5P_B6	B6	DM	DQ0	DQ0	DQ0
J11	P_D4P_B6	B6	DQ0	DQ0	DQ0	DQ0
J12	P_D5P_BNE	BNE	–	–	–	–
J13	P_D5N_BNE	BNE	–	–	–	–
J14	P_D11P_BNE	BNE	–	–	–	–
J15	P_D11N_BNE	BNE	–	–	–	–
J16	P_D18P_BNE	BNE	–	–	–	–
J17	P_D18N_BNE	BNE	–	–	–	–
J18	P_D25P_BNE	BNE	–	–	–	–
J19	P_D25N_BNE	BNE	–	–	–	–
J20	P_D34P_BNE	BNE	–	–	–	–
J21	P_D34N_BNE	BNE	–	–	–	–
J22	P_D40P_BNE	BNE	–	–	–	–
J23	P_D40P_BNW	BNW	–	–	–	–
J24	P_D34N_BNW	BNW	–	–	–	–
J25	P_D34P_BNW	BNW	–	–	–	–
J26	P_D25N_BNW	BNW	–	–	–	–
J27	P_D25P_BNW	BNW	–	–	–	–
J28	P_D18N_BNW	BNW	–	–	–	–
J29	P_D18P_BNW	BNW	–	–	–	–
J30	P_D11N_BNW	BNW	–	–	–	–
J31	P_D11P_BNW	BNW	–	–	–	–
J32	P_D5N_BNW	BNW	–	–	–	–
J33	P_D5P_BNW	BNW	–	–	–	–
J34	P_D4P_B1	B1	DQ0	DQ0	DQ0	DQ0
J35	P_D5P_B1	B1	DM	DQ0	DQ0	DQ0

Table 45: *FG1892 Pin Listing for SPD60*

Pin	Pin Name	Group	DDR123 Hard Controller (x8)	x8/x9 DQ–QS	x16/x18 DQ–QS	x32/x36 DQ–QS
J36	VDDO_B1	B1	–	–	–	–
J37	P_D11P_B1	B1	DM	DQ1	DQ0	DQ0
J38	P_D10P_B1	B1	DQ1	DQ1	DQ0	DQ0
J39	P_D26N_B1	B1	DQSN4	DQSN4	DQSN2	DQ1
J40	P_D25N_B1	B1	DQ4	DQ4	DQ2	DQ1
J41	VSS	VSS	–	–	–	–
J42	VDDO_B1	B1	–	–	–	–
J43	P_D18P_B1	B1	DQ3	DQ3	DQ1	DQ0
J44	P_D18N_B1	B1	DQ3	DQ3	DQ1	DQ0
K1	P_D20P_B6	B6	DQSP3	DQSP3	DQ1	DQ0
K2	P_D20N_B6	B6	DQSN3	DQSN3	DQ1	DQ0
K3	P_D19P_B6	B6	DQ3	DQ3	DQ1	DQ0
K4	P_D19N_B6	B6	DQ3	DQ3	DQ1	DQ0
K5	P_D28P_B6	B6	DQ4	DQ4	DQ2	DQ1
K6	P_D27P_B6	B6	DQ4	DQ4	DQ2	DQ1
K7	P_D10N_B6	B6	DQ1	DQ1	DQ0	DQ0
K8	P_D11N_B6	B6	RESERVED	DQ1	DQ0	DQ0
K9	VSS	VSS	–	–	–	–
K10	P_D5N_B6	B6	RESERVED	DQ0	DQ0	DQ0
K11	P_D4N_B6	B6	DQ0	DQ0	DQ0	DQ0
K12	P_D6P_BNE	BNE	–	–	–	–
K13	P_D6N_BNE	BNE	–	–	–	–
K14	P_D10P_BNE	BNE	–	–	–	–
K15	P_D10N_BNE	BNE	–	–	–	–
K16	P_D19P_BNE	BNE	–	–	–	–
K17	P_D19N_BNE	BNE	–	–	–	–
K18	P_D24P_BNE	BNE	–	–	–	–
K19	P_D24N_BNE	BNE	–	–	–	–
K20	P_D33P_BNE	BNE	–	–	–	–
K21	P_D33N_BNE	BNE	–	–	–	–
K22	P_D40N_BNE	BNE	–	–	–	–
K23	P_D40N_BNW	BNW	–	–	–	–
K24	P_D33N_BNW	BNW	–	–	–	–
K25	P_D33P_BNW	BNW	–	–	–	–
K26	P_D24N_BNW	BNW	–	–	–	–
K27	P_D24P_BNW	BNW	–	–	–	–
K28	P_D19N_BNW	BNW	–	–	–	–
K29	P_D19P_BNW	BNW	–	–	–	–
K30	P_D10N_BNW	BNW	–	–	–	–
K31	P_D10P_BNW	BNW	–	–	–	–
K32	P_D6N_BNW	BNW	–	–	–	–
K33	P_D6P_BNW	BNW	–	–	–	–
K34	P_D4N_B1	B1	DQ0	DQ0	DQ0	DQ0
K35	P_D5N_B1	B1	RESERVED	DQ0	DQ0	DQ0

Table 45: *FG1892 Pin Listing for SPD60*

Pin	Pin Name	Group	DDR123 Hard Controller (x8)	x8/x9 DQ–QS	x16/x18 DQ–QS	x32/x36 DQ–QS
K36	VSS	VSS	–	–	–	–
K37	P_D11N_B1	B1	RESERVED	DQ1	DQ0	DQ0
K38	P_D10N_B1	B1	DQ1	DQ1	DQ0	DQ0
K39	P_D27P_B1	B1	DQ4	DQ4	DQ2	DQ1
K40	P_D28P_B1	B1	DQ4	DQ4	DQ2	DQ1
K41	P_D19N_B1	B1	DQ3	DQ3	DQ1	DQ0
K42	P_D19P_B1	B1	DQ3	DQ3	DQ1	DQ0
K43	P_D20P_B1	B1	DQSP3	DQSP3	DQ1	DQ0
K44	P_D20N_B1	B1	DQSN3	DQSN3	DQ1	DQ0
L1	P_D22P_B6	B6	DQ3	DQ3	DQ1	DQ0
L2	P_D22N_B6	B6	DQ3	DQ3	DQ1	DQ0
L3	P_D21P_B6	B6	DQ3	DQ3	DQ1	DQ0
L4	P_D21N_B6	B6	DQ3	DQ3	DQ1	DQ0
L5	P_D28N_B6	B6	DQ4	DQ4	DQ2	DQ1
L6	P_D27N_B6	B6	DQ4	DQ4	DQ2	DQ1
L7	P_D37P_B6	B6	DDR_A[2]	DQ6	DQ3	DQ1
L8	P_D36P_B6	B6	DDR_A[0]	DQ6	DQ3	DQ1
L9	P_DRVLO_B6	B6	–	–	–	–
L10	P_D31P_B6	B6	CKE[0]	DQ5	DQ2	DQ1
L11	P_D30P_B6	B6	CS_N[0]	DQ5	DQ2	DQ1
L12	P_D2P_CB3	CB3	–	–	–	–
L13	P_D2N_CB3	CB3	–	–	–	–
L14	VSS	VSS	–	–	–	–
L15	P_D9P_BNE	BNE	–	–	–	–
L16	P_D9N_BNE	BNE	–	–	–	–
L17	VDDO_BNE	BNE	–	–	–	–
L18	P_D23P_BNE	BNE	–	–	–	–
L19	P_D23N_BNE	BNE	–	–	–	–
L20	VSS	VSS	–	–	–	–
L21	P_D32P_BNE	BNE	–	–	–	–
L22	VDDO_BNE	BNE	–	–	–	–
L23	VDDO_BNW	BNW	–	–	–	–
L24	P_D32P_BNW	BNW	–	–	–	–
L25	VSS	VSS	–	–	–	–
L26	P_D23N_BNW	BNW	–	–	–	–
L27	P_D23P_BNW	BNW	–	–	–	–
L28	VDDO_BNW	BNW	–	–	–	–
L29	P_D9N_BNW	BNW	–	–	–	–
L30	P_D9P_BNW	BNW	–	–	–	–
L31	VSS	VSS	–	–	–	–
L32	P_D2N_CB4	CB4	–	–	–	–
L33	P_D2P_CB4	CB4	–	–	–	–
L34	P_D30P_B1	B1	CS_N[0]	DQ5	DQ2	DQ1
L35	P_D31P_B1	B1	CKE[0]	DQ5	DQ2	DQ1

Table 45: *FG1892 Pin Listing for SPD60*

Pin	Pin Name	Group	DDR123 Hard Controller (x8)	x8/x9 DQ–QS	x16/x18 DQ–QS	x32/x36 DQ–QS
L36	P_DRVLO_B1	B1	–	–	–	–
L37	P_D36P_B1	B1	DDR_A[0]	DQ6	DQ3	DQ1
L38	P_D37P_B1	B1	DDR_A[2]	DQ6	DQ3	DQ1
L39	P_D27N_B1	B1	DQ4	DQ4	DQ2	DQ1
L40	P_D28N_B1	B1	DQ4	DQ4	DQ2	DQ1
L41	P_D21N_B1	B1	DQ3	DQ3	DQ1	DQ0
L42	P_D21P_B1	B1	DQ3	DQ3	DQ1	DQ0
L43	P_D22P_B1	B1	DQ3	DQ3	DQ1	DQ0
L44	P_D22N_B1	B1	DQ3	DQ3	DQ1	DQ0
M1	P_D23P_B6	B6	DM	DQ3	DQ1	DQ0
M2	P_D23N_B6	B6	RESERVED	DQ3	DQ1	DQ0
M3	P_D42P_B6	B6	DDR_A[10]	DQ7	DQ3	DQ1
M4	P_D42N_B6	B6	DDR_A[11]	DQ7	DQ3	DQ1
M5	P_D29P_B6	B6	DM	DQ4	DQ2	DQ1
M6	VDDO_B6	B6	–	–	–	–
M7	P_D37N_B6	B6	DDR_A[3]	DQ6	DQ3	DQ1
M8	P_D36N_B6	B6	DDR_A[1]	DQ6	DQ3	DQ1
M9	P_DRVHI_B6	B6	–	–	–	–
M10	P_D31N_B6	B6	CKE[1]	DQ5	DQ2	DQ1
M11	P_D30N_B6	B6	CS_N[1]	DQ5	DQ2	DQ1
M12	VDDO_CB3	CB3	–	–	–	–
M13	P_D1P_CB3	CB3	–	–	–	–
M14	P_D1N_CB3	CB3	–	–	–	–
M15	P_D8P_BNE	BNE	–	–	–	–
M16	P_D8N_BNE	BNE	–	–	–	–
M17	P_D22P_BNE	BNE	–	–	–	–
M18	P_D22N_BNE	BNE	–	–	–	–
M19	P_D31P_BNE	BNE	–	–	–	–
M20	P_D31N_BNE	BNE	–	–	–	–
M21	P_D32N_BNE	BNE	–	–	–	–
M22	P_D41P_BNE	BNE	–	–	–	–
M23	P_D41P_BNW	BNW	–	–	–	–
M24	P_D32N_BNW	BNW	–	–	–	–
M25	P_D31N_BNW	BNW	–	–	–	–
M26	P_D31P_BNW	BNW	–	–	–	–
M27	P_D22N_BNW	BNW	–	–	–	–
M28	P_D22P_BNW	BNW	–	–	–	–
M29	P_D8N_BNW	BNW	–	–	–	–
M30	P_D8P_BNW	BNW	–	–	–	–
M31	P_D1N_CB4	CB4	–	–	–	–
M32	P_D1P_CB4	CB4	–	–	–	–
M33	VDDO_CB4	CB4	–	–	–	–
M34	P_D30N_B1	B1	CS_N[1]	DQ5	DQ2	DQ1
M35	P_D31N_B1	B1	CKE[1]	DQ5	DQ2	DQ1

Table 45: *FG1892 Pin Listing for SPD60*

Pin	Pin Name	Group	DDR123 Hard Controller (x8)	x8/x9 DQ–QS	x16/x18 DQ–QS	x32/x36 DQ–QS
M36	P_DRVHI_B1	B1	–	–	–	–
M37	P_D36N_B1	B1	DDR_A[1]	DQ6	DQ3	DQ1
M38	P_D37N_B1	B1	DDR_A[3]	DQ6	DQ3	DQ1
M39	VDDO_B1	B1	–	–	–	–
M40	P_D29P_B1	B1	DM	DQ4	DQ2	DQ1
M41	P_D42N_B1	B1	DDR_A[11]	DQ7	DQ3	DQ1
M42	P_D42P_B1	B1	DDR_A[10]	DQ7	DQ3	DQ1
M43	P_D23P_B1	B1	DM	DQ3	DQ1	DQ0
M44	P_D23N_B1	B1	RESERVED	DQ3	DQ1	DQ0
N1	P_D43P_B6	B6	DDR_A[12]	DQ7	DQ3	DQ1
N2	P_D43N_B6	B6	DDR_A[13]	DQ7	DQ3	DQ1
N3	VSS	VSS	–	–	–	–
N4	VDDO_B6	B6	–	–	–	–
N5	P_D29N_B6	B6	RESERVED	DQ4	DQ2	DQ1
N6	VSS	VSS	–	–	–	–
N7	P_D38P_B6	B6	DDR_CLKP[1]	DQSP6	DQSP3	DQ1
N8	P_D39P_B6	B6	DDR_A[4]	DQ6	DQ3	DQ1
N9	VSS	VSS	–	–	–	–
N10	P_D32P_B6	B6	DDR_CLKP[0]	DQSP5	DQ2	DQSP1
N11	P_D33P_B6	B6	ODT[0]	DQ5	DQ2	DQ1
N12	P_D0P_CB3	CB3	–	–	–	–
N13	P_D0N_CB3	CB3	–	–	–	–
N14	P_D7P_BNE	BNE	–	–	–	–
N15	P_D7N_BNE	BNE	–	–	–	–
N16	P_D20P_BNE	BNE	–	–	–	–
N17	P_D20N_BNE	BNE	–	–	–	–
N18	P_D21P_BNE	BNE	–	–	–	–
N19	P_D21N_BNE	BNE	–	–	–	–
N20	P_D30P_BNE	BNE	–	–	–	–
N21	P_D30N_BNE	BNE	–	–	–	–
N22	P_D41N_BNE	BNE	–	–	–	–
N23	P_D41N_BNW	BNW	–	–	–	–
N24	P_D30N_BNW	BNW	–	–	–	–
N25	P_D30P_BNW	BNW	–	–	–	–
N26	P_D21N_BNW	BNW	–	–	–	–
N27	P_D21P_BNW	BNW	–	–	–	–
N28	P_D20N_BNW	BNW	–	–	–	–
N29	P_D20P_BNW	BNW	–	–	–	–
N30	P_D7N_BNW	BNW	–	–	–	–
N31	P_D7P_BNW	BNW	–	–	–	–
N32	P_D0N_CB4	CB4	–	–	–	–
N33	P_D0P_CB4	CB4	–	–	–	–
N34	P_D33P_B1	B1	ODT[0]	DQ5	DQ2	DQ1
N35	P_D32P_B1	B1	DDR_CLKP[0]	DQSP5	DQ2	DQSP1

Table 45: *FG1892 Pin Listing for SPD60*

Pin	Pin Name	Group	DDR123 Hard Controller (x8)	x8/x9 DQ–QS	x16/x18 DQ–QS	x32/x36 DQ–QS
N36	VSS	VSS	–	–	–	–
N37	P_D39P_B1	B1	DDR_A[4]	DQ6	DQ3	DQ1
N38	P_D38P_B1	B1	DDR_CLKP[1]	DQSP6	DQSP3	DQ1
N39	VSS	VSS	–	–	–	–
N40	P_D29N_B1	B1	RESERVED	DQ4	DQ2	DQ1
N41	VDDO_B1	B1	–	–	–	–
N42	VSS	VSS	–	–	–	–
N43	P_D43P_B1	B1	DDR_A[12]	DQ7	DQ3	DQ1
N44	P_D43N_B1	B1	DDR_A[13]	DQ7	DQ3	DQ1
P1	P_D45P_B6	B6	DDR_BA[0]	DQ7	DQ3	DQ1
P2	P_D45N_B6	B6	DDR_BA[1]	DQ7	DQ3	DQ1
P3	P_D44P_B6	B6	DDR_CLKP[2]	DQSP7	DQ3	DQ1
P4	P_D44N_B6	B6	DDR_CLKN[2]	DQSN7	DQ3	DQ1
P5	VDDO_B5_UP	B5	–	–	–	–
P6	P_D0P_B5	B5	DQ5	DQ8	DQ4	DQ2
P7	P_D38N_B6	B6	DDR_CLKN[1]	DQSN6	DQSN3	DQ1
P8	P_D39N_B6	B6	DDR_A[5]	DQ6	DQ3	DQ1
P9	VDDO_B6	B6	–	–	–	–
P10	P_D32N_B6	B6	DDR_CLKN[0]	DQSN5	DQ2	DQSN1
P11	P_D33N_B6	B6	ODT[1]	DQ5	DQ2	DQ1
P12	P_RTTLO_CB3	CB3	–	–	–	–
P13	VDDO_CB3	CB3	–	–	–	–
P14	VREF_CB3	CB3	–	–	–	–
P15	N/C	–	–	–	–	–
P16	N/C	–	–	–	–	–
P17	N/C	–	–	–	–	–
P18	N/C	–	–	–	–	–
P19	VDDA_5GB	5GB	–	–	–	–
P20	VDDA_5GB	5GB	–	–	–	–
P21	VDDA_5GB	5GB	–	–	–	–
P22	VDDA_5GB	5GB	–	–	–	–
P23	VDDA_5GA	5GA	–	–	–	–
P24	VDDA_5GA	5GA	–	–	–	–
P25	VDDA_5GA	5GA	–	–	–	–
P26	VDDA_5GA	5GA	–	–	–	–
P27	N/C	–	–	–	–	–
P28	N/C	–	–	–	–	–
P29	N/C	–	–	–	–	–
P30	N/C	–	–	–	–	–
P31	VREF_CB4	CB4	–	–	–	–
P32	VDDO_CB4	CB4	–	–	–	–
P33	P_RTTLO_CB4	CB4	–	–	–	–
P34	P_D33N_B1	B1	ODT[1]	DQ5	DQ2	DQ1
P35	P_D32N_B1	B1	DDR_CLKN[0]	DQSN5	DQ2	DQSN1

Table 45: *FG1892 Pin Listing for SPD60*

Pin	Pin Name	Group	DDR123 Hard Controller (x8)	x8/x9 DQ–QS	x16/x18 DQ–QS	x32/x36 DQ–QS
P36	VDDO_B1	B1	–	–	–	–
P37	P_D39N_B1	B1	DDR_A[5]	DQ6	DQ3	DQ1
P38	P_D38N_B1	B1	DDR_CLKN[1]	DQSN6	DQSN3	DQ1
P39	P_D0P_B2	B2	DQ5	DQ8	DQ4	DQ2
P40	VDDO_B2_UP	B2	–	–	–	–
P41	P_D44N_B1	B1	DDR_CLKN[2]	DQSN7	DQ3	DQ1
P42	P_D44P_B1	B1	DDR_CLKP[2]	DQSP7	DQ3	DQ1
P43	P_D45P_B1	B1	DDR_BA[0]	DQ7	DQ3	DQ1
P44	P_D45N_B1	B1	DDR_BA[1]	DQ7	DQ3	DQ1
R1	P_D47P_B6	B6	DDR_CAS_N	DQ7	DQ3	DQ1
R2	P_D47N_B6	B6	DDDR_RAS_N	DQ7	DQ3	DQ1
R3	P_D46P_B6	B6	DDR_BA[2]	DQ7	DQ3	DQ1
R4	P_D46N_B6	B6	DDR_WE_N	DQ7	DQ3	DQ1
R5	P_D1P_B5	B5	DQ5	DQ8	DQ4	DQ2
R6	P_D0N_B5	B5	DQ5	DQ8	DQ4	DQ2
R7	P_D41P_B6	B6	DDR_A[8]	DQ6	DQ3	DQ1
R8	P_D40P_B6	B6	DDR_A[6]	DQ6	DQ3	DQ1
R9	N/C	–	–	–	–	–
R10	P_D35P_B6	B6	DDR_A[14]	DQ5	DQ2	DQ1
R11	P_D34P_B6	B6	RESET	DQ5	DQ2	DQ1
R12	P_RTTHI_CB3	CB3	–	–	–	–
R13	VREF_CB3	CB3	–	–	–	–
R14	PLL_VSSA1_NE	PLL_NE	–	–	–	–
R15	PLL_VDDA0_NE	PLL_NE	–	–	–	–
R16	PLL_VSSA1_NE	PLL_NE	–	–	–	–
R17	PLL_VDDA1_NE	PLL_NE	–	–	–	–
R18	VDD	VDD	–	–	–	–
R19	VSS	VSS	–	–	–	–
R20	VDDL	VDD	–	–	–	–
R21	VSS	VSS	–	–	–	–
R22	VDD	VDD	–	–	–	–
R23	VSS	VSS	–	–	–	–
R24	VDDL	VDD	–	–	–	–
R25	VSS	VSS	–	–	–	–
R26	VDD	VDD	–	–	–	–
R27	VSS	VSS	–	–	–	–
R28	PLL_VDDA1_NW	PLL_NW	–	–	–	–
R29	PLL_VSSA1_NW	PLL_NW	–	–	–	–
R30	PLL_VDDA0_NW	PLL_NW	–	–	–	–
R31	PLL_VSSA1_NW	PLL_NW	–	–	–	–
R32	VREF_CB4	CB4	–	–	–	–
R33	P_RTTHI_CB4	CB4	–	–	–	–
R34	P_D34P_B1	B1	RESET	DQ5	DQ2	DQ1
R35	P_D35P_B1	B1	DDR_A[14]	DQ5	DQ2	DQ1

Table 45: *FG1892 Pin Listing for SPD60*

Pin	Pin Name	Group	DDR123 Hard Controller (x8)	x8/x9 DQ–QS	x16/x18 DQ–QS	x32/x36 DQ–QS
R36	N/C	–	–	–	–	–
R37	P_D40P_B1	B1	DDR_A[6]	DQ6	DQ3	DQ1
R38	P_D41P_B1	B1	DDR_A[8]	DQ6	DQ3	DQ1
R39	P_D0N_B2	B2	DQ5	DQ8	DQ4	DQ2
R40	P_D1P_B2	B2	DQ5	DQ8	DQ4	DQ2
R41	P_D46N_B1	B1	DDR_WE_N	DQ7	DQ3	DQ1
R42	P_D46P_B1	B1	DDR_BA[2]	DQ7	DQ3	DQ1
R43	P_D47P_B1	B1	DDR_CAS_N	DQ7	DQ3	DQ1
R44	P_D47N_B1	B1	DDDR_RAS_N	DQ7	DQ3	DQ1
T1	P_D19P_B5	B5	DQ8	DQ11	DQ5	DQ2
T2	P_D19N_B5	B5	DQ8	DQ11	DQ5	DQ2
T3	P_D18P_B5	B5	DQ8	DQ11	DQ5	DQ2
T4	P_D18N_B5	B5	DQ8	DQ11	DQ5	DQ2
T5	P_D1N_B5	B5	DQ5	DQ8	DQ4	DQ2
T6	P_D3P_B5	B5	DQ5	DQ8	DQ4	DQ2
T7	P_D41N_B6	B6	DDR_A[9]	DQ6	DQ3	DQ1
T8	P_D40N_B6	B6	DDR_A[7]	DQ6	DQ3	DQ1
T9	N/C	–	–	–	–	–
T10	P_D35N_B6	B6	DDR_A[15]	DQ5	DQ2	DQ1
T11	P_D34N_B6	B6	–	DQ5	DQ2	DQ1
T12	N/C	–	–	–	–	–
T13	VREF_BNE	BNE	–	–	–	–
T14	PLL_VDDA1_NE	PLL_NE	–	–	–	–
T15	PLL_VSSA0_NE	PLL_NE	–	–	–	–
T16	VSS	VSS	–	–	–	–
T17	VDDL	VDD	–	–	–	–
T18	VSS	VSS	–	–	–	–
T19	VDD	VDD	–	–	–	–
T20	VSS	VSS	–	–	–	–
T21	VDDL	VDD	–	–	–	–
T22	VSS	VSS	–	–	–	–
T23	VDD	VDD	–	–	–	–
T24	VSS	VSS	–	–	–	–
T25	VDDL	VDD	–	–	–	–
T26	VSS	VSS	–	–	–	–
T27	VDD	VDD	–	–	–	–
T28	VSS	VSS	–	–	–	–
T29	VDDL	VDD	–	–	–	–
T30	PLL_VSSA0_NW	PLL_NW	–	–	–	–
T31	PLL_VDDA1_NW	PLL_NW	–	–	–	–
T32	VREF_BNW	BNW	–	–	–	–
T33	N/C	–	–	–	–	–
T34	P_D34N_B1	B1	–	DQ5	DQ2	DQ1
T35	P_D35N_B1	B1	DDR_A[15]	DQ5	DQ2	DQ1

Table 45: *FG1892 Pin Listing for SPD60*

Pin	Pin Name	Group	DDR123 Hard Controller (x8)	x8/x9 DQ–QS	x16/x18 DQ–QS	x32/x36 DQ–QS
T36	N/C	–	–	–	–	–
T37	P_D40N_B1	B1	DDR_A[7]	DQ6	DQ3	DQ1
T38	P_D41N_B1	B1	DDR_A[9]	DQ6	DQ3	DQ1
T39	P_D3P_B2	B2	DQ5	DQ8	DQ4	DQ2
T40	P_D1N_B2	B2	DQ5	DQ8	DQ4	DQ2
T41	P_D18N_B2	B2	DQ8	DQ11	DQ5	DQ2
T42	P_D18P_B2	B2	DQ8	DQ11	DQ5	DQ2
T43	P_D19P_B2	B2	DQ8	DQ11	DQ5	DQ2
T44	P_D19N_B2	B2	DQ8	DQ11	DQ5	DQ2
U1	P_D20P_B5	B5	DQSP8	DQSP11	DQ5	DQ2
U2	P_D20N_B5	B5	DQSN8	DQSN11	DQ5	DQ2
U3	VDDO_B5_UP	B5	–	–	–	–
U4	VSS	VSS	–	–	–	–
U5	P_D2P_B5	B5	DQSP5	DQSP8	DQSP4	DQ2
U6	P_D3N_B5	B5	DQ5	DQ8	DQ4	DQ2
U7	P_D13P_B5	B5	DQ7	DQ10	DQ5	DQ2
U8	P_D12P_B5	B5	DQ7	DQ10	DQ5	DQ2
U9	VDDO_B5_UP	B5	–	–	–	–
U10	P_D7P_B5	B5	DQ6	DQ9	DQ4	DQ2
U11	P_D6P_B5	B5	DQ6	DQ9	DQ4	DQ2
U12	VSS	VSS	–	–	–	–
U13	VREF_BNE	BNE	–	–	–	–
U14	PLL_VDDA0_NE	PLL_NE	–	–	–	–
U15	VSS	VSS	–	–	–	–
U16	VDDL	VDD	–	–	–	–
U17	VSS	VSS	–	–	–	–
U18	VDD	VDD	–	–	–	–
U19	VSS	VSS	–	–	–	–
U20	VDDL	VDD	–	–	–	–
U21	VSS	VSS	–	–	–	–
U22	VDD	VDD	–	–	–	–
U23	VSS	VSS	–	–	–	–
U24	VDDL	VDD	–	–	–	–
U25	VSS	VSS	–	–	–	–
U26	VDD	VDD	–	–	–	–
U27	VSS	VSS	–	–	–	–
U28	VDDL	VDD	–	–	–	–
U29	VSS	VSS	–	–	–	–
U30	VDD	VDD	–	–	–	–
U31	PLL_VDDA0_NW	PLL_NW	–	–	–	–
U32	VREF_BNW	BNW	–	–	–	–
U33	VSS	VSS	–	–	–	–
U34	P_D6P_B2	B2	DQ6	DQ9	DQ4	DQ2
U35	P_D7P_B2	B2	DQ6	DQ9	DQ4	DQ2

Table 45: *FG1892 Pin Listing for SPD60*

Pin	Pin Name	Group	DDR123 Hard Controller (x8)	x8/x9 DQ–QS	x16/x18 DQ–QS	x32/x36 DQ–QS
U36	VDDO_B2_UP	B2	–	–	–	–
U37	P_D12P_B2	B2	DQ7	DQ10	DQ5	DQ2
U38	P_D13P_B2	B2	DQ7	DQ10	DQ5	DQ2
U39	P_D3N_B2	B2	DQ5	DQ8	DQ4	DQ2
U40	P_D2P_B2	B2	DQSP5	DQSP8	DQSP4	DQ2
U41	VSS	VSS	–	–	–	–
U42	VDDO_B2_UP	B2	–	–	–	–
U43	P_D20P_B2	B2	DQSP8	DQSP11	DQ5	DQ2
U44	P_D20N_B2	B2	DQSN8	DQSN11	DQ5	DQ2
V1	P_D22P_B5	B5	DQ8	DQ11	DQ5	DQ2
V2	P_D22N_B5	B5	DQ8	DQ11	DQ5	DQ2
V3	P_D21P_B5	B5	DQ8	DQ11	DQ5	DQ2
V4	P_D21N_B5	B5	DQ8	DQ11	DQ5	DQ2
V5	P_D2N_B5	B5	DQSN5	DQSN8	DQSN4	DQ2
V6	VDDO_B5_UP	B5	–	–	–	–
V7	P_D13N_B5	B5	DQ7	DQ10	DQ5	DQ2
V8	P_D12N_B5	B5	DQ7	DQ10	DQ5	DQ2
V9	VSS	VSS	–	–	–	–
V10	P_D7N_B5	B5	DQ6	DQ9	DQ4	DQ2
V11	P_D6N_B5	B5	DQ6	DQ9	DQ4	DQ2
V12	VDDO_B6	B6	–	–	–	–
V13	VDDL	VDD	–	–	–	–
V14	PLL_VSSA0_NE	PLL_NE	–	–	–	–
V15	VDD	VDD	–	–	–	–
V16	VSS	VSS	–	–	–	–
V17	VDDL	VDD	–	–	–	–
V18	VSS	VSS	–	–	–	–
V19	VDD	VDD	–	–	–	–
V20	VSS	VSS	–	–	–	–
V21	VDDL	VDD	–	–	–	–
V22	VSS	VSS	–	–	–	–
V23	VDD	VDD	–	–	–	–
V24	VSS	VSS	–	–	–	–
V25	VDDL	VDD	–	–	–	–
V26	VSS	VSS	–	–	–	–
V27	VDD	VDD	–	–	–	–
V28	VSS	VSS	–	–	–	–
V29	VDDL	VDD	–	–	–	–
V30	VSS	VSS	–	–	–	–
V31	PLL_VSSA0_NW	PLL_NW	–	–	–	–
V32	VSS	VSS	–	–	–	–
V33	VDDO_B1	B1	–	–	–	–
V34	P_D6N_B2	B2	DQ6	DQ9	DQ4	DQ2
V35	P_D7N_B2	B2	DQ6	DQ9	DQ4	DQ2

Table 45: *FG1892 Pin Listing for SPD60*

Pin	Pin Name	Group	DDR123 Hard Controller (x8)	x8/x9 DQ–QS	x16/x18 DQ–QS	x32/x36 DQ–QS
V36	VSS	VSS	–	–	–	–
V37	P_D12N_B2	B2	DQ7	DQ10	DQ5	DQ2
V38	P_D13N_B2	B2	DQ7	DQ10	DQ5	DQ2
V39	VDDO_B2_UP	B2	–	–	–	–
V40	P_D2N_B2	B2	DQSN5	DQSN8	DQSN4	DQ2
V41	P_D21N_B2	B2	DQ8	DQ11	DQ5	DQ2
V42	P_D21P_B2	B2	DQ8	DQ11	DQ5	DQ2
V43	P_D22P_B2	B2	DQ8	DQ11	DQ5	DQ2
V44	P_D22N_B2	B2	DQ8	DQ11	DQ5	DQ2
W1	P_D23P_B5	B5	DM	DQ11	DQ5	DQ2
W2	P_D23N_B5	B5	RESERVED	DQ11	DQ5	DQ2
W3	P_D24N_B5	B5	RESERVED	DQ11	DQ5	DQ2
W4	P_D24P_B5	B5	DM	DQ11	DQ5	DQ2
W5	P_D5P_B5	B5	DM	DQ8	DQ4	DQ2
W6	P_D4P_B5	B5	DQ5	DQ8	DQ4	DQ2
W7	P_D15P_B5	B5	DQ7	DQ10	DQ5	DQ2
W8	P_D14P_B5	B5	DQSP7	DQSP10	DQSP5	DQ2
W9	N/C	–	–	–	–	–
W10	P_D8P_B5	B5	DQSP6	DQSP9	DQ4	DQSP2
W11	P_D9P_B5	B5	DQ6	DQ9	DQ4	DQ2
W12	VDDO_B5_UP	B5	–	–	–	–
W13	VSS	VSS	–	–	–	–
W14	VDD	VDD	–	–	–	–
W15	VSS	VSS	–	–	–	–
W16	VDDL	VDD	–	–	–	–
W17	VSS	VSS	–	–	–	–
W18	VDD	VDD	–	–	–	–
W19	VSS	VSS	–	–	–	–
W20	VDDL	VDD	–	–	–	–
W21	VSS	VSS	–	–	–	–
W22	VDD	VDD	–	–	–	–
W23	VSS	VSS	–	–	–	–
W24	VDDL	VDD	–	–	–	–
W25	VSS	VSS	–	–	–	–
W26	VDD	VDD	–	–	–	–
W27	VSS	VSS	–	–	–	–
W28	VDDL	VDD	–	–	–	–
W29	VSS	VSS	–	–	–	–
W30	VDD	VDD	–	–	–	–
W31	VSS	VSS	–	–	–	–
W32	VDDL	VDD	–	–	–	–
W33	VDDO_B2_UP	B2	–	–	–	–
W34	P_D9P_B2	B2	DQ6	DQ9	DQ4	DQ2
W35	P_D8P_B2	B2	DQSP6	DQSP9	DQ4	DQSP2

Table 45: *FG1892 Pin Listing for SPD60*

Pin	Pin Name	Group	DDR123 Hard Controller (x8)	x8/x9 DQ–QS	x16/x18 DQ–QS	x32/x36 DQ–QS
W36	N/C	–	–	–	–	–
W37	P_D14P_B2	B2	DQSP7	DQSP10	DQSP5	DQ2
W38	P_D15P_B2	B2	DQ7	DQ10	DQ5	DQ2
W39	P_D4P_B2	B2	DQ5	DQ8	DQ4	DQ2
W40	P_D5P_B2	B2	DM	DQ8	DQ4	DQ2
W41	P_D24P_B2	B2	DM	DQ11	DQ5	DQ2
W42	P_D24N_B2	B2	RESERVED	DQ11	DQ5	DQ2
W43	P_D23P_B2	B2	DM	DQ11	DQ5	DQ2
W44	P_D23N_B2	B2	RESERVED	DQ11	DQ5	DQ2
Y1	P_D25N_B5	B5	DQ8	DQ11	DQ5	DQ2
Y2	P_D25P_B5	B5	DQ8	DQ11	DQ5	DQ2
Y3	P_D26N_B5	B5	DQ8	DQ11	DQ5	DQ2
Y4	P_D26P_B5	B5	DQ8	DQ11	DQ5	DQ2
Y5	P_D5N_B5	B5	RESERVED	DQ8	DQ4	DQ2
Y6	P_D4N_B5	B5	DQ5	DQ8	DQ4	DQ2
Y7	P_D15N_B5	B5	DQ7	DQ10	DQ5	DQ2
Y8	P_D14N_B5	B5	DQSN7	DQSN10	DQSN5	DQ2
Y9	N/C	–	–	–	–	–
Y10	P_D8N_B5	B5	DQSN6	DQSN9	DQ4	DQSN2
Y11	P_D9N_B5	B5	DQ6	DQ9	DQ4	DQ2
Y12	P_DRVLO_B5	B5	–	–	–	–
Y13	VREF_B6	B6	–	–	–	–
Y14	VSS	VSS	–	–	–	–
Y15	VDD	VDD	–	–	–	–
Y16	VSS	VSS	–	–	–	–
Y17	VDDL	VDD	–	–	–	–
Y18	VSS	VSS	–	–	–	–
Y19	VDD	VDD	–	–	–	–
Y20	VSS	VSS	–	–	–	–
Y21	VDDL	VDD	–	–	–	–
Y22	VSS	VSS	–	–	–	–
Y23	VDD	VDD	–	–	–	–
Y24	VSS	VSS	–	–	–	–
Y25	VDDL	VDD	–	–	–	–
Y26	VSS	VSS	–	–	–	–
Y27	VDD	VDD	–	–	–	–
Y28	VSS	VSS	–	–	–	–
Y29	VDDL	VDD	–	–	–	–
Y30	VSS	VSS	–	–	–	–
Y31	VDD	VDD	–	–	–	–
Y32	VREF_B1	B1	–	–	–	–
Y33	P_DRVLO_B2	B2	–	–	–	–
Y34	P_D9N_B2	B2	DQ6	DQ9	DQ4	DQ2
Y35	P_D8N_B2	B2	DQSN6	DQSN9	DQ4	DQSN2

Table 45: *FG1892 Pin Listing for SPD60*

Pin	Pin Name	Group	DDR123 Hard Controller (x8)	x8/x9 DQ–QS	x16/x18 DQ–QS	x32/x36 DQ–QS
Y36	N/C	–	–	–	–	–
Y37	P_D14N_B2	B2	DQSN7	DQSN10	DQSN5	DQ2
Y38	P_D15N_B2	B2	DQ7	DQ10	DQ5	DQ2
Y39	P_D4N_B2	B2	DQ5	DQ8	DQ4	DQ2
Y40	P_D5N_B2	B2	RESERVED	DQ8	DQ4	DQ2
Y41	P_D26P_B2	B2	DQ8	DQ11	DQ5	DQ2
Y42	P_D26N_B2	B2	DQ8	DQ11	DQ5	DQ2
Y43	P_D25N_B2	B2	DQ8	DQ11	DQ5	DQ2
Y44	P_D25P_B2	B2	DQ8	DQ11	DQ5	DQ2

Note:

1. Reset capable pin. See **"Reset Input Block,"** on page 43 for details.

Package Mechanicals

1892-Pin Fine Ball Grid Array (FG1892)

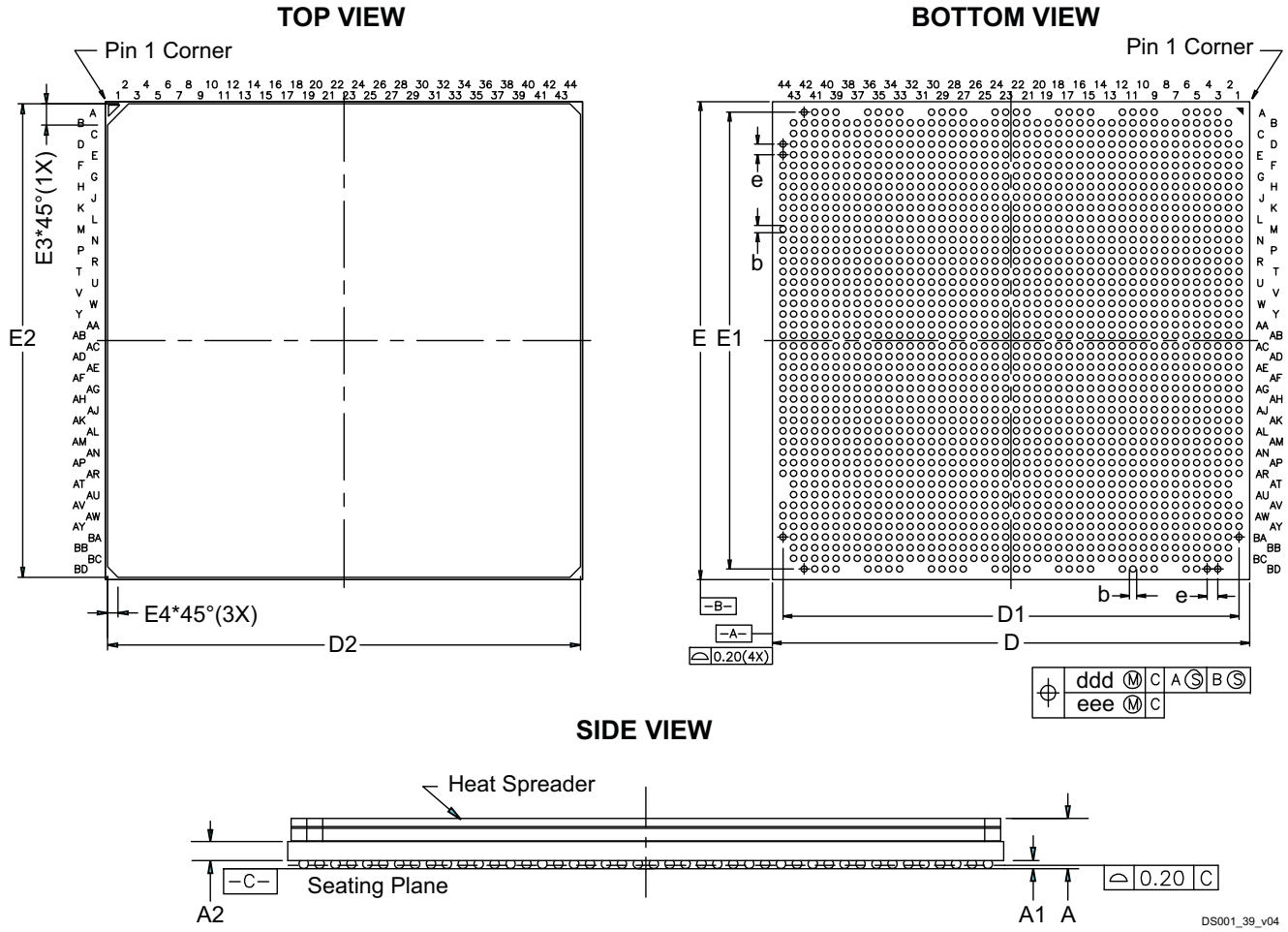


Figure 34: *1892-Pin Fine Ball Grid Array*

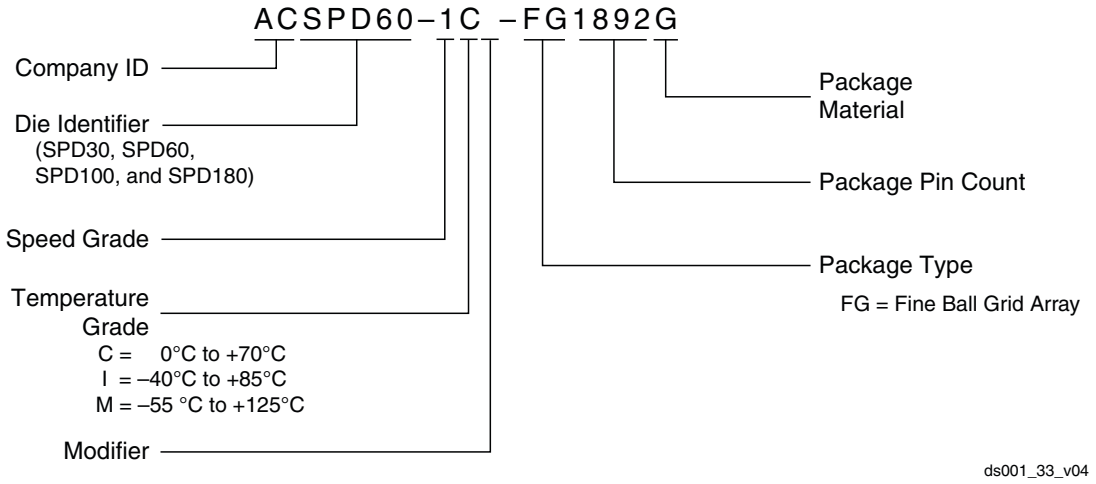
Table 46: *1892-Pin Fine Ball Grid Array Dimensions*

Symbol	Measurement	Tolerance	Units
A	3.14	±0.25	mm
A1	0.50	±0.10	mm
A2	1.19	±0.15	mm
b	0.60	±0.10	mm
ddd	0.25	–	mm
D/E	45.00	±0.10	mm

Table 46: *1892-Pin Fine Ball Grid Array Dimensions (Continued)*

Symbol	Measurement	Tolerance	Units
D1/E1	43.00	–	mm
D2/E2	44.60	±0.05	mm
e	1.00	–	mm
eee	0.10	–	mm
E3	2.00	–	mm
E4	1.00	–	mm

Ordering Information



Revision History

The following table lists the revision history of this document.

Version	Revision
1.0	Initial released version.
1.1	• Corrected pin names (*base_name*_TXN_I to *base_name*_TXN_O) for pins **AR43**, **AT2**, **AU43**, **AV2**, **BA43**, **BB2**, **BC3**, **BC7**, **BC9**, **BC13**, **BC15**, **BC19**, **BC21**, **BC25**, **BC27**, **BC31**, **BC33**, **BC37**, **BC39**, and **BC43**. • Added **"LVTTL,"** on page 32, **"LVCMOS18,"** on page 34, and **"LVCMOS15,"** on page 35. • Updated **"LVCMOS25,"** on page 33. • Updated **Figure 21**, page 21m • Moved I/O leakage specifications to **"I/O Leakage,"** on page 38. • Updated the number of user I/O for the SPD60 in **Table 1**, page 1 and **Table 43**, page 48.
1.2	• Updated the performance of embedded RAM blocks. • Removed support for HyperTransport. • Removed support for PCI and PCI-X. • Updated junction temperature in **Table 9**, page 25 and **Table 10**, page 26. • Updated DDR123 Hard Controller (×8) signal connections for pins **AK1**–**AK3**, **AK42**–**AK44**, **R10**, **R35**, **T10**–**T11**, and **T34**–**T35**. • Updated the M grade temperature range under **"Ordering Information,"** on page 99. • Other minor edits and corrections. • Added **Figure 33**, page 47. • Updated **Table 7**, page 16.

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