CS 61C Fall 2015 (Solutions)
Guerrilla Section 3: Synchronous Digital Systems

Problem 1:

a) Convert the following truth table to a Boolean expression and simplify it. An X means we don't care about the value of that output (it can be either 0 or 1).

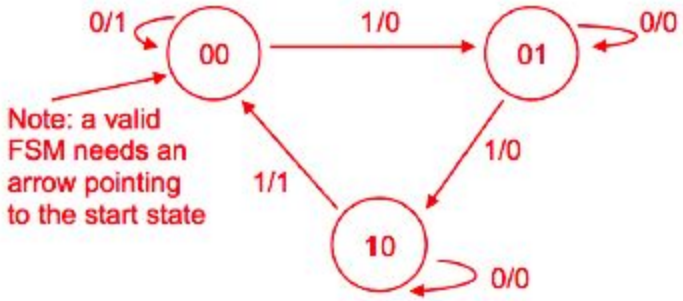
A	B	C	Out
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	X
1	1	1	X

The trick is to set the output of the last 2 rows to 1.
Then we get:
!ABC + A!B!C + AB!C + ABC
So we can group terms 1 and 4 and terms 2 and 3:
=BC(!A + A) + A!C(!B + B)
=BC + A!C
This solution uses 4 gates (2 AND, 1 OR, 1 NOT).

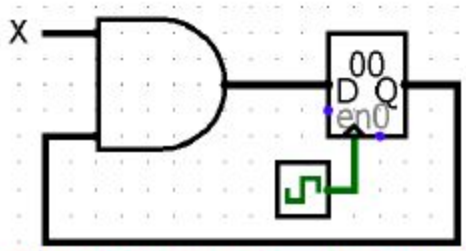
Note that this is a mux! (A and B are the inputs and C is selecting between them)

b) Draw the transition state diagram from a FSM that reads a binary string bit-by-bit and outputs whether the total number of 1s seen since the beginning is divisible by 3.

State = (number of 1s seen) % 3



c) For the circuit below, assume that the setup time is 15ns, hold time is 30ns, and the AND gate delay is 10ns. If the clock rate is 10 MHz and x updates 25ns after the rising edge of the clock, what are the minimum and maximum values for the clk-to-Q delay to ensure proper functionality?



Min: 20 ns

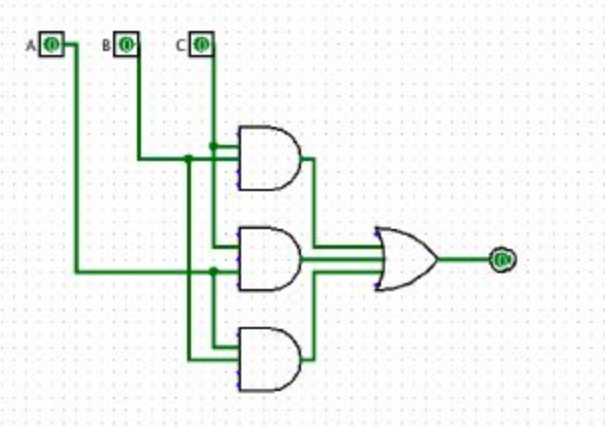
Max: 75 ns

If the clk-to-Q delay is too fast, the input to the register will change before the hold time is finished. Thus, the minimum clk-to-Q delay is $t_{hold} - t_{AND} = 30 - 10 = 20$ns.

On the other hand, we must make sure the critical path is no longer than the clock period, which is 100 ns (= 1/(10 MHz)). In other words, $t_{setup} + t_{AND} + t_{clk\text{-}to\text{-}Q} \leq 100$ns, or $t_{clk\text{-}to\text{-}Q} \leq 100\text{ns} - t_{setup} - t_{AND}$. Solving yields $t_{clk\text{-}to\text{-}Q} \leq 75$ ns.

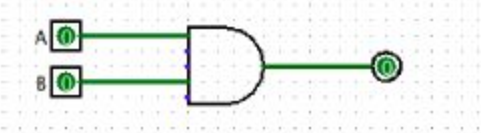
d) Build a 3-bit majority circuit (outputs 1 if 2 or more bits are 1 otherwise outputs 0).

A	B	C	Out
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1



e) Reduce the Boolean expression AB + ABC + ABCD + ABCDE + ABCDEF and draw the logic gate.

AB

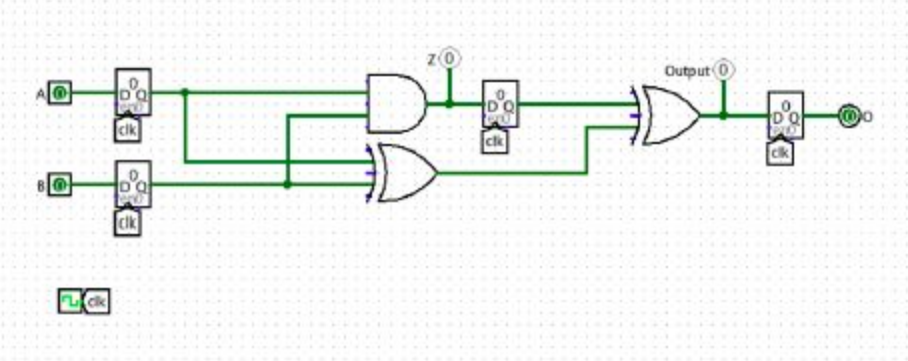


f) Reduce the Boolean expression !(A + !B) * !(C + D + E) + (A + B)*(!C). How many gates needed?

!A*B*!C*!D*!E + A*!C + B*!C = B*!C*(!A*!D*!E + 1) + A*!C = B*!C + A*!C = (!C)*(B + A)
3 gates (1 not, 1 and, 1 or)

Problem 2:

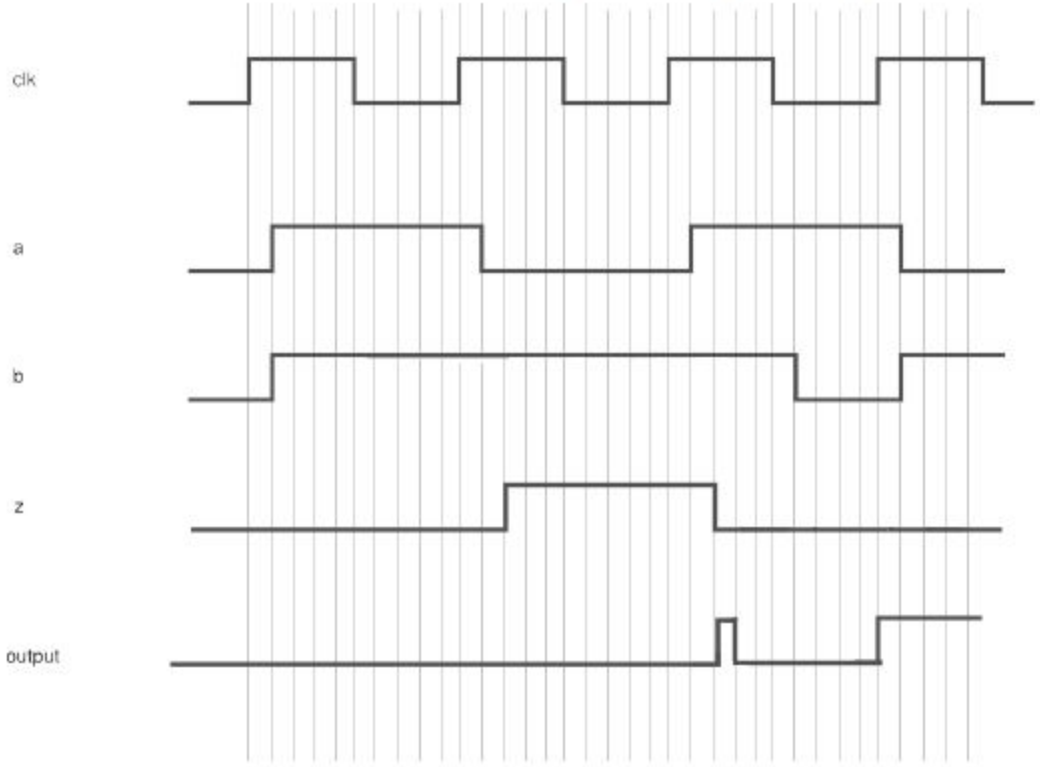
Assume all inputs and outputs are clocked registers, clk-to-q is 1 ns, all gates are 1 ns, setup time is 1 ns, and hold time is 1 ns.



i. Find the max delay and the fastest possible clock rate?

Critical path: 4 ns (clk-to-q + XOR_CL + XOR_CL + output setup time)
Max clock speed: 250 Mhz

ii. Assume each clock cycle lasts 10 ns. Draw the signals below (assume registers are initially 0).



Problem 3:

Using only NAND gates build AND, NOT, and XOR