CS 61C Fall 2015

Guerrilla Section 3: Synchronous Digital Systems

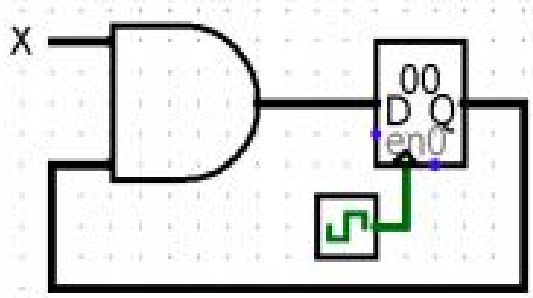
Problem 1:

a) Convert the following truth table to a Boolean expression and simplify it. An X means we don't care about the value of that output (it can be either 0 or 1).

A	B	C	Out
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	X
1	1	1	X

b) Draw the transition state diagram from a FSM that reads a binary string bit-by-bit and outputs whether the total number of 1s seen since the beginning is divisible by 3.

c) For the circuit below, assume that the setup time is 15ns, hold time is 30ns, and the AND gate delay is 10ns. If the clock rate is 10 MHz and x updates 25ns after the rising edge of the clock, what are the minimum and maximum values for the clk-to-Q delay to ensure proper functionality?



Min: _____ns

Max: _____ns

d) Fill in the truth table for a 3-bit majority circuit and build it using logic gates. A 3-bit majority circuit outputs 1 if 2 or more bits are 1, otherwise it outputs 0.

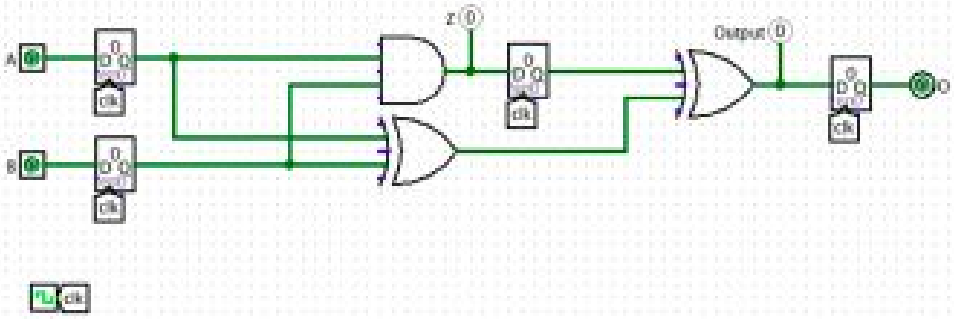
A	B	C	Out
0	0	0	0
1	1	1	1

e) Reduce the Boolean expression AB + ABC + ABCD + ABCDE + ABCDEF and draw the logic gate.

f) Reduce the Boolean expression !(A + !B) * !(C + D + E) + (A + B)*(!C). How many and/or/not gates needed?

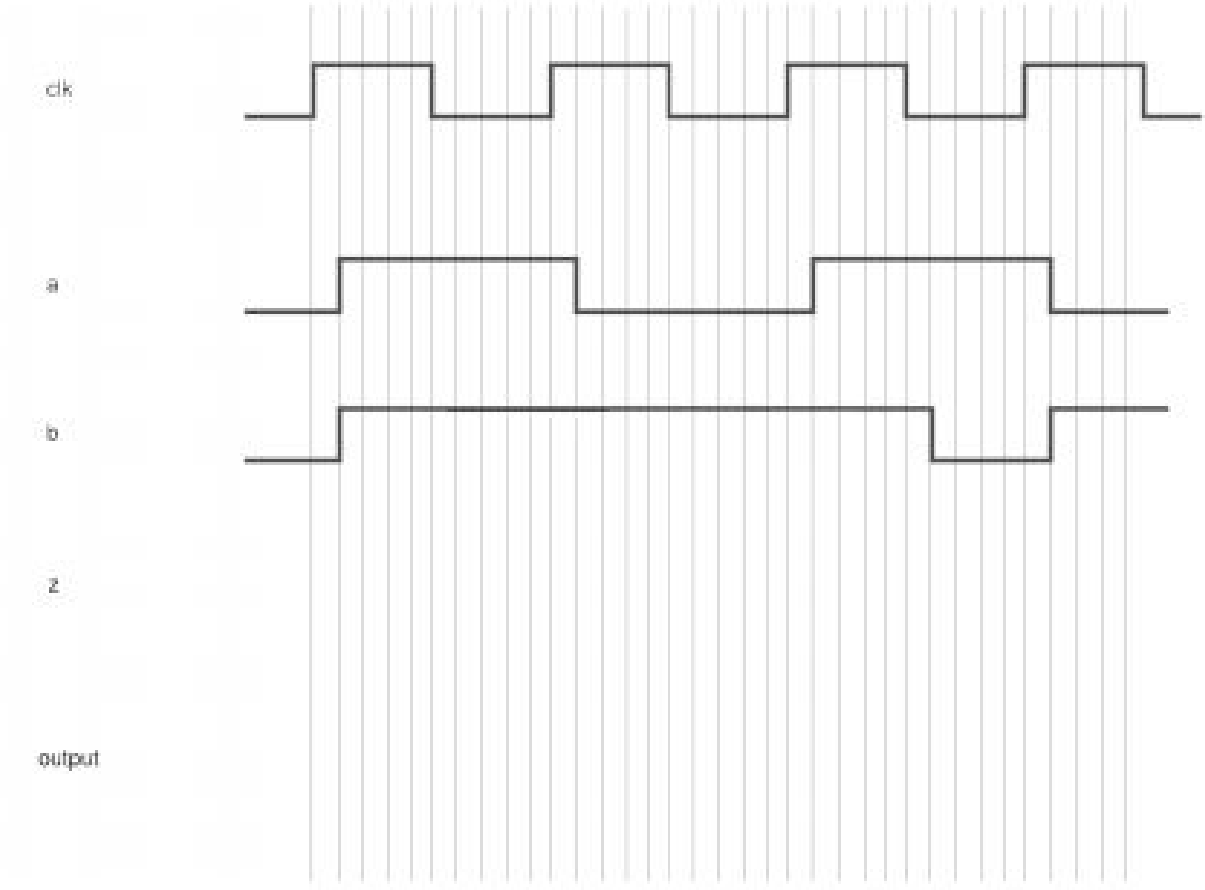
Problem 2:

Assume all inputs (A, B) are clocked registers (note: A and B are separate from the registers shown below directly after them). For all registers assume clk-to-q is 1 ns, setup time is 1 ns, hold time is 1 ns and that they are initialized to 0. Assume the delay for each logic gate is 1 ns.



i. Find the max delay and the fastest possible clock rate such that the behavior of the ?

ii. Assume each clock cycle lasts 10 ns. Draw the signals below (assume registers are initially 0).



Problem 3:

Using only NAND gates build:

i) NOT GATE

ii) AND GATE

ii) OR GATE

ii) XOR GATE