I/O & Performance

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Polling vs. Interrupts

Operation	Definition	Pro/Con	Good for
Polling			
Interrupts			

CPU Performance

- *Iron Law (or Performance Equation)*: CPU time = (# instructions)(CPI)(Clock Period)
  - *# instructions*: how many instructions executed during program (insts/program)
  - *CPI (Cycles per Instruction)*: avg number of cycles to complete an instruction
  - *Clock Period*: Inverse of clock frequency

Performance Problem

- What is the CPI of our pipelined MIPS processor if it has forwarding, every branch delay slot is filled with useful work, and there are no load hazards?

- What if only half of the branch delay slots contain useful work and branches occur about 20% of the time?

Operation Type	Frequency	CPI for CPU A	CPI for CPU B
ALU	50%	2	1
Load	20%	4	2
Store	10%	2	1
Branch	20%	1	1

- If CPU A and B have the same clock speed, how many times faster is B?

- Clearly CPUA is bottlenecked by not having a cache. What would the CPI of Loads and Stores need to be to match the performance of B?

- By only changing the clock speed, how many times faster would that need to be for CPU A to match the performance of B?