CS 61C Spring 2010

Combinational Logic & State

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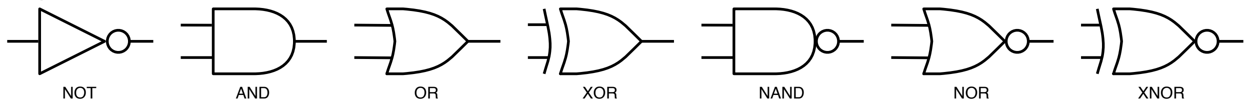
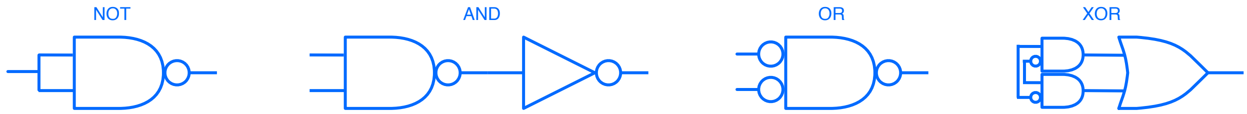
Week 9 (3/16)

Logic Gates

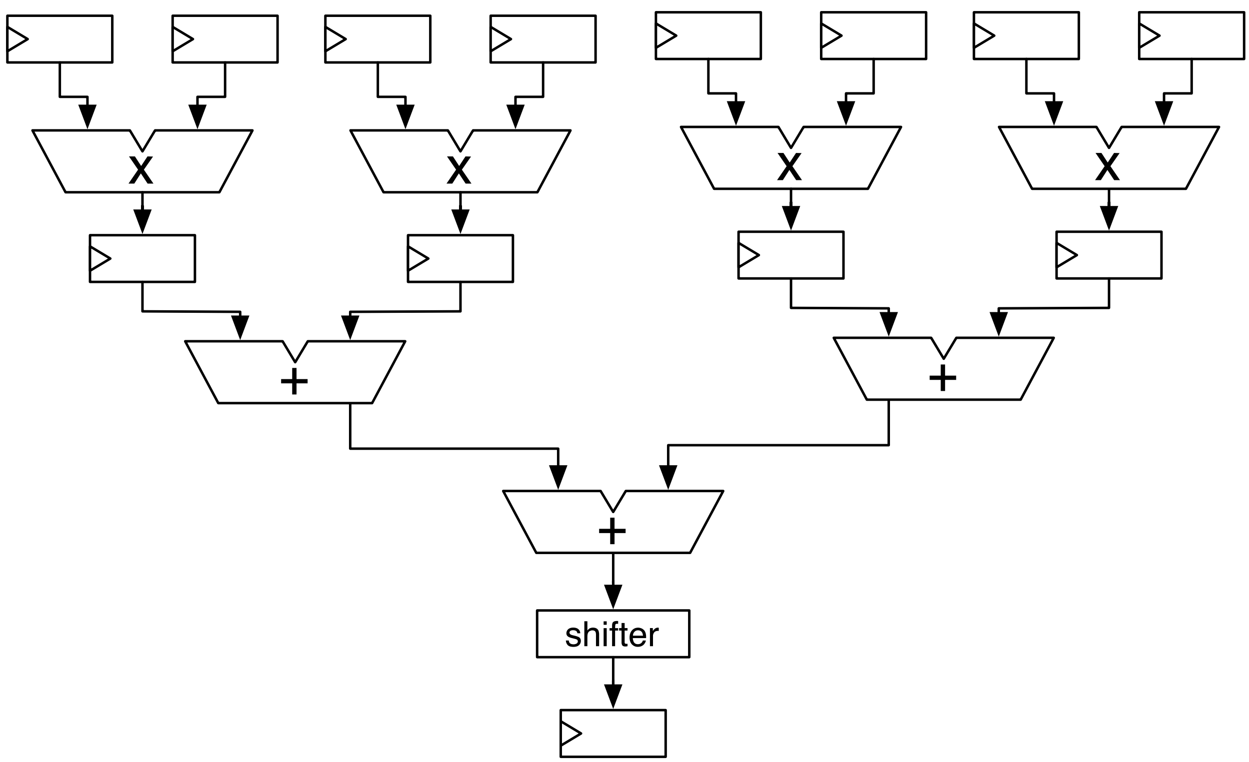


- Looking at what XNOR does, can you think of another name for it? Equality test
- How many different two-input logic gates are possible? $2^4 = 16$
- Build NOT, AND, OR, and XOR using only NAND. To save yourself writing, once you have built a gate, you can re-use it.



Pipelining Problem

- The circuit below computes the weighted average of 4 values
- Logic Delays - t_{mult} = 55ns, t_{add} = 19ns, t_{shift} = 2ns
- Register Parameters - t_{setup} = 2ns, t_{hold} = 1ns, $t_{clk\text{-}to\text{-}q}$ = 3ns
- What is the critical path delay and the maximum frequency this circuit can operate at?
  delay = 3ns + 55ns + 19ns + 19ns + 2ns + 2ns = 100ns => max frequency = 10MHz
- If you add one stage of registers (pipelining), what is the highest frequency you can get?
  delay = 3ns + 55ns + 2ns = 60ns => max frequency = 16.66MHz



Boolean Simplification Practice

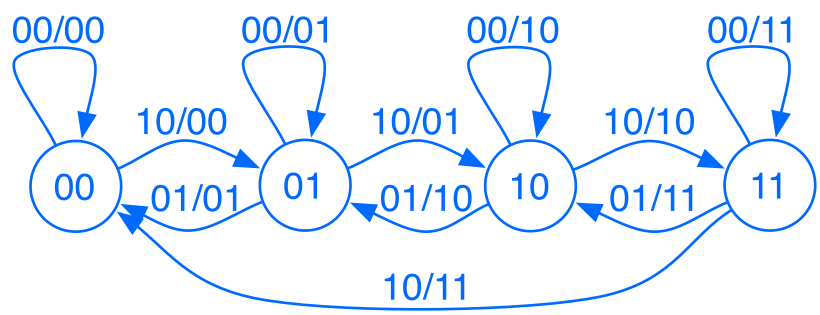
- Minimize the following boolean expressions:

$(A + B)(A + \bar{B})C$	$\bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + AB\bar{C} + A\bar{B}\bar{C} + ABC + A\bar{B}C$	$\bar{A}B + A\bar{B}$
AC	$\bar{C} + AC$	$A \oplus B$

Finite State Machine Practice

- Draw a finite state machine for this system.

increment,decrement/output



- Assign states binary encodings and complete a truth table for your FSM.

Increment	Decrement	Current State	Next State	Output
0	0	00	00	00
0	1	00	11	00
1	0	00	01	00
1	1	00	xx	00
0	0	01	01	01
0	1	01	00	01
1	0	01	10	01
1	1	01	xx	01
0	0	10	10	10
0	1	10	01	10
1	0	10	11	10
1	1	10	xx	10
0	0	11	11	11
0	1	11	10	11
1	0	11	00	11
1	1	11	xx	11

- Starting from sum-of-product expressions from the truth table, derive simplified expressions for next state as well as the output.
- Output = State
- $NS0 = CS0 \oplus (I + D)$ $NS1 = CS1\bar{I}\bar{D} + (CS0 \oplus CS1)\bar{I}D + (CS0 \oplus CS1)I\bar{D}$