Discussion 13: VM (cont), I/O

1. Consider a call to the following MIPS code (no delay slots) with the given initial page table. Assume that pages are 4KiB and that all page faults (but not protection faults) can be serviced by the OS without evicting pages. $sp is initially 0x6004, $ra is initially 0x1040, and $a0 is initially 0x1.

MIPS

V.A.	Instructions
0x2004	Foo: addiu $sp, $sp, -4
0x2008	sw $ra, 0($sp)
0x200C	beq $a0, $zero, Skip
0x2010	addiu $a0, $a0, -1
0x2014	jal Foo
0x2018	Skip: lw $ra, 0($sp)
0x201C	addiu $sp, $sp, 4
0x2020	jr $ra

Initial Page Table			
Valid	Dirty	A.R.	P.P.N.
0	0	None	4
1	0	Read, Exec	5
0	0	Read, Exec	1
0	0	None	1
0	0	Read, Write	12
1	0	Read, Write	3
1	0	Read, Write	2
…	…	…	…

a. Where will page faults occur in the execution of this function?

b. Assuming that we don't have a TLB, (or that all the TLB was flushed), what will be in the page table after this function is completely executed?

Final Page Table			
Valid	Dirty	A.R.	P.P.N.
…	…	…	…

c. Suppose $a0 were initially 0xC00 instead of 0x1, what other exceptions can occur?

2. Fill this table of polling and interrupts.

Operation	Definition	Pro/Good for	Con
Polling			
Interrupts			

3. Memory Mapped I/O
   Certain memory addresses correspond to registers in I/O devices and not normal memory.
   0xFFFF0000 – Receiver Control:
   Lowest two bits are interrupt enable bit and ready bit.
   0xFFFF0004 – Receiver Data:
   Received data stored at lowest byte.
   0xFFFF0008 – Transmitter Control
   Lowest two bits are interrupt enable bit and ready bit.
   0xFFFF000C – Transmitter Data
   Transmitted data stored at lowest byte.

   Write MIPS code to read a byte from the receiver and immediately send it to the transmitter.