CS61c Spring 2014 Discussion 10 – Single Cycle Datapath & Control

1 Register Transfer Language (RTL)

- Use to describe flow of data: $dest \leftarrow src$
- Each line happens in parallel (at the same time): $b \leftarrow c$, $a \leftarrow b$
- In MIPS, use R[x] for register x, and Mem[y] for memory at y.

2 CPU Design

On the next page is the basic datapath as discussed in lecture, shown in simplified format, in which all wires are 32 bits wide, except wires for registers and an immediate. For convenience, the control block is visually split into input and output blocks.

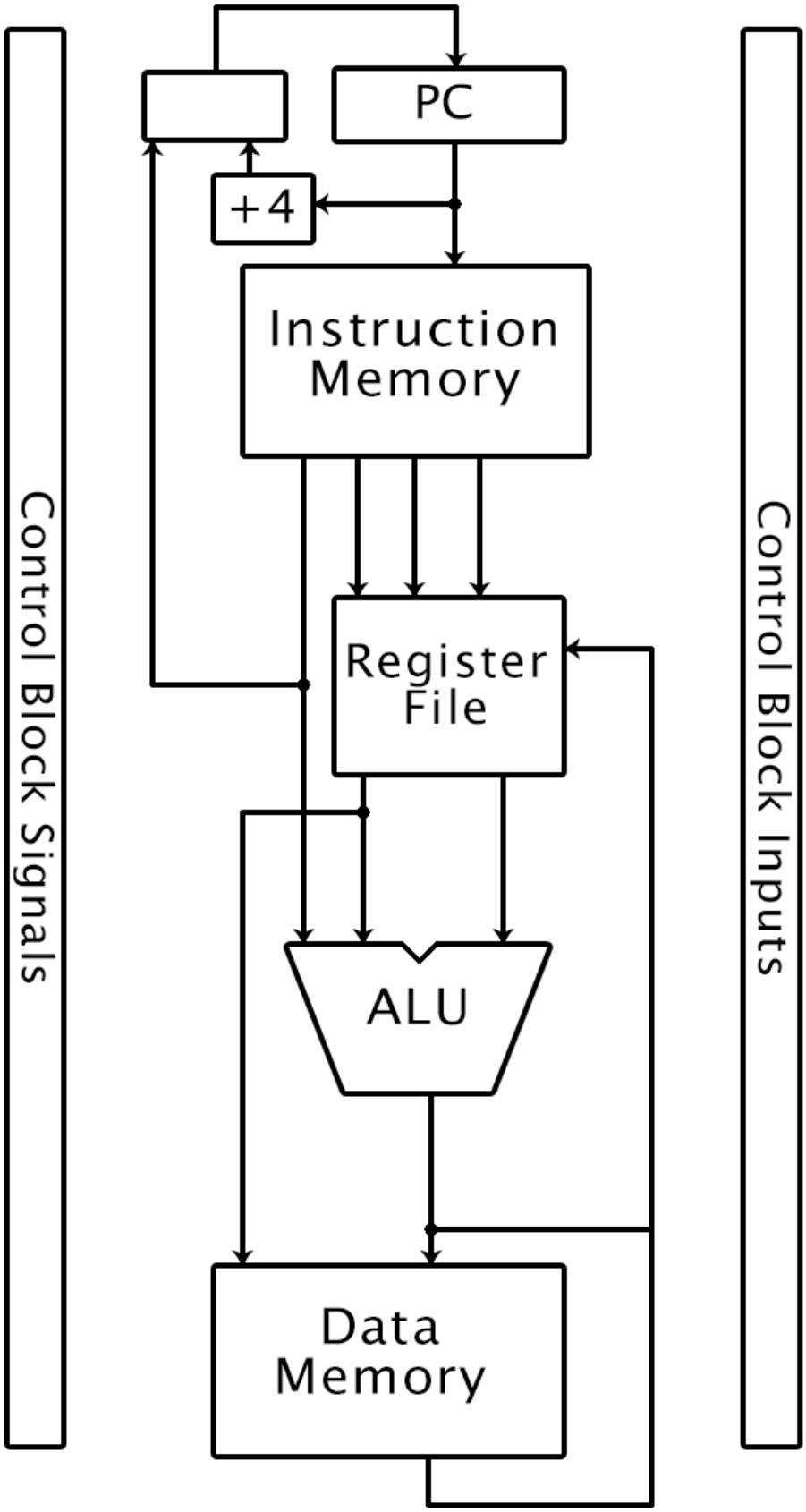
3 Exercises

For the following exercises, assume that the ALU is able to output an "equals" signal, which is high/on/one when its two inputs are equal.

1. Label the wires in the datapath diagram, describing what data is on each line. For example, one of the outputs of the registers block might be R[rs].
2. Add control signals and missing elements (such as multiplexers) to the diagram so that the datapath can execute the following instructions: `add`, `lui`, `sw`, `bne`, `j`.
3. Fill out the values for the control signals from question 2 (Write your control signals' names along the top row):

Inst								
`add`								
`lui`								
`sw`								
`bne`								
`j`								

4. Suppose you wanted to add a new instruction, `beqr`, which will be used like this: `beqr $x, $y, $z` will branch to the address in `$z` if `$x` and `$y` are equal, otherwise continue to the next instruction. Show any changes that would need to be made to the datapath to make this instruction work.


Control Block Signals
PC
+4
Instruction Memory
Register File
ALU
Data Memory
Control Block Inputs