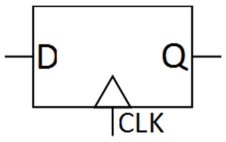
State Elements

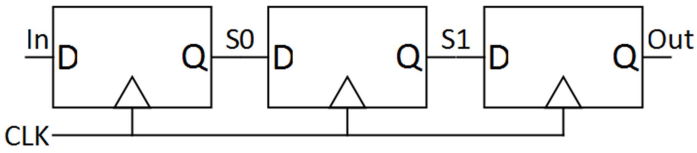
State elements provide a means of storing values, and controlling the flow of information in the circuit. The most basic state element (we're concerned with) is a DQ Flip-Flop:



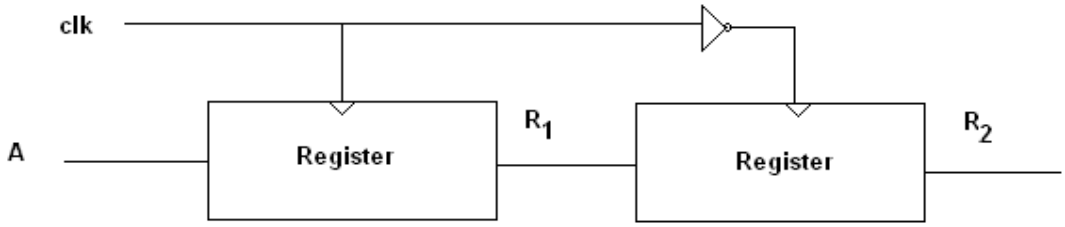
D is a single bit input, Q is a single bit output. On the **rising edge** of the clock, the value from D is copied to Q, after a small delay (known as the CLK-to-Q delay). At all other times, Q presents the value last copied and ignores D.

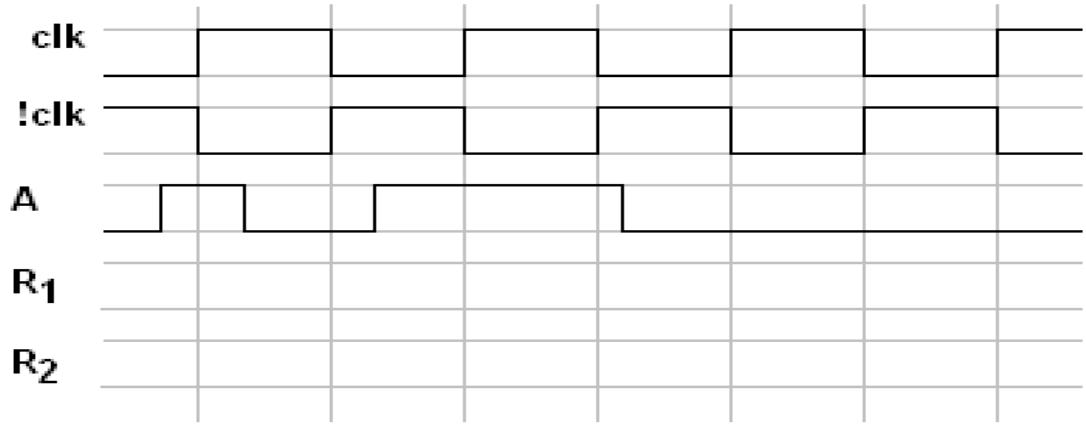
An n-bit register is just n DQ Flip-Flops aligned in parallel, tied to the same clock.

Timing Diagram 1: Fill out the timing diagram for the circuit below



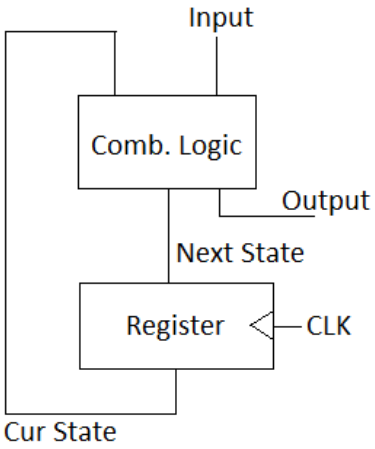
Timing Diagram 2: Fill out the timing diagram for the circuit below





Finite State Machines

FSMs can be an incredibly useful computational tool. They have a straightforward implementation in hardware:



The register holds the current state (encoded as a particular combination of bits), and the combinational logic block maps from {current state, input} to {next state, output}.

Exercises

Draw a transition diagram for an FSM that can take in an input sequence one bit at a time, and after each input is received, output whether the number of 1s is divisible by 3. Write out the truth table that the combinational logic block must implement (remember to assign each state a binary encoding). Finally, write the Boolean algebra expressions that implement the FSM's truth table.

Clocking Methodology

- The input signal to each state element must stabilize before each rising edge.
- Critical path: Longest delay path between state elements in the circuit.
- Min clock period = $t_{clk\text{-}to\text{-}q} + t_{CL} + t_{setup}$, where t_{CL} is the Combinational Logic delay in the critical path.
- If we place registers in the critical path, we can shorten the period by reducing the amount of logic between registers

Clocking Problem

- The circuit below computes the weighted average of 4 values
- Logic Delays - t_{mult} = 55ns, t_{add} = 19ns, t_{shift} = 2ns
- Register Parameters - t_{setup} = 2ns, t_{hold} = 1ns, $t_{clk\text{-}to\text{-}q}$ = 3ns

What is the critical path delay and the maximum clock rate this circuit can operate at?

If you add one stage of registers (pipelining), what is the highest clock rate you can get?