CS61C Summer 2018 Discussion 6 – Single Cycle Datapath

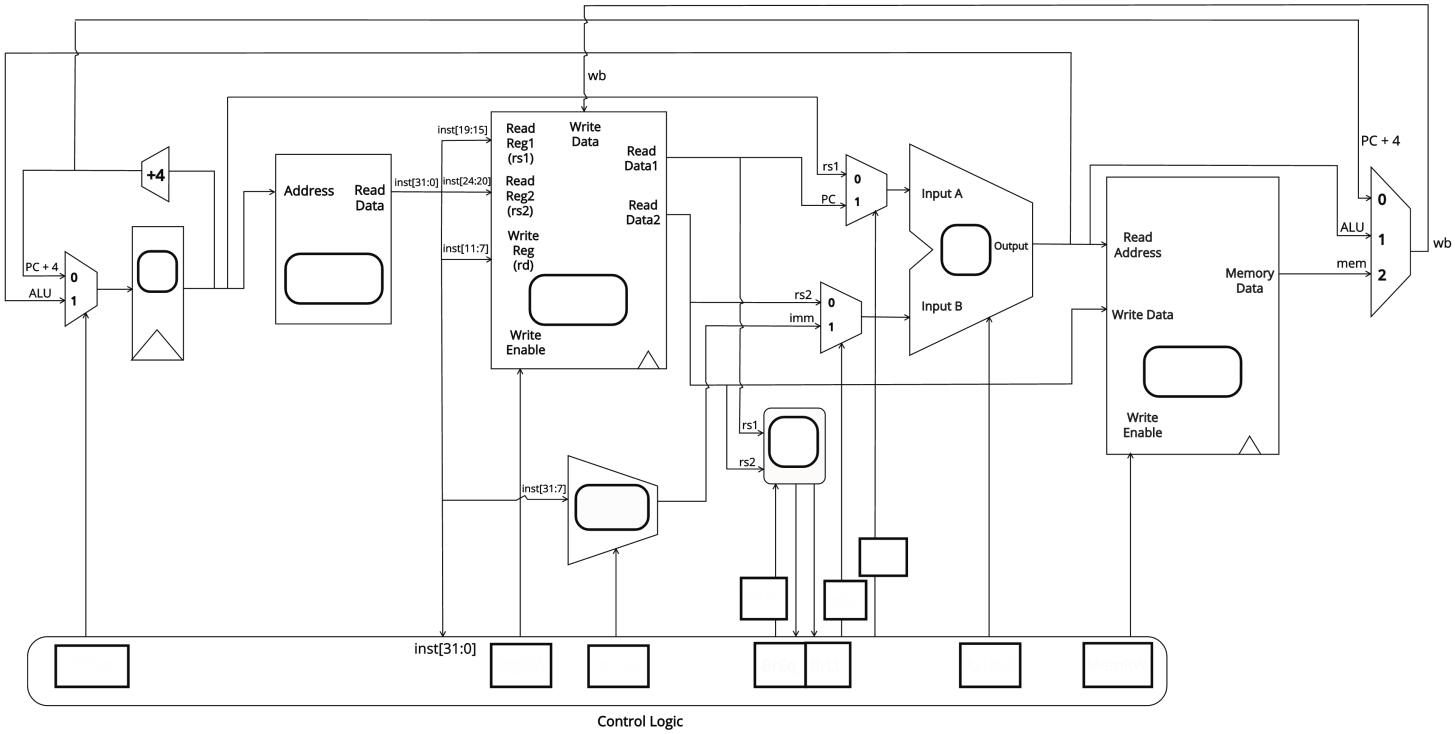
Single Cycle CPU Design

1. Fill in each blank box with **round** edges on the datapath below with the name of the datapath component.

2. Name each datapath stage and explain what happens in that stage.

Stage	Functionality
IF:	
ID:	
EX:	
MEM:	
WB:	

3. Fill in each blank box with with **square** edges on the datapath below with the name of the control signal.



Single Cycle CPU Control Logic

1. Fill out the following table with the control signals for each instruction based on the datapath on the previous page. Wherever possible, use * to indicate that what this signal is does not matter.

	BrEq	BrLT	PCSel	ImmSel	BrUn	ASel	BSel	ALUSel	MemRW	RegRW	WBSel
add											
ori											
lw											
sw											
beq											
jal											
bltu											

Single Cycle CPU Performance Analysis

Clocking Methodology Overview

- A **"state element"** is an element connected to the clock (denoted by a triangle at the bottom). The **input signal** to each state element must stabilize before each **rising edge**.
- The **critical path** is the longest delay path between state elements in the circuit. If we place registers in the critical path, we can shorten the period by **reducing the amount of logic between registers**.

For this exercise, assume the delay for each stage in the datapath is as follows:

Stage	IF	ID	EX	MEM	WB
Delay	200 ps	100 ps	200 ps	200 ps	100 ps

1. Mark the stages of the datapath that the following instructions use and calculate the total time needed to execute the instruction.

	IF	ID	EX	MEM	WB	Total Time
add						
ori						
lw						
sw						
beq						
jal						
bltu						

2. Which instruction(s) exercise the critical path?

3. What is the fastest you could clock this single cycle datapath?

4. Why is the single cycle datapath inefficient?

5. How can you improve its performance? What is the purpose of pipelining?