



## 1.3 Clocking Methodology

- A **state element** is an element connected to the clock (denoted by a triangle at the bottom). The **input signal** to each state element must stabilize before each **rising edge**.
- The **critical path** is the longest delay path between state elements in the circuit. If we place registers in the critical path, we can shorten the period by **reducing the amount of logic between registers**.

For this exercise, assume the delay for each stage in the datapath is as follows:

IF: 200 ps      ID: 100 ps      EX: 200 ps      MEM: 200 ps      WB: 100 ps

- (a) Mark the stages of the datapath that the following instructions use and calculate the total time needed to execute the instruction.

	IF	ID	EX	MEM	WB	Total Time
add						
ori						
lw						
sw						
beq						
jal						
bltu						

- (b) Which instruction(s) exercise the critical path?
- (c) What is the fastest you could clock this single cycle datapath?
- (d) Why is the single cycle datapath inefficient?
- (e) How can you improve its performance? What is the purpose of pipelining?

