(10.32) $V_{OUT} = V_{IN} \frac{R_L}{R_o' + R_L}$ FOR THE VOLTAGE FOLLOWER. AS $R_L \to \infty$ $V_{OUT} = V_{IN} = 5V$

WHEN $R_L = 1000\Omega$

$$V_{OUT} = (5 - 0.01m)V = V_{IN} \cdot \frac{R_L}{R_o' + R_L}$$

$$\Rightarrow \quad 5 - 0.01m = 5 \frac{1000}{R_o' + 1000}$$

$$\Rightarrow \quad R_o' = \underline{\underline{2 \times 10^{-3} \Omega}}$$

(10.33) $V_{OUT} = 15 \cos \omega t + 0.225 \cos^2 \omega t$

NOTE THAT $\cos^2 x = \frac{1}{2}(\cos 2x + 1)$. THUS

$$V_{OUT} = \underset{(\text{freq}=0)}{0.1125} + \underset{(\omega)}{15 \cos \omega T} + \underset{(2\omega)}{0.1125 \cos 2\omega t}$$

(10.34) $V_{OUT} = 15[\cos \omega t + \sin \omega t] + 0.225[\cos \omega_1 t + \cos \omega_2 t]^2$

NOTE THAT $\cos A \cos B = \frac{1}{2}[\cos(A+B) + \cos(A-B)]$

THE TERM IN V_{OUT} CONTAINING THE FREQ. $(\omega_1 - \omega_2)$ IS THUS

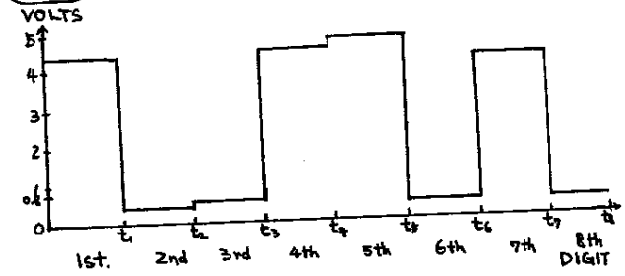
$$(0.225)(2)\left(\tfrac{1}{2}\right) \cos(\omega_1 - \omega_2)t$$

$$= 0.225 \cos(\omega_1 - \omega_2)t$$

THIS PROBLEM ILLUSTRATES <u>INTERMODULATION</u>.

CHAPTER 11 – PROBLEMS

(11.1) DIGITS = 1001101.0



(11.2) (a) THE BINARY DIGIT "1" IS USED TO REPRESENT THE VALUE OF ONE FOR BINARY NUMBER REPRESENTATION.

(b) A SWITCHING VARIABLE $\underset{\sim}{A}$ IS A VARIABLE WHICH TAKES ON LOGIC VALUE OF EITHER ONE OR ZERO; BUT NO OTHER POSSIBILITIES EXIST, DEPENDING ON THE VOLTAGE AT A.

(c) LOGICAL STATE $\underset{\sim}{1}$ REPRESENTS A VOLTAGE SIGNAL LYING IN ITS HIGH RANGE IN POSITIVE LOGIC AND LOW RANGE IN NEGATIVE LOGIC.

(d) THE "HIGH" RANGE IS THE RANGE OF VOLTAGES ALLOWED, WHICH REPRESENTS LOGIC STATE "$\underset{\sim}{1}$"

IN POSITIVE LOGIC AND LOGIC STATE 0 IN NEGATIVE LOGIC. ■

11.3 (a)

A	B	$\bar{A}$	F
0	0	1	1
1	0	0	1
0	1	1	0
1	1	0	1

(b)

A	B	$\bar{A}$	$\bar{B}$	F
0	0	1	1	0
1	0	0	1	0
0	1	1	0	0
1	1	0	0	1

(c)

A	B	C	$\bar{B}$	$\bar{C}$	F
0	0	0	1	1	0
0	0	1	1	0	0
0	1	0	0	1	0
0	1	1	0	0	0
1	0	0	1	1	1
1	0	1	1	0	0
1	1	0	0	1	0
1	1	1	0	0	0

■

11.4 (a)

A	B	AB	A + B	(AB)(A+B)	F
0	0	0	0	0	1
1	0	0	1	0	1
0	1	0	1	0	1
1	1	1	1	1	0

(THIS IS EQUIVALENT TO A NAND OPERATION)

(b)

A	$\bar{A}$	$A\bar{A}$ (=F)
0	1	0
1	0	0

IT IS IMPOSSIBLE FOR A AND $\bar{A}$ TO BOTH EQUAL 1. HENCE $A\bar{A}$ IS ALWAYS ZERO, NO MATTER WHAT A IS.

(c)

A	B	$A \oplus B$	$A \odot B$	F
0	0	0	1	1
1	0	1	0	1
0	1	1	0	1
1	1	0	1	1

INSPECTING THE TRUTH TABLES FOR $\oplus$ AND $\odot$, WE SEE THAT WHENEVER THE OUTPUT OF $\oplus$ IS 1, THE OUTPUT OF $\odot$ IS 0, AND VICE VERSA. THUS THE OR OPERATION PERFORMED ON THER OUTPUTS ALWAYS GIVES 1. ■

11.5 (a) $F = \overline{\bar{A}B}$

(b) $F = \overline{\bar{A}+\bar{B}}$

(c) $F = A\bar{B}\bar{C}$

11.6 (a) $F = \overline{(AB)(A+B)}$

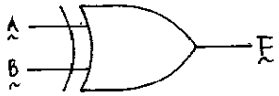
(b) $F = A\bar{A}$

(c) $F = A \oplus B + A \odot B$

11.7 (1) NEGATIVE LOGIC — HIGH: 0 ; LOW: 1

A	B	F
1	1	0
1	0	1
0	1	1
0	0	0

SO THIS IS EXACTLY AN <u>EXCLUSIVE-OR</u> OPERATION. LOGIC BLOCK NEEDED IS AS FOLLOWS:



(2) POSITIVE LOGIC
— HIGH: 1 ; LOW: 0

A	B	F
0	0	1
0	1	0
1	0	0
1	1	1

THIS TIME IT IS THE <u>COINCIDENCE</u> OPERATION.

11.8 (a) $(1+0)1 = 1 \cdot 1 = 1$

(b) $0 + (1\bar{1})1 = (1\bar{1})1 = (1 \cdot 0)1 = 0 \cdot 1 = 0$

(c) $\overline{(1+0)}(1+1) = \bar{1}(1) = 0 \cdot 1 = 0$

11.9 (a) $F = (X+Y)\bar{X}$

X	Y	X+Y	$\bar{X}$	F
0	0	0	1	0
1	0	1	0	0
0	1	1	1	1
1	1	1	0	0

(b) $F = (Y \cdot Z)\bar{X} + X$

X	$\bar{X}$	Y	Z	$Y \cdot Z$	$(Y \cdot Z)\bar{X}$	F
0	1	0	0	0	0	0
0	1	0	1	0	0	0
0	1	1	0	0	0	0
0	1	1	1	1	1	1
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	0	0	1
1	0	1	1	1	0	1

11.10 (a) THERE WOULD BE FOUR ROWS IN THE TRUTH TABLE. THERE ARE TWO POSSIBILITIES IN EACH ROW i.e. 1 OR 0. SO THE NUMBER OF <u>DIFFERENT</u> SWITCHING FUNCTIONS IS

$$2^4 = 16$$

(b)

A	B	F
0	0	1
0	1	0
1	0	1
1	1	0

$$F = A'B' + AB'$$
$$= B'(A' + A)$$
$$= B'$$

(c) SIMILARLY, THERE ARE 2^3 ROWS. THEREFORE FOR THREE INPUTS, THERE ARE $2^{2^3} = 256$ DIFFERENT SWITCHING FUNCTIONS. ■

11.11 (a)

A	1	(A)(1)
0	1	0
1	1	1

COMPARING 1st AND 3rd COLUMN, WE KNOW

$$A = (A)(1)$$

(b)

A	$\bar{A}$	$A + \bar{A}$
0	1	1
1	0	1

THEREFORE $A + \bar{A} = 1$ ■

11.12

A	B	A+B	A(A+B)
0	0	0	0
0	1	1	0
1	0	1	1
1	1	1	1

COMPARING 1st AND 4th COLUMN, WE GET

$$A = A(A + B)$$

11.13

A	B	C	A+B	A+C	(A+B)(A+C)	BC	A+BC
0	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0
0	1	0	1	0	0	0	0
0	1	1	1	1	1	1	1
1	0	0	1	1	1	0	1
1	0	1	1	1	1	0	1
1	1	0	1	1	1	0	1
1	1	1	1	1	1	1	1

COMPARING THE LAST AND THE LAST BUT TWO COLUMNS, WE SHOWED THAT $(A+B)(A+C) = A + BC$ ■

11.14 <u>DE MORGAN'S THM</u>

FROM THE TRUTH TABLE $\overline{AB} = \bar{A} + \bar{B}$

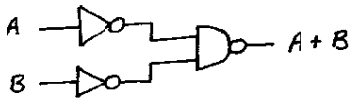
A	B	AB	$\overline{AB}$	$\bar{A}$	$\bar{B}$	$\bar{A}+\bar{B}$
0	0	0	1	1	1	1
0	1	0	1	1	0	1
1	0	0	1	0	1	1
1	1	1	0	0	0	0

■

11.15 BY DE MORGAN'S THM,

$$A+B \equiv \overline{(\overline{A+B})} = \overline{(\overline{A}\,\overline{B})}$$

HENCE THE FOLLOWING CIRCUIT PERFORMS THE "OR" OPERATION:



■

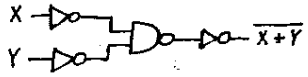
11.16 (a) WHEN $A=0$, WE HAVE A NAND GATE WITH BOTH INPUTS ZERO $\Rightarrow F=1$. WHEN BOTH INPUTS TO NAND ARE 1, $F=0$.

(b) WHEN $A=1$, THE INPUTS TO NAND ARE $1,1 \Rightarrow F=0$. WHEN $A=0$, THE INPUTS TO NAND ARE $0,1 \Rightarrow F=1$. ■

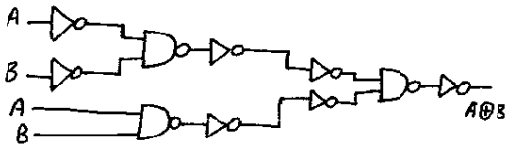
11.17 FIG 11.12 SHOWS HOW TO MAKE AN XOR OUT OF TWO "NOR'S" AND ONE "AND". FROM DE MORGAN'S THM, $\bar{A}+\bar{B}=\overline{AB}$, OR, IF WE RENAME $\bar{A}=X$, $\bar{B}=Y$,

$$X+Y=\overline{\bar{X}\,\bar{Y}} \Rightarrow \overline{X+Y}=\bar{X}\,\bar{Y}$$

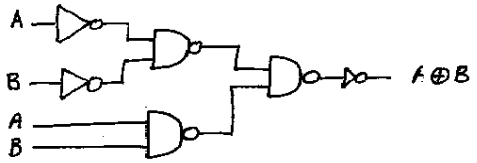
THUS A NOR GATE IS REALIZED BY



11.17 (CONT'D) THUS FROM FIG 11.12,

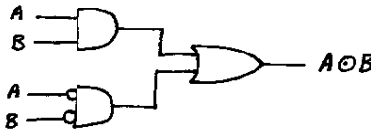


(ALL INPUTS MARKED "A" ARE CONNECTED TOGETHER, ETC.) ELIMINATING THE DOUBLE NEGATIVES, THIS SIMPLIFIES TO



THE INVERTERS CAN BE IN EITHER FORM SHOWN IN FIG. 9.33. ■

11.18 WE WANT AN OUTPUT OF 1 WHEN INPUTS OF 0,0 OR 1,1 ARE PRESENTED. USING THE SUM-OF-PRODUCTS METHOD WE HAVE

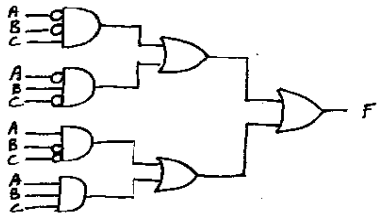


■

11.19 THE DESIRED TRUTH TABLE IS

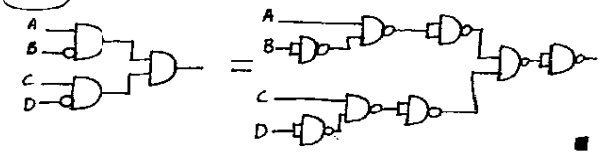
A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

TO AVOID A 4-INPUT OR GATE WE REALIZE (USING SUM-OF-PRODUCTS METHOD) AS FOLLOWS:



■

11.20

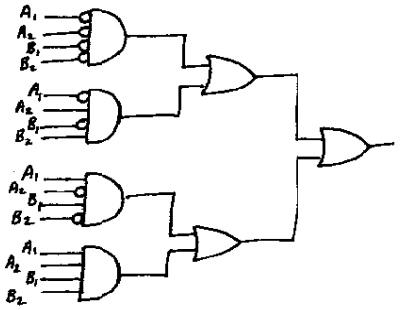


■

11.21 THE ONLY SETS OF INPUTS FOR WHICH THE OUTPUT SHOULD BE 1 ARE

A_1 A_2	B_1 B_2
0 0	0 0
0 1	0 1
1 0	1 0
1 1	1 1

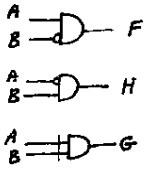
THUS WE OBTAIN FROM SUM-OF-PRODUCTS



FOR THE INVERTERS USE FIG 11.33 (a OR b). FOR THE OR GATES SEE PROBLEM 11.15. ■

11.22

A	B	F	G	H
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0



■

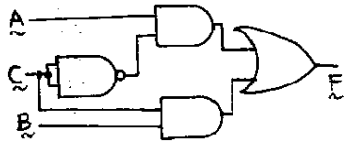
11.23

A	B	C	E
0	0	0	0
0	1	0	0
1	0	0	1
1	1	0	1
0	0	1	0
0	1	1	1
1	0	1	0
1	1	1	1

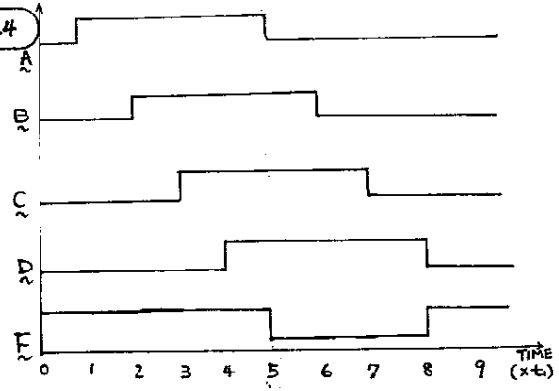
$\therefore E = A\bar{C} + BC$

IT CAN BE REALIZED AS FOLLOWS:

MULTIPLEXER



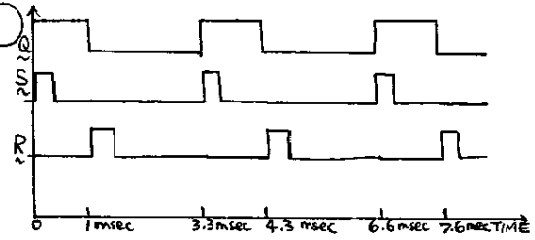
11.24



(1)

A	B	C	D	$\overline{AB}$	C+D	$E = \overline{\overline{AB}(C+D)}$
0	0	0	0	1	0	1
0	0	0	1	1	1	0
0	0	1	0	1	1	0
0	0	1	1	1	1	0
0	1	0	0	1	0	1
0	1	0	1	1	1	0
0	1	1	0	1	1	0
0	1	1	1	1	1	0
1	0	0	0	1	0	1
1	0	0	1	1	1	0
1	0	1	0	1	1	0
1	0	1	1	1	1	0
1	1	0	0	0	0	1
1	1	0	1	0	1	1
1	1	1	0	0	1	1
1	1	1	1	0	1	1

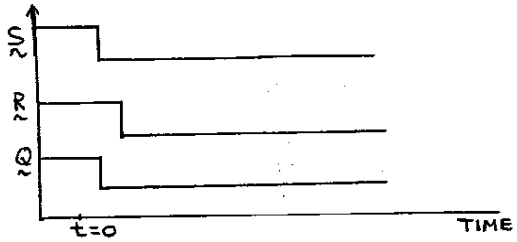
11.25



NOTE THAT THE PERIOD OF THE LOGIC STATE 1 OF S OR R NEED NOT BE 1 msec LONG. IT CAN BE A SHORTER PULSE. ■

11.26 a) FOR $t<0$, $S = 1$ AND $R = 1$, Q WOULD BE 1.

(b) THE TIMING DIAGRAM IS AS FOLLOW



SINCE THE DELAY TIME OF THE WIRE TO R IS LONGER, THERE IS A DURATION WHEN $R = 1$ AND $S = 0$. SO Q WOULD BE RESET FROM 1 TO 0. THE FINAL VALUE IS THEN 0.

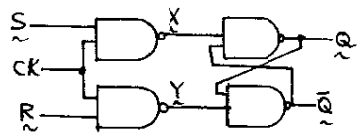
THIS PROBLEM ILLUSTRATES HOW THE INPUT $S=1$, $R=1$ CAN LEAD TO UNPREDICTABLE RESULTS. IN THIS CASE THE FINAL OUTPUT DEPENDS ON THE LENGTH OF THE WIRES (OVER WHICH THE SYSTEM DESIGNER MAY HAVE LITTLE CONTROL.) ■

11.27

S	R	Q (QUESS)	$\bar{Q}$ (QUESS)	Q	$\bar{Q}$
0	0	1	0	1	0
0	0	0	1	0	1
1	0	1	0	1	0
0	1	0	1	0	1
1	1	1	1	1	1

■

11.28

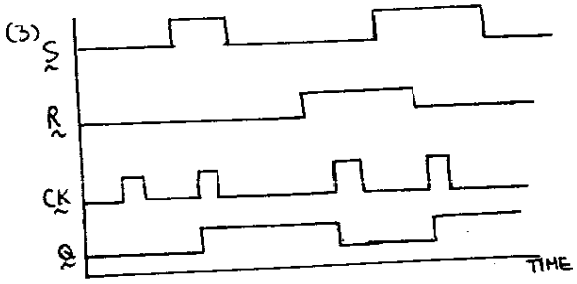


THE CIRCUIT ON THE RIGHT SIDE IS JUST A S-R FLIP-FLOP EXCEPT THAT $X = \bar{S}_R$, $Y = \bar{R}_R$.

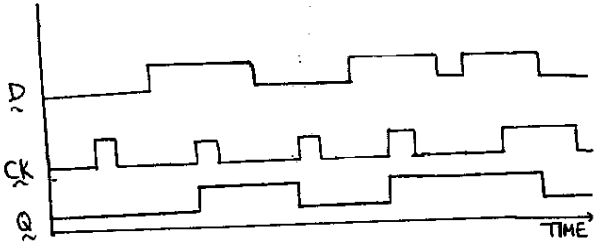
(1) WHEN $CK = 0$, $X = 1$, $Y = 1$. SO $S_R = R_R = 0$ THEREFORE THE VALUE OF Q DOES NOT CHANGE.

(2) WHEN $CK = 1$, $X = \bar{S}$, $Y = \bar{R}$ SO $S_R = S$ AND $R_R = R$. THEREFORE IT IS JUST ACTING LIKE AN ORDINARY S-R FLIPFLOP.

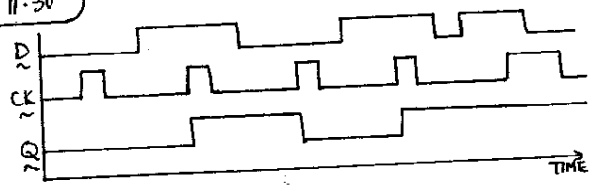
(3)



11.29

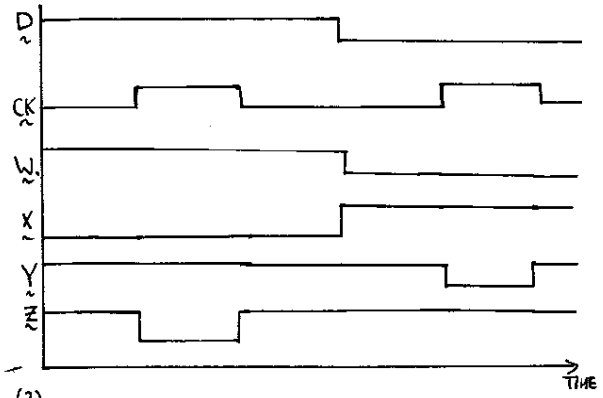


11.30

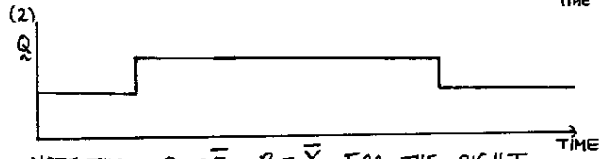


THE ONLY DIFFERENCE BETWEEN AN EDGE-TRIGGERED AND A NON-EDGE-TRIGGERERED FLIPFLOP IS THAT IN THE LATTER, THE VALUE OF Q CHANGE DURING THE ENTIRE HIGH STATE OF CK, WHEREAS THE FORMER ONE WOULD NOT. (NOTE EFFECT OF THE LAST CLOCK PULSE IN THE TWO CASES.) ■

11.31 (1)



(2)



NOTE THAT $S = \overline{Z}$, $R = \overline{Y}$ FOR THE RIGHT S-R FLIP-FLOP. ■

11.32 (a) IT'S GIVEN BY $V_{IH} = 2$ VOLTS

(b) IT'S GIVEN BY THE LOWEST (WORST-CASE) $V_{IL} = 0.7$ VOLTS

(c) WORST CASE IS MIN$[V_{OH}] = 2.4$ VOLTS

(d) WORST CASE IS MAX$[V_{OL}] = 0.5$ VOLTS

(e) TWO CONDITIONS MUST BE SATISFIED.

(1) $V_{OH} \geq V_{IH}$ [ie. $V_c \geq V_a$]

(2) $V_{OL} \leq V_{IL}$ [ie. $V_d \leq V_b$]

WE CAN SEE THAT $V_c = 2.4$ VOLTS $> V_a$

AND $V_d = 0.5$ VOLTS $< V_b$

THEREFORE THE CONDITIONS ARE SATISFIED ■

END

CHAPTER 12 - EXERCISES

Ex 12.1 CONVERTING 258_{16} TO DECIMAL,

$$258_{16} = 8(1) + 5(16) + 2(16)^2 = 600_{10}$$

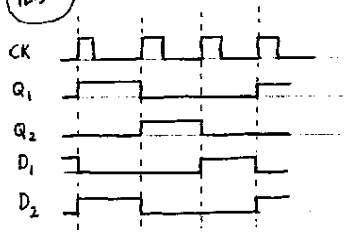
SINCE $A_{16} = 10_{10}$, THE ANSWER IS 60_{10}. NOTING THAT $60_{10} = 3(16) + 12(1)$ AND THAT $12_{10} = C_{16}$, THE ANSWER IN HEX IS 3C. ■

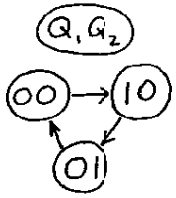
Ex 12.2

N	I_N	Q_{1N}	Q_{2N}	Q_{3N}	Q_{4N}
0	1	0	0	0	0
1	0	1	0	0	0
2	1	0	1	0	0
3	1	1	0	1	0
4	0	1	1	0	1
5	0	0	1	1	0
6	1	0	0	1	1

■

Ex 12.3





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