7.64

B8	B4	B2	B1	Out
0	1	0	0	1
0	1	1	0	1
1	1	0	0	1
1	1	1	0	1

SOP:

$Fr = B_8 B_4 B_2 B_1 + B_8 B_4 B_2 B_1 + B_8 B_4 B_2 B_1 + B_8 B_4 B_2 B_1$

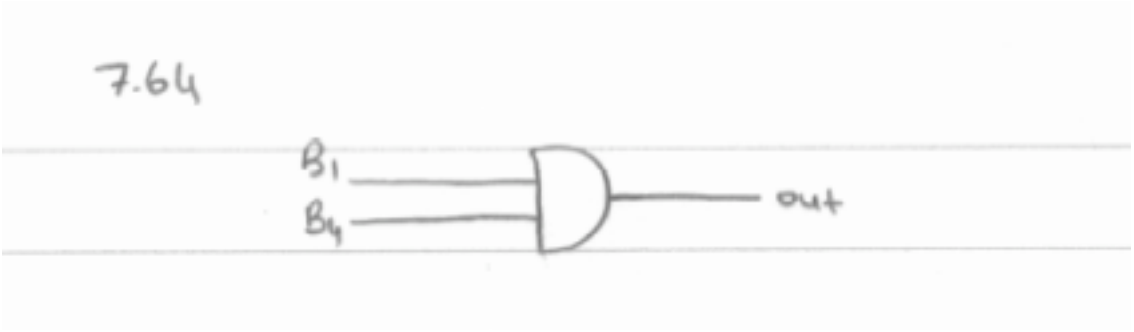
$= B_1 (B_8 B_4 B_2 + B_8 B_4 B_2 + B_8 B_4 B_2 + B_8 B_4 B_2)$

$= B_1 B_4 (B_8 (B_2 + B_2) + B_8 (B_2 + B_2))$

$= B_8 B_4 B_1 + B_8 B_4 B_1$

$= B_4 B_1 (B_8 + B_8)$

$= B_4 B_1$



7.64

I1	I2	S	O1	O2
0	0	0	0	0
0	0	1	0	0
0	1	0	0	1
0	1	1	1	0
1	0	0	1	0
1	0	1	0	1
1	1	0	1	1
1	1	1	1	1

SOP:

For O1;

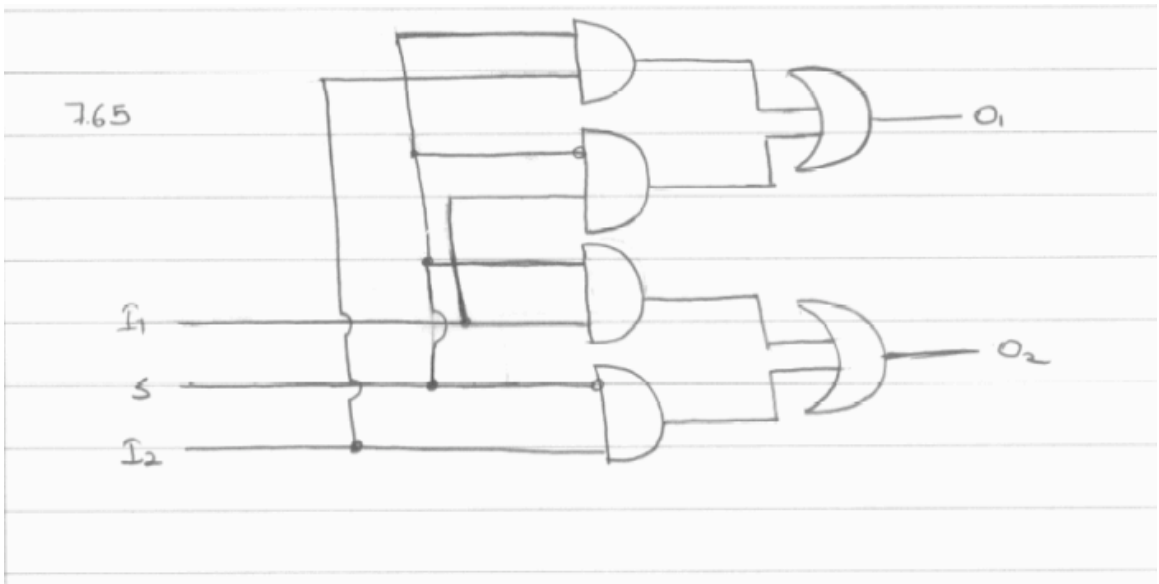
I1I2S+I1I2S+I1I2S+I1I2S=1(O1)

SI2 + SI1=O1

For O2:

I1I2S+ I1I2S+ I1I2S+ I1I2S=1(O2)

SI1+SI2=O2



7.66

SOP:

=ABC+ABC+ABC+ABC

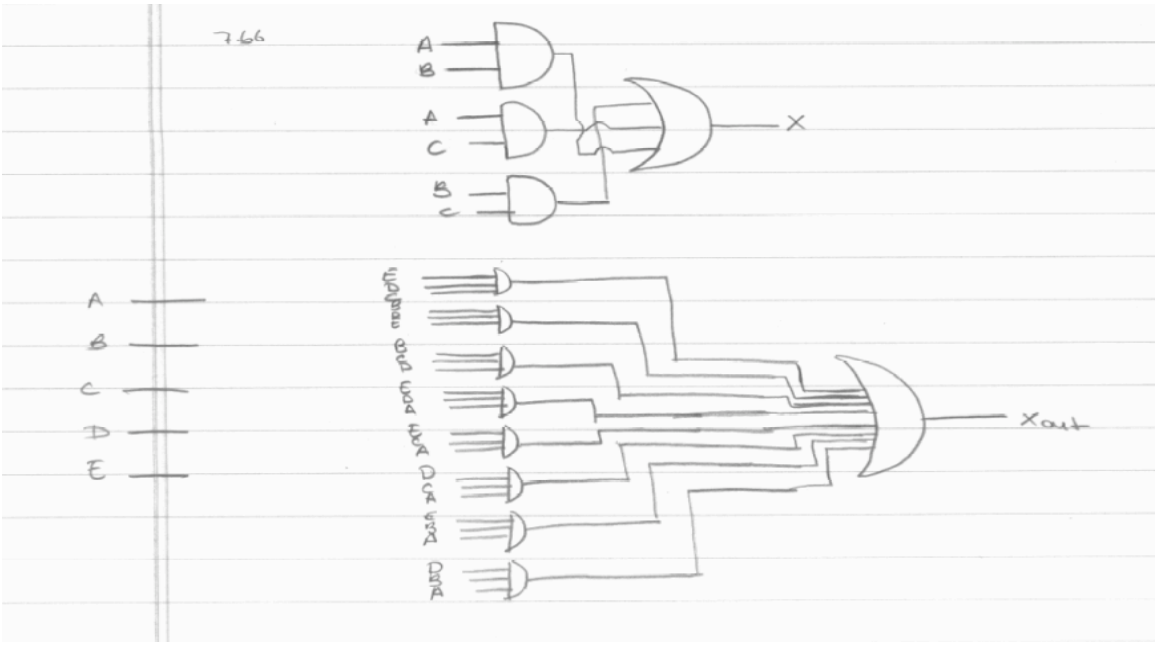
=BC+AC+AB

A	B	C	X ☺
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

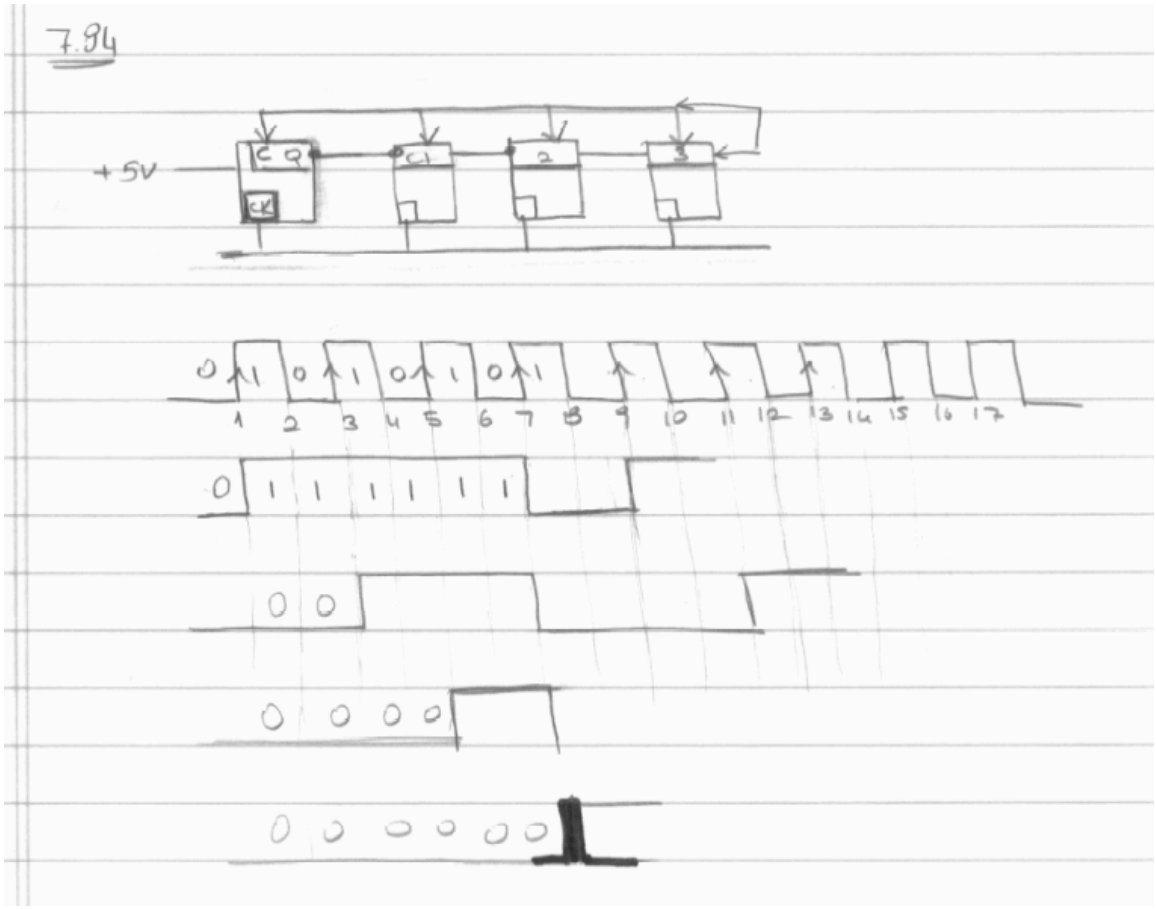
Part 2,

Similar to first part,

X=AB C+ ABD+ABE+ACD+ACE+ADE+BCD+BCE+BDE+CDE



7.84

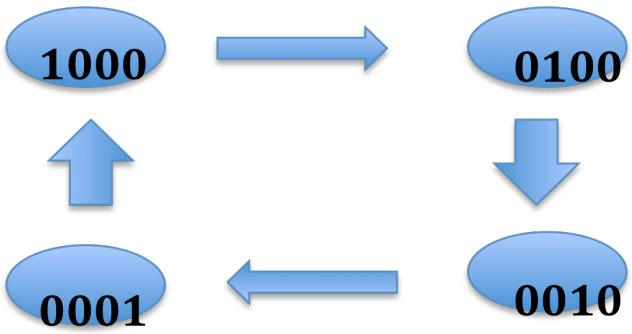

7.84
+5V
Q
CK
1
2
3
0 1 0 1 0 1 0 1
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17
0 1 1 1 1 1 1
0 0
0 0 0 0
0 0 0 0 0 0

12.18

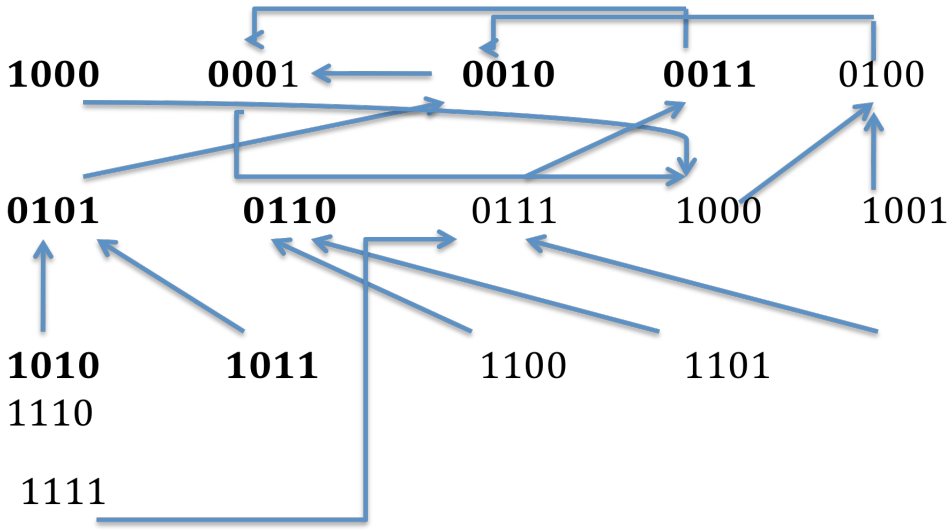
a) Q1=1, Q2=Q3=Q4=0

N	Q1	Q2	Q3	Q4	I
0	1	0	0	0	0
1	0	1	0	0	0
2	0	0	1	0	0
3	0	0	0	1	1
4	1	0	0	0	0

b)



12.19



Limiting Cycle: 1000→0100→0010→0001→1000

12.20.

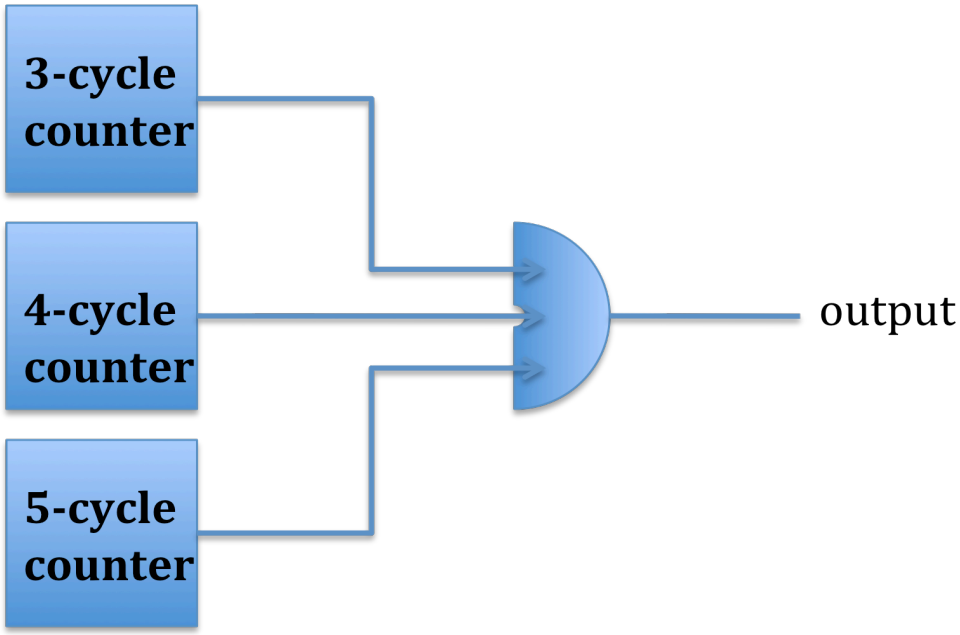
Looking at the state table in #2 and starting w/ when I is 1 (state 0001) we see that I is I after every fourth clock pulse after.

To give an output of 1 after every fifth clock pulse, we can add another fip-flag to the chain.

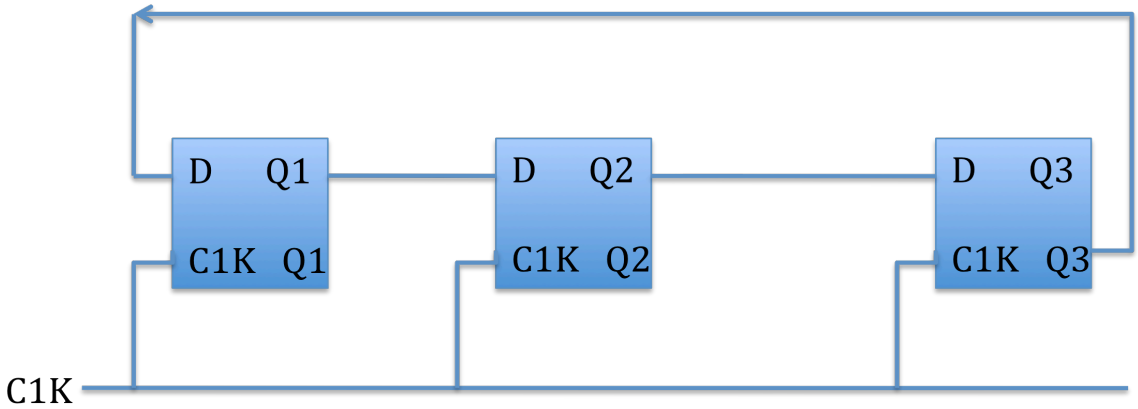
12.21

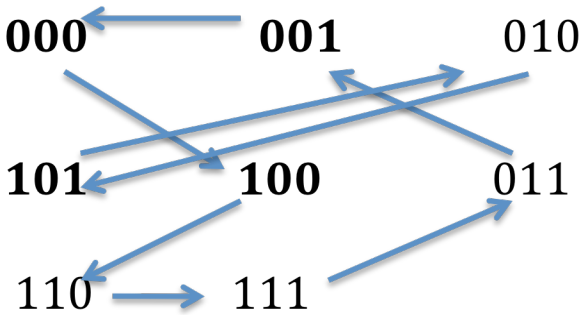
From previous questions, we see that the way to build on n-cycle counter is to have n flip-flops and an n-1 input AND gate. If we want to use less (as stated in this questions) we can use an AND gate to combine the output of 2 or maic counters , such the final output is only high when al the outputs of the counters are high (in other words, a common multiple)

In this case we want the LCM of our counters to be 60. In order to use less than 12 flip-flops, we can have a design like this:



12.22





Cycle 1: 000→100→110→111→011→001→000

Cycle 2:101→010→101

We can use an AND gate to combine Q1, Q2, Q3 => it will only give a 1 when all of them are 1, which is once every 6 cycles according to unit cycle 1.