EE 100/42 Homework 10 Spring 2009

Issued: Friday, April 10, 2009
Due: Friday, April 17, 2009 by 4pm Sharp!

Remember to print the homework cover sheet from the course website, fill it in (name, Lab section, etc) and staple your solution to it.

All problems refer to the fourth edition of the text by Hambley.
Electrical Engineering: Principles and Applications. Prentice Hall, 2008.

Reading Assignment:

Chapter 12 Schwarz & Oldham, ``Electrical Engineering: an Introduction'', Saunders, 2nd edition.

Homework Problems:

7.64 Skip the Karnaugh map part and just draw a logic circuit that solves the problem.
7.65 Skip the Karnaugh map part and just draw a logic circuit that solves the problem.
7.66 Skip the Karnaugh map part and just draw a logic circuit that solves the problem.
7.84

For the following problems, see Page 2 of this document:
12.19 Schwarz & Oldham
12.20 Schwarz & Oldham
12.21 Schwarz & Oldham
12.22 Schwarz & Oldham

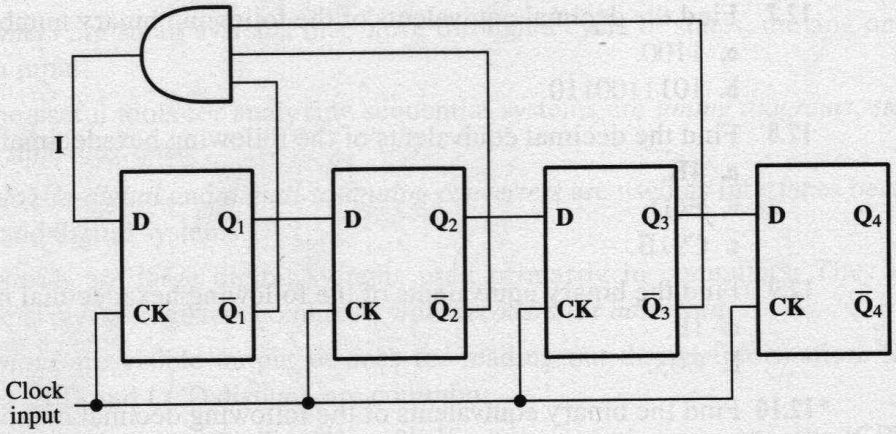

FIGURE 12.24 A 4-bit ring counter.

***12.19** For the system of Fig. 12.24, construct a complete state diagram showing all 16 states of the system. Your diagram should have 16 circles, numbered 0000 through 1111, connected with arrows showing which state each state goes to after one tick of the clock. Interestingly, this system has a *limit cycle:* that is, no matter which state it starts in, it ends up going repetitively through the same sequence of states. Find the limit cycle.

***12.20** The system of Fig. 12.24 is known as a 4-bit *ring counter* because it can be used to give an output of **1** after every fourth clock pulse. Show how it can be used in this way. Can you design a system that gives an output of **1** after every *fifth* clock pulse?

***12.21** We wish to design a system that gives an output of **1** after every 60 input pulses. (This system, which would be called a *divide-by-sixty counter*, could be used in a household clock. It would move a second hand one notch after every 60 cycles of the 60 Hz electric power line.) Design a suitable system using three ring counters. Do not use more than a total of 12 flip-flops.

***12.22** Figure 12.25 shows a 3-bit *Johnson counter*. Construct a complete state diagram showing all eight possible states. Show that the system has two different limit cycles. Show how (with the addition of one gate) it can be used as a divide-by-six counter. (See Problem 12.21.)

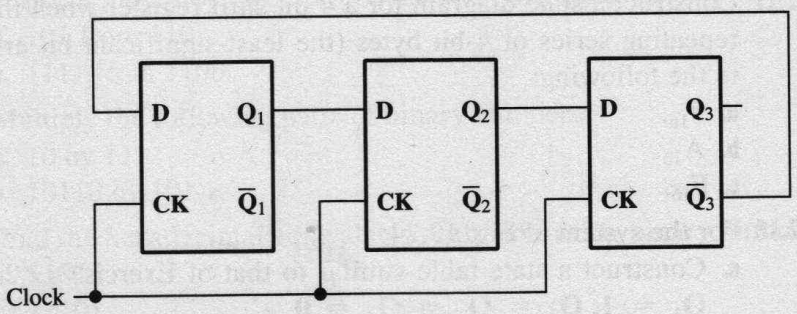

FIGURE 12.25 A 3-bit Johnson counter.