CHAPTER

ONE

KIRCHHOFF'S LAWS

As an electrical engineer, one needs to analyze and design circuits. Electric circuits are present almost everywhere, in home computers, television and hi-fi sets, electric power networks, transcontinental telecommunication systems, etc. Circuits in these applications vary a great deal in nature and in the ways they are analyzed and designed. The purpose of this book is to give an introductory treatment of circuit theory which covers considerable breadth and depth. This differs from a traditional introductory course on circuits, which is restricted to "linear" circuits and covers mainly circuits containing the classical *RLC* elements.

The first chapter deals with the fundamental postulates of lumped-circuit theory, namely, Kirchhoff's laws. Naturally, we need to explain the word "lumped" first. It is also important to understand the concept of "modeling." For example, in circuit theory we first model a "physical circuit" made of electric devices by a "circuit" which is an interconnection of circuit elements. Since Kirchhoff's laws hold for any lumped circuit, the discussion can be dissociated with the electrical properties of circuit elements, which will be treated in the succeeding chapters.

A key concept introduced in this chapter is the representation of a circuit by a graph. This allows us to deal with multiterminal devices in the same way as we would with a conventional two-terminal device. In addition, it enables us to give a formal treatment of Kirchhoff's laws and a related fundamental theorem, Tellegen's theorem.

1 THE DISCIPLINE OF CIRCUIT THEORY

Circuit theory is the fundamental engineering discipline that pervades all electrical engineering. For the present, by *physical circuit* we mean any

interconnection of (physical) *electric devices*. Familiar examples of electric devices are resistors, coils, condensers, diodes, transistors, operational amplifiers (op amps), batteries, transformers, electric motors, electric generators, etc.

The goal of circuit theory is to *predict* the electrical *behavior* of physical circuits. The purpose of these predictions is to improve their design: in particular, to decrease their cost and improve their performance under all conditions of operation (e.g., temperature effects, aging effects, possible fault conditions, etc.).

Circuit theory is an *engineering discipline* whose domain of application is extremely broad. For example, the *size* of the circuits varies enormously: from large-scale integrated circuits which include hundreds of thousands of components and which fit on a fingernail to circuits found in radios, TV sets, electronic instruments, small and large computers, and finally, to telecommunications circuits and power networks that span continents. The *voltages* encountered in the study of circuits vary from the microvolt (μV) [e.g., in noise studies of precision instruments—to megavolts (MV) of power networks]. The *currents* vary from femtoamperes ($1\ \text{fA} = 10^{-15}$ A) [e.g., in electrometers—to megaamperes (MA)] encountered in studies of power networks under fault conditions. The *frequencies* encountered in circuit theory vary from zero frequency [direct current (dc) conditions] to tens of gigahertz ($1\ \text{GHz} = 10^{9}$ Hz) encountered in microwave circuits. The *power levels* vary greatly from 10^{-14} watts (W) for the incoming signal to a sensitive receiver (e.g., faint radio signals from distant galaxies) to electric generators producing $10^{9}\ \text{W} = 1000$ megawatts (MW).

Circuit theory focuses on the *electrical* behavior of circuits. For example, it does not concern itself with thermal, mechanical, or chemical effects. Its aim is to predict and explain the (terminal) *voltages* and (terminal) *currents* measured at the device *terminals*. It does not concern itself with the physical phenomena occurring inside the device (e.g., in a transistor or in a motor). These considerations are covered in device physics courses and in electrical machinery courses.

The goal of circuit theory is to make quantitative and qualitative predictions on the electrical behavior of circuits; consequently the tools of circuit theory will be mathematical, and the *concepts* and *results* pertaining to circuits will be expressed in terms of circuit equations and *circuit variables*, each with an obvious operational interpretation.

2 LUMPED-CIRCUIT APPROXIMATION

Throughout this book we shall consider only *lumped circuits*. For a physical circuit to be considered *lumped*, its physical dimension must be small enough so that, for the problem at hand, electromagnetic waves propagate across the circuit virtually instantaneously. Consider the following two examples:

Example 1 Consider a small computer circuit on a chip whose extent is, say, 1 millimeter (mm); let the shortest signal time of interest be 0.1 nanosecond [$\frac{1}{10}$ of a nanosecond (ns) = 10^{-10} of a second (s)]. Electromagnetic waves travel at the velocity of light, i.e., 3×10^8 meters per second (m/s); to travel 1 mm, the time elapsed is 10^{-3} m/$(3 \times 10^8$ m/s$) = 3.3 \times 10^{-12}$ s = 0.0033 ns. Therefore the propagation time in comparison with the shortest signal time of interest is negligible. More generally, let d be the largest dimension of the circuit, Δt the shortest time of interest, and c the velocity of light. If $d \ll c \cdot \Delta t$, then the circuit may be considered to be lumped.

Example 2 Consider an audio circuit: The highest frequency of interest is, say, $f = 25$ kHz. For electromagnetic waves, this corresponds to a wavelength of $\lambda = c/f = (3 \times 10^8$ m/s$)/(2.5 \times 10^4$ s$^{-1}) = 1.2 \times 10^4$ m = 12 km $\cong$ 7.5 miles. So even if the circuit is spread across a football stadium, the size of the circuit is very small compared to the shortest wavelength of interest λ. More generally, if $d \ll \lambda$, the circuit may be considered to be lumped.

When these conditions are satisfied, electromagnetic theory proves[1] and experiments show that the lumped-circuit approximation holds; namely, throughout the physical circuit the current $i(t)$ through any device terminal and the voltage difference $v(t)$ across any pair of terminals, at any time t, are well-defined. A circuit that satisfies these conditions is called a *lumped circuit.*

From an electromagnetic theory point of view, a lumped circuit reduces to a point since it is based on the approximation that electromagnetic waves propagate through the circuit instantaneously. For this reason, in lumped-circuit theory, the respective locations of the elements of the circuit will not affect the behavior of the circuit. The approximation of a *physical* circuit by a *lumped* circuit is analogous to the modeling of a rigid body as a particle: In doing so, all the data relating to the extent (shape, size, orientation, etc.) of the body are ignored by the theory.

Thus, lumped-circuit theory is related to the more general electromagnetic theory by an approximation (propagation effects are neglected). This is analogous to the relation of classical mechanics to the more exact relativistic mechanics: Classical mechanics delivers excellent predictions provided the velocities are much smaller than the velocity of light. Similarly, when the above conditions hold, lumped-circuit theory delivers excellent predictions of physical circuit behavior.

In situations where lumped approximation is not valid, the physical dimensions of the circuit must be considered. To distinguish such circuits from

[1] R. M. Fano, L. J. Chu, and R. M. Adler, *Electromagnetic Fields, Energy and Forces*, John Wiley and Sons, New York, 1960.

lumped circuits we call them *distributed circuits*. Typical examples of distributed circuits are circuits made of waveguides and transmission lines. In distributed circuits the current and voltage variables would depend not only on time, but also on space variables such as length and width. We need electromagnetic theory for predictions of the behavior of distributed circuits and for analysis and design. In this book we restrict our treatment to lumped circuits.

3 ELECTRIC CIRCUITS, MODELS, AND CIRCUIT ELEMENTS

By *electric device* we mean the physical object in the laboratory or in the factory, for example, the coil, the capacitor, the battery, the diode, the transistor, the motor, etc. *Physical circuits* are obtained by connecting electric devices by wires. Most of the time, these wires will be assumed to be perfectly conducting. We think of these electric devices in terms of *idealized models* like the resistor ($v = Ri$), the inductor ($v = L\, di/dt$), the capacitor ($i = C\, dv/dt$), etc., that you have studied in physics.

Note that these *idealized models* are precisely defined; to distinguish them from electric devices we call them *circuit elements*. It is important to distinguish between a coil made of a fine wire wrapped around a ferrite torus—an *electric device*—and its model as an inductor, or as a resistor in series with an inductor—a *circuit element*, or a combination of circuit elements.

Every model is an approximation. Depending on the application or the problem under consideration, the same physical device may be approximated by several different models. Each of these models is an interconnection of (idealized) circuit elements. For example, we will encounter several different models for the operational amplifier (op amp).[2]

Any *interconnection* of *circuit elements* is called a *circuit*. Thus a circuit is an interconnection of (idealized) models of the corresponding physical devices. The relation between physical circuits and circuits is illustrated in Fig. 3.1. If the (theoretical) predictions based on *analysis* of the circuit do not agree with the measurements, the cause of the disagreement may lie at any step of the process (e.g., erroneous measurement, faulty analysis, etc.). One frequent cause is a poor choice of model, e.g., using a low-frequency model outside of its frequency range of validity, or a linear model outside its amplitude range of validity.

Our subject is circuit theory, consequently we consider the models of the electric devices constituting the physical circuit as given at the outset; our goal is to develop methods to predict the behavior of the circuit. Note that we say "circuit," not "physical circuit": Past experience, however, does give us the

[2] Analogously, in classical mechanics a communications satellite circling the earth may be modeled as a particle, or a rigid body, or an elastic body depending on the problem being studied.

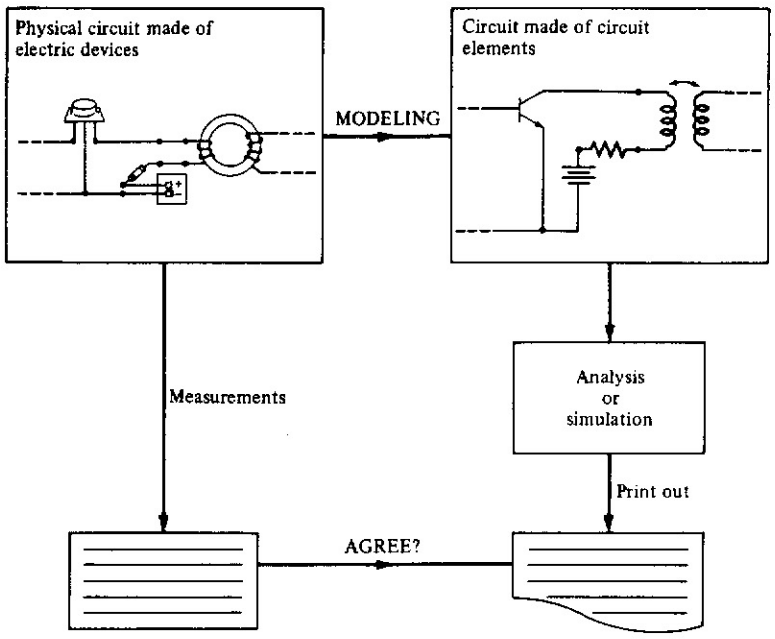

Figure 3.1 Illustration of the relation between physical circuits and circuits, between physical devices and circuit elements, and between laboratory measurements and circuit analysis.

confidence that given any physical circuit we can model it by a circuit which will adequately predict its behavior.

In Fig. 3.2*a* we show a *physical circuit* made up of *electric devices*: a generator, resistor, transistor, battery, transformer, and load. To analyze the physical circuit, we first model it with the circuit shown in Fig. 3.2*b*, which is an interconnection of *circuit elements*: voltage sources, resistors, a capacitor,

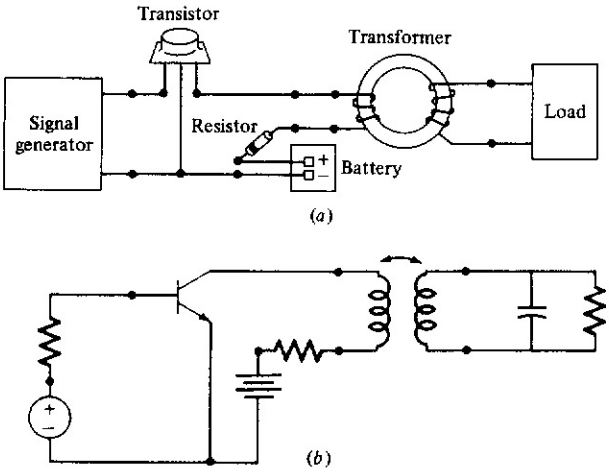

Figure 3.2 (*a*) Physical circuit made of electric devices and (*b*) its circuit model made of circuit elements.

coupled inductors, and a transistor represented by their usual symbols. The electrical properties of some of the two-terminal elements (voltage sources and resistors) will be discussed in Chap. 2, and that of the multiterminal elements (transistor and ideal transformer) will be treated in Chap. 3.

When electric devices are interconnected, we use conducting wires to tie the terminals together as shown in Fig. 3.2*a*. When circuit elements are interconnected, we delete the conducting wires and merge the terminals to obtain the circuit in Fig. 3.2*b*. A *node* is any junction in a circuit where terminals are joined together or any isolated terminal of a circuit element, which is not connected. The circuit in Fig. 3.2*b* has eight nodes (marked with heavy dots). With the introduction of the concept of a node, we are ready to formally treat the subject of interconnection and state the two fundamental postulates of circuit theory, namely, Kirchhoff's voltage law and Kirchhoff's current law.

4 KIRCHHOFF'S LAWS

In lumped circuits, the voltage between any two nodes and the current flowing into any element through a node are well-defined.[3] Since the *actual* direction of current flow and the *actual* polarity of voltage difference in a circuit can *vary* from one instant to another, it is generally impossible to specify in advance the *actual* current direction and voltage polarity in a given circuit. Just as in classical mechanics where it is essential to set up a "frame of reference" from which the actual instantaneous positions of a system of particles can be uniquely specified, so too must we set up an "electrical frame of reference" in a circuit in order that currents and voltages may be *unambiguously* measured.

4.1 Reference Directions

To set up an electrical reference frame, we assign *arbitrarily* a *reference direction* to each current variable by an arrow, and a *reference polarity* to each voltage variable by a pair of plus (+) and minus (−) signs, as illustrated in Fig. 4.1 for two-terminal, three-terminal, and n-terminal elements.[4]

On each terminal lead we indicate an arrow called the *current reference direction*. It plays a crucial role. Consider Fig. 4.1*a*. If at some time t_0, $i_2(t_0) = 2\,\text{A}$, it means that, at time t_0, a current of 2 A flows *out* of the two-terminal element of Fig. 4.1*a* by node ②. If, at some later time t_1,

[3] We assume that the circuit is connected; the definition of "connectedness" will be given later.

[4] An example of a six-terminal element is the filter at the output of an audio amplifier: It directs the high frequencies to the tweeter and the low frequencies to the woofer. (Later we shall see that such a filter may also be viewed as a three-port.)

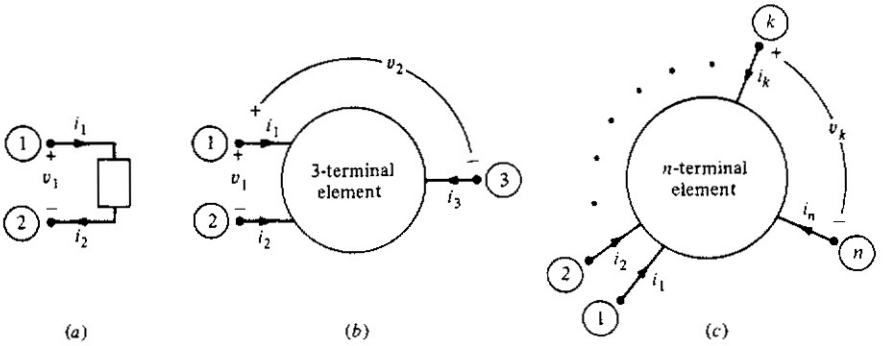

Figure 4.1 Illustration of reference directions using two-, three-, and n-terminal elements.

$i_2(t_1) = -25$ mA, it means that, at time t_1, a current of 25 mA flows *into* the two-terminal element by node ②.

The point is that the current reference direction together with the sign of $i(t)$ determines the actual direction of the flow of electric charges.

On Fig. 4.1 we assign + and − signs to pairs of terminals, e.g., in Fig. 4.1*b* the pair ①, ② and the pair ①, ③. These signs indicate the *voltage reference direction*. Consider Fig. 4.1*a*. If, at some time t_0, $v_1(t_0) = 3$ millivolts (mV), it means that, at time t_0, the electric potential of terminal ① is 3 mV *larger* than the electric potential of terminal ②. Similarly, considering Fig. 4.1*c*, if at time t_1, $v_k(t_1) = -320$ V, it means that the electric potential of terminal ⓚ is, at time t_1, 320 V *smaller* than the electric potential of terminal ⓝ.

Exercise Write down the physical meaning of the following statements in Fig. 4.1*c*: $i_k(t_1) = -2$ mA, $i_2(t_1) = 4$ A, $-v_k(t_1) = 5$ V.

4.2 Kirchhoff's Voltage Law (KVL)

Given any *connected* lumped circuit having n nodes, we may choose (arbitrarily) one of these nodes as a *datum node*, i.e., as a reference for measuring electric potentials. By *connected*, we mean that any node can be reached from any other node in the circuit by traversing a path through the circuit elements. Note that the circuit in Fig. 3.2*b* is not connected. With respect to the chosen datum node, we define $n-1$ *node-to-datum* voltages as shown in Fig. 4.2. Since the circuit is a connected lumped circuit, these $n-1$ node-to-datum voltages are well-defined and, in principle, physically measurable quantities. Henceforth, we shall label them $e_1, e_2, \ldots, e_{n-1}$, and dispense with the + and − signs indicating the voltage reference direction. Note that $e_n = 0$ since node ⓝ is the chosen datum node.

Let v_{k-j} denote the voltage difference between node ⓚ and node ⓙ (see Fig. 4.2). Kirchhoff's voltage law states:

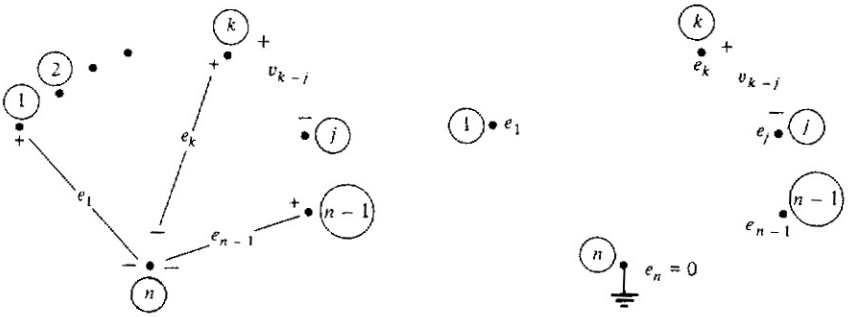

Figure 4.2 Labeling node-to-datum voltages for a circuit with n nodes.

KVL For all lumped connected circuits, for all choices of datum node, for all times t, for all pairs of nodes ⓚ and ⓙ,

$$v_{k-j}(t) = e_k(t) - e_j(t)$$

REMARK Clearly,

$$v_{j-k}(t) = e_j(t) - e_k(t) = -v_{k-j}(t) \tag{4.1}$$

Example The connected circuit in Fig. 4.3 is made of five 2-terminal elements and one 3-terminal element labeled T. There are five nodes, labeled ① through ⑤. Choosing (arbitrarily) node ⑤ as datum, we define the four node-to-datum voltages, e_1, e_2, e_3, and e_4. Therefore by KVL, we may write the following seven equations[5] (for convenience, we drop the dependence on t):

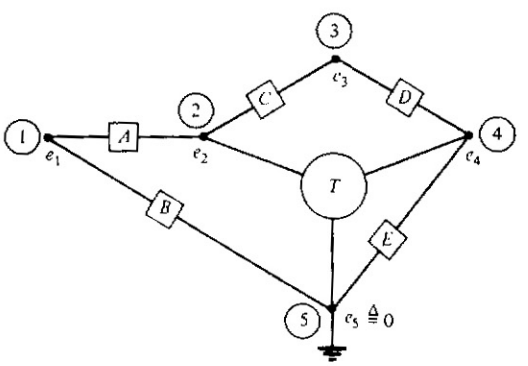

Figure 4.3 A connected circuit with five nodes.

[5] In view of Eq. (4.1) there are altogether two out of five, i.e., $C_2^5 = 10$ nontrivial equations which can be written.

$$
\begin{aligned}
v_{1-5} &= e_1 - e_5 = e_1 \\
v_{1-2} &= e_1 - e_2 \\
v_{2-3} &= e_2 - e_3 \\
v_{3-4} &= e_3 - e_4 \\
v_{4-5} &= e_4 - e_5 = e_4 \\
v_{2-4} &= e_2 - e_4 \\
v_{5-2} &= e_5 - e_2 = -e_2
\end{aligned}
\tag{4.2}
$$

Note that $v_{1\text{-}5}$ and v_{1-2} are the voltages across the two-terminal elements B and A, respectively; v_{2-4}, v_{4-5}, and v_{5-2} are the voltages across the node pairs ②, ④; ④, ⑤; and ⑤, ② of the three-terminal element T, respectively.

If we add the last three equations in (4.2), we find that

$$v_{4-5} + v_{2-4} + v_{5-2} = 0$$

Let us consider the *closed node sequence* ②–④–⑤–②. It is *closed* because the sequence starts and ends at the same node ②. Thus for this particular closed node sequence, the sum of the voltages is equal to zero.

Let us consider a different closed node sequence ①–②–③–④–⑤–①. From the first five equations of (4.2) and using Eq. (4.1), we find that

$$v_{1-2} + v_{2-3} + v_{3-4} + v_{4-5} + v_{5-1} = 0$$

The closed node sequence ①–②–③–④–⑤–① is identified as a *loop* in the circuit, i.e., it is a closed path starting from any node, traversing through *two-terminal elements*, and ending at the same node. The closed node sequence ②–④–⑤–② is not a loop, neither is the closed node sequence ②–③–⑤–②.

Exercise Show that for the closed node sequence ②–③–⑤–② the sum of the voltages, v_{2-3}, v_{3-5}, and v_{5-2} is equal to zero.

We can state KVL in terms of closed node sequences:

> *KVL (closed node sequences)* For all lumped connected circuits, for all closed node sequences, for all times t, the algebraic sum of all node-to-node voltages around the chosen closed node sequence is equal to zero.

Theorem KVL in terms of node voltages is equivalent to KVL in terms of closed node sequences.

PROOF

1. We assume that KVL in terms of node voltages holds. Consider any closed node sequence, say ⓐ–ⓑ–ⓒ–ⓓ–ⓐ, and write the algebraic sum of all voltages around that sequence.

$$v_{a-b} + v_{b-c} + v_{c-d} + v_{d-a}$$

   By KVL in terms of node voltages this sum can be expressed as

$$(e_a - e_b) + (e_b - e_c) + (e_c - e_d) + (e_d - e_a) = 0$$

   so the first statement implies the second.

2. Now assume that KVL in terms of closed node sequences is true. Consider any closed node sequence, say ⓟ–ⓠ–ⓡ–ⓟ then

$$v_{p-q} + v_{q-r} + v_{r-p} = 0 \tag{4.3}$$

   Choosing (arbitrarily) ⓡ as the datum node, we have $v_{q-r} = e_q$ and $v_{r-p} = -e_p$ by definition of the node-to-datum voltages. Therefore from Eq. (4.3), we obtain

$$v_{p-q} = e_p - e_q$$

   So KVL in terms of closed node sequences implies KVL in terms of node voltages. ∎

REMARK For any given connected circuit with n nodes, let us choose (arbitrarily) node ⓝ as the datum node; then the $n-1$ node-to-datum voltages $e_1, e_2, \ldots, e_{n-1}$ specify uniquely and unambiguously the voltage v_{j-k} from any node ⓙ to any other node ⓚ in the circuit. This fact is of crucial importance in circuit theory and is the key concept in node analysis of Chap. 5.

4.3 Kirchhoff's Current Law (KCL)

A fundamental law of physics asserts that electric charge is conserved: There is no known experiment in which a net electric charge is either created or destroyed. Kirchhoff's current law (KCL) expresses this fundamental law in the context of lumped circuits.

To express KCL we shall use gaussian surfaces. A *gaussian surface* is by definition a two-sided "balloon-like" closed surface. Since it is two-sided, it has an "inside" and an "outside." To express the fact that the sum of the charges inside the gaussian surface $\mathcal{S}$ is constant, we shall require that at all times, the algebraic sum of all the currents leaving the surface $\mathcal{S}$ is equal to zero. Let us choose $\mathcal{S}$ so that it cuts only the connecting wires which connect the circuit elements as shown in Fig. 4.4. In the circuit, we have shown a four-terminal element: an operational amplifier, which is connected to the rest of the circuit

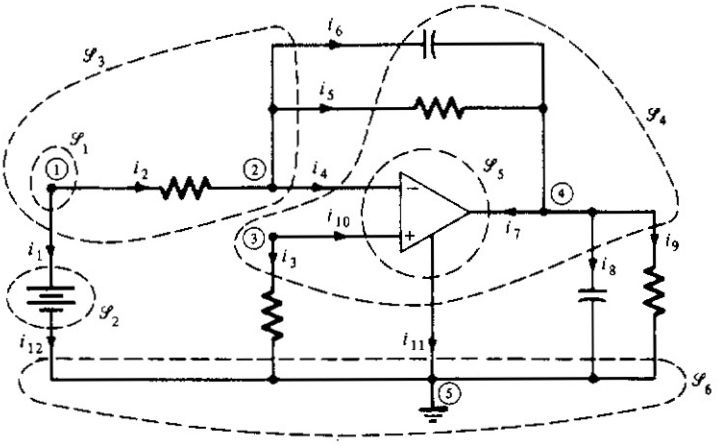

Figure 4.4 An op-amp circuit illustrating gaussian surfaces and KCL.

at nodes ②, ③, ④, and ⑤. The properties of the op amp will be treated in Chap. 4. In the figure we draw six gaussian surfaces: $\mathcal{S}_1, \mathcal{S}_2, \ldots, \mathcal{S}_6$. We will use these surfaces to illustrate Kirchhoff's current law:

> *KCL* For all lumped circuits, for all gaussian surfaces $\mathcal{S}$, for all times t, the algebraic sum of all the currents *leaving* the gaussian surface $\mathcal{S}$ at time t is equal to zero.

For $\mathcal{S}_1$, KCL states:

$$i_1(t) + i_2(t) = 0 \qquad \text{for all } t$$

Note that $\mathcal{S}_1$ contains only node ① in its "inside"; thus a node may be considered as a special case of a gaussian surface, i.e., the surface is shrunk to a point.

For $\mathcal{S}_2$, KCL states:

$$-i_1(t) + i_{12}(t) = 0 \qquad \text{or} \qquad i_1(t) = i_{12}(t)$$

Note that $\mathcal{S}_2$ encloses the two-terminal element, namely, the battery. Thus we make the conclusion that for a *two-terminal element*, the current entering the element from one node at any time t is equal to the current leaving the element from the other node at t.

For $\mathcal{S}_3$, KCL states:

$$i_1(t) + i_4(t) + i_5(t) + i_6(t) = 0$$

For $\mathcal{S}_4$, KCL states:

$$i_3(t) + i_{11}(t) + i_8(t) + i_9(t) - i_6(t) - i_5(t) - i_4(t) = 0$$

For $\mathcal{S}_5$, KCL states:

$$i_{11}(t) - i_{10}(t) - i_4(t) - i_7(t) = 0$$

Note that these are the four currents pertaining to the op amp. Thus choosing a gaussian surface which encloses any n-terminal element, we state that the algebraic sum of the currents leaving or entering the n-terminal element is equal to zero at all times t. This fact will be used in the next section when we discuss n-terminal elements.

For $\mathcal{S}_6$, we have

$$-i_{12}(t) - i_3(t) - i_{11}(t) - i_8(t) - i_9(t) = 0$$

Note that $\mathcal{S}_6$ contains only the datum node ⑤.

We state KCL for nodes:

> *KCL (node law)* For all lumped circuits, for all times t, the algebraic sum of the currents *leaving* any node is equal to zero.

REMARK Although a node is a special case of a gaussian surface, KCL for nodes is far more useful than the general statement in terms of gaussian surfaces. Equations written for nodes from the node law are subsets of the equations written for gaussian surfaces of a given circuit. Yet as we shall see in Sec. 6, KCL equations for nodes lead easily to simple analytic formulation of KCL and are the key idea in the node analysis of Chap. 5.

4.4 Three Important Remarks

1. KVL and KCL are the two fundamental postulates of lumped-circuit theory.
2. KVL and KCL hold irrespective of the *nature* of the elements constituting the circuit. Hence, we may say that Kirchhoff's laws reflect the *interconnection* properties of the circuit.
3. KVL and KCL always lead to *homogeneous linear algebraic* equations with *constant real coefficients*, 0, 1, and -1, if written in the fashion given in this section.

5 FROM CIRCUITS TO GRAPHS

The interconnection properties of a circuit can best be exhibited by way of a graph, called a *circuit graph*. In this section, we will demonstrate how a graph can be obtained from a circuit. The graph retains all the interconnection properties of the circuit but suppresses the information on the circuit elements. Therefore, as far as KVL and KCL are concerned, the circuit graph is all that we need.

A *graph* $\mathcal{G}$ is specified by a set of nodes $\{①, ②, \ldots, ⓝ\}$ together with a set of branches $\{\beta_1, \beta_2, \ldots, \beta_b\}$. If each branch is given an orientation, indicated by an arrow on the branch, we call the graph directed, or, simply, a *digraph*. In Fig. 5.1, we show a connected digraph with five nodes and seven

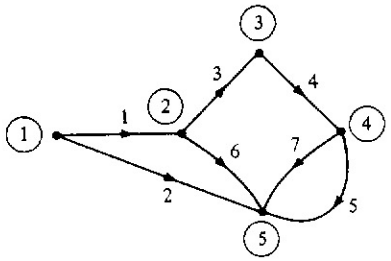

Figure 5.1 A digraph with five nodes and seven branches.

branches, i.e., $n = 5$ and $b = 7$. The *arrows* on the branches are used to denote the reference directions of the currents.

5.1 The Element Graph: Branch Currents, Branch Voltages, and the Associated Reference Directions

A two-terminal element, shown in Fig. 5.2*a*, can be represented by a graph with two nodes and one branch. This graph is called the *element graph* of the two-terminal element. By KCL, the current i flowing from node ① into the element is equal to the current leaving the element by node ②. We therefore represent a two-terminal element by a digraph with the arrow on the branch indicating the reference direction of the current a shown in Fig. 5.2*b*. By doing so we have suppressed the circuit element; and, as such, the current i is called the *branch current* of the two-terminal element.

The voltage across the element is the voltage v between the node-pair ①, ② shown in Fig. 5.2*a*. The voltage v is called the *branch voltage* of the two-terminal element. The reference direction is specified by the + and − signs associated with node-pair ①, ②. Thus the branch voltage $v(t) > 0$ if and only if, at time t, the potential of node ① is larger than that of node ②. Similarly, the branch current $i(t) > 0$ if and only if, at time t, the current enters the element by node ① and leaves it by node ②. When, for the two-terminal elements shown, the current and voltage reference directions are chosen as in Fig. 5.2*a*, we say that we have chosen associated reference directions for that two-terminal element.

More precisely, the *associated reference directions* are defined as follows: Suppose that the voltage reference direction is chosen; then the current

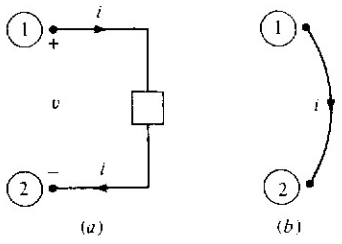

Figure 5.2 (*a*) A two-terminal element and (*b*) its digraph representation.

reference direction is always selected so that the arrow is directed from the + sign toward the − sign through the element. Or, if the reference direction for the current is chosen, the voltage reference direction is specified with the + sign at the node where the current enters the element. This is the convention we will follow throughout, giving us the distinct advantage of not having to mark the signs for the voltage reference direction any more. Therefore in Fig. 5.2*b*, we show only the arrow on the digraph.

Associated reference directions have a very useful property, namely, they make the accounting of power flow quite easy. For the two-terminal element of Fig. 5.2:

$$p(t) \triangleq v(t)i(t) \qquad (5.1)$$
$$= \textit{power} \text{ delivered at time } t \textit{ to} \text{ the two-terminal element } \textit{by} \text{ the remainder of the circuit to which it is connected}$$

If the voltage $v(t)$ is expressed in *volts* and the current in *amperes*, then the power is expressed in *watts*.

Three-terminal elements The digraph representation of two-terminal elements discussed above can be extended to three-terminal elements. For a three-terminal element as shown in Fig. 5.3, there are three node currents i_1, i_2, and i_3, and three voltages v_{1-3}, v_{3-2}, and v_{2-1}. However, from KVL we know that $v_{1-3} + v_{3-2} + v_{2-1} = 0$; and therefore only two voltages can be specified independently. So let us choose arbitrarily node ③ as the datum node and use the node-to-datum voltages for nodes ① and ② as the two independent voltages. Similarly, from KCL, we know that $i_1 + i_2 + i_3 = 0$. Therefore, for the datum node chosen at ③, we use i_1 and i_2 as the two independent currents.

The digraph representation of a three-terminal element with node ③ as datum is shown in Fig. 5.4. Note that it contains *two* branches and three nodes. The arrows indicate the current reference directions for i_1 and i_2. The two currents i_1 and i_2 are called the *branch currents* of the three-terminal element. Using the associated reference directions for the voltages, we redraw the three-terminal element as shown in Fig. 5.5 and define $v_1 = v_{1-3}$ and $v_2 = v_{2-3}$

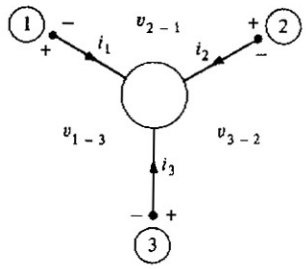

Figure 5.3 A three-terminal element.

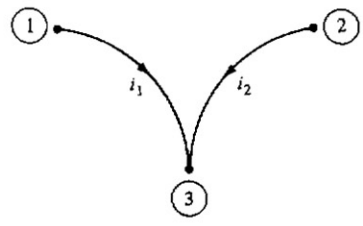

Figure 5.4 The digraph representation of a three-terminal element with node ③ chosen as datum.

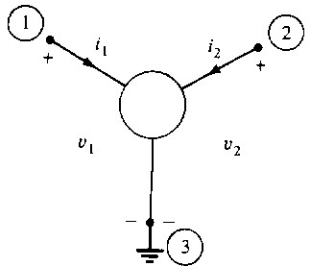

Figure 5.5 A three-terminal element with branch currents i_1, i_2 and branch voltages, v_1, v_2 using associated reference directions.

as the two *branch voltages* of the three-terminal element. Thus by using the digraph representation, we have extended the *circuit variables*: branch voltages and branch currents from two-terminal elements to three-terminal elements.

Obviously, for a three-terminal element, there exist altogether three possible digraph representations depending on which node is chosen as the datum node. In addition to the digraph in Fig. 5.4 we have two other digraphs as shown in Fig. 5.6.

***n*-Terminal elements** We can easily generalize the above to n-terminal elements as shown in Fig. 5.7. Thus for an n-terminal element, we have an

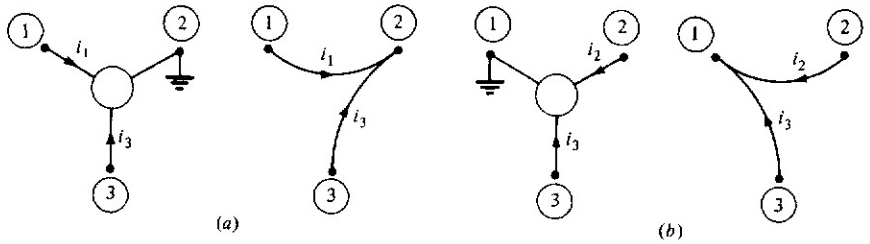

Figure 5.6 Other digraph representations of a three-terminal element: (*a*) Datum node, ②; (*b*) datum node, ①.

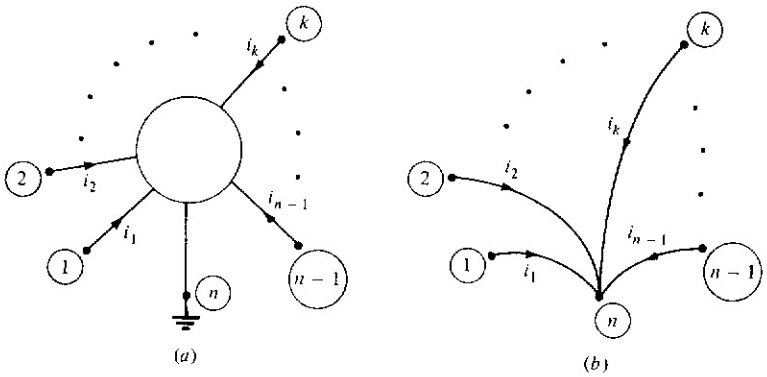

Figure 5.7 An n-terminal element and its element graph with node ⓝ as datum node.

element graph with $n-1$ branches and n nodes. There are $n-1$ branch currents and $n-1$ branch voltages; and we always use the associated reference directions and choose the current reference directions as shown, i.e., with arrows entering the element at the nodes. The *power* delivered to the element from the outside to the element at time t is therefore

$$p(t) = \sum_{k=1}^{n-1} v_k(t) i_k(t) \tag{5.2}$$

5.2 The Circuit Graph: Digraph

For a given circuit, if we replace each element by its element graph, the result is a directed *circuit graph*, or simply a *digraph*.

For example, a digraph associated with the circuit in Fig. 4.3 is the one shown in Fig. 5.1. We may now use the digraph instead of the circuit to write equations of KVL and KCL. It is interesting to note that since the circuit contains a three-terminal element, the digraph bears little resemblance to the circuit. In fact, given the digraph, without specifying which nodes belong to the three-terminal element, it is not possible to reconstruct the circuit. This observation is not true if the circuit contains only two-terminal elements.

Exercise 1 Demonstrate that the op-amp circuit in Fig. 4.4 has its associated digraph shown in Fig. 5.8 if node ⑤ is chosen as the datum node for the op amp.

Note that in the circuit there are seven two-terminal elements and one four-terminal element. The total number of branches in the digraph is equal to $7+(4-1)=10$. (Remember for an n-terminal element, the element graph has $n-1$ branches.)

Exercise 2 Choosing note ⑤ as the datum node for the circuit, show by KVL that one can express all 10 branch voltages $v_1, v_2, \ldots, v_{10}$ in terms of

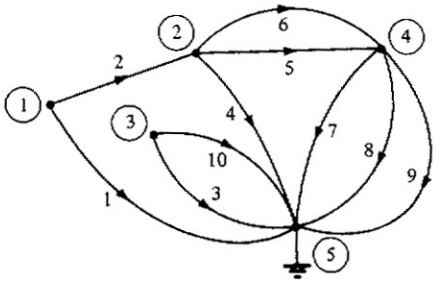

Figure 5.8 Digraph associated with the circuit in Fig. 4.4. The branches are numbered according to the corresponding currents in Fig. 4.4.

the four node-to-datum voltages e_1, e_2, e_3, and e_4 as follows:

$$\begin{aligned} v_1 &= e_1 \\ v_2 &= e_1 - e_2 \\ v_3 &= e_3 \\ v_4 &= e_2 \\ v_5 &= e_2 - e_4 \\ v_6 &= e_2 - e_4 \\ v_7 &= e_4 \\ v_8 &= e_4 \\ v_9 &= e_4 \\ v_{10} &= e_3 \end{aligned} \tag{5.3}$$

Exercise 3 Show that KCL equations written for the four nodes ① to ④ are

$$\begin{aligned} i_1 + i_2 &= 0 \\ -i_2 + i_4 + i_5 + i_6 &= 0 \\ i_3 + i_{10} &= 0 \\ -i_5 - i_6 + i_7 + i_8 + i_9 &= 0 \end{aligned} \tag{5.4}$$

Exercise 4 Express Eqs. (5.3) and (5.4) in matrix form using the vectors $\mathbf{v}$, $\mathbf{e}$, and $\mathbf{i}$, e.g., $\mathbf{v} = [\mathbf{v}_1, \mathbf{v}_2, \ldots, \mathbf{v}_{10}]^T$, where the superscript T denotes matrix transposition.

REMARK The fundamental concept of using a circuit graph instead of the circuit itself in writing KVL and KCL equations is the following:

1. We convert circuit elements whether two-terminal, three-terminal, or n-terminal into *branches*, thus we were able to define *branch voltages* and *branch currents* for any element in a circuit.
2. With a circuit graph we can define precisely the interconnection properties of a circuit using the branch-node incidence relation of a graph to be discussed in Sec. 6.

Exercise 5 Show that if branch 3 in Fig. 4.4 is replaced by a short circuit thereby coalescing nodes ③ and ⑤ into one node, then the digraph in Fig. 5.8 will contain a *self-loop*, i.e., a loop made of one branch and one node.

5.3 Two-Ports, Multiports, and Hinged Graphs

Up to now we have assumed that the circuit is connected. In Fig. 3.2*b* the circuit, because of the presence of a two-winding transformer, is not connected. It turns out that we can easily take care of the situation; but before we do so, we need to introduce a special class of four-terminal elements called two-ports. A *two-port* is a circuit element or a circuit with two *pairs* of *accessible* terminals. Thus a two-port may contain many circuit elements.

Two-ports In many engineering situations the terminals of a multiterminal device are naturally associated in pairs: For example, in a hi-fi chain the input pair is connected, say, to a microphone and the output pair to a loudspeaker system. These pairs of associated terminals are called *ports*. Another example is a two-winding transformer: The two input terminals constitute a natural *input port* and the two output terminals constitute a natural *output port*. In either case, the typical connections to the four-terminal element have the form shown in Fig. 5.9. Note the labeling of the nodes and the currents: the input pair is ①, ①′ and the output pair is ②, ②′.

When we view the four-terminal element of Fig. 5.9 as a *two-port*, we consider *only* the voltages v_1 and v_2 and the four terminal currents i_1, i_1', i_2, i_2'. Naturally, v_k is called the *port voltage* at port ⓚ, $k = 1, 2$. Now the gaussian surfaces $\mathcal{S}_1$ and $\mathcal{S}_2$ shown in Fig. 5.9 and KCL impose the two current constraints:

$$i_1 = i_1' \qquad \text{and} \qquad i_2 = i_2'$$

The point is that these two port constraints reduce the number of current variables from four to two: i_1 and i_2. The current i_k is called the *port current* at port ⓚ.

Note that at each port the port voltage v_k and the port current i_k have associated reference directions: Hence $v_k(t)i_k(t)$ is the power entering port k at time t. For example, the power delivered at time t, *by* the remainder of the circuit *to* the two-port of Fig. 5.9 is given by

$$v_1(t)i_1(t) + v_2(t)i_2(t)$$

Naturally, a two-terminal element may be viewed as a one-port. Thus, in generalizing the digraph representation from a one-port to a two-port, we use two branches and four nodes for its element graph as shown in Fig. 5.10.

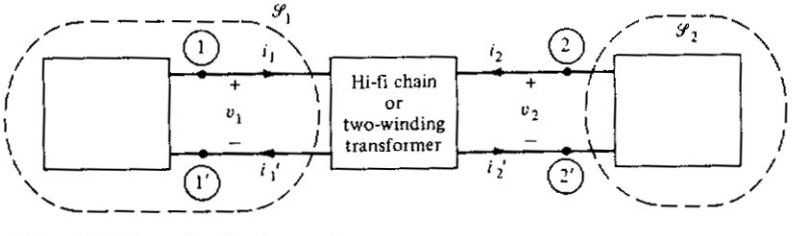

Figure 5.9 Example of a two-port.

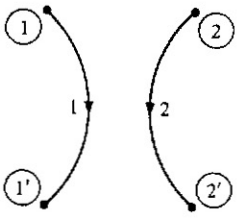

Figure 5.10 The element graph of a two-port.

Therefore the port voltages v_1 and v_2 are also referred to as the branch voltages of the two-port. Similarly, we can also call the port currents i_1 and i_2 the branch currents of the two-port. This is in contrast to a four-terminal element where there are three branches in its element graph, thus three branch voltages and three branch currents.

Multiports We can generalize the concept of two-ports to multiports. For example, a three-winding transformer is a three-port as shown in Fig. 5.11. Its element graph has three branches and six nodes as shown in Fig. 5.11*c*. The three branch voltages and three branch currents are the port voltages and port currents, respectively, for the three-port.

Hinged graphs The element graph of a two-port consists of two branches which are not connected. It signifies that the port voltages or port currents at different ports are not related because of connections but rather are *coupled* because of physical phenomena within the element. For example, the trans-

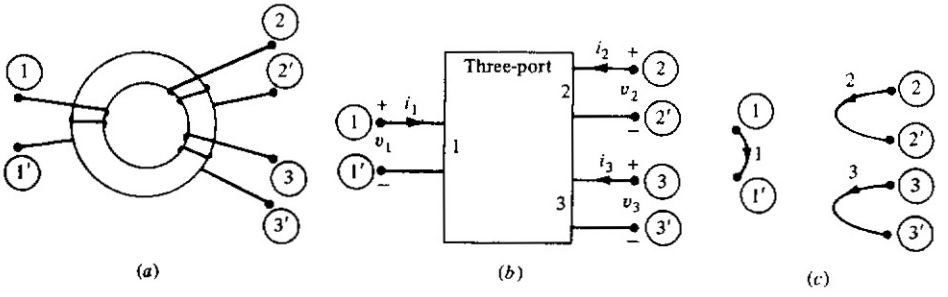

Figure 5.11 (*a*) A three-winding transformer. (*b*) the corresponding three-port, and (*c*) its element graph.

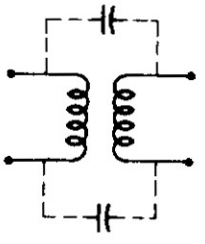

Figure 5.12 A model of a physical transformer which includes two parasitic capacitors.

former port voltages are coupled magnetically via the flux linkages among the various windings. Therefore circuits containing two-ports or multiports have circuit graphs which are often unconnected.[6]

To avoid an "unconnected" circuit graph, we can tie together the two separate ports of a circuit graph at two arbitrary nodes by a branch. This is illustrated in Fig. 5.13*a*, where nodes ③ and ⑤ are tied together by a branch k. This connection does not change any branch voltage or current in the original circuit. This is easily seen because, by using KCL with a gaussian surface which encloses one of the separate parts of the graph and which cuts branch k, the current i_k is zero. If $i_k = 0$, it amounts to an open circuit or no connection; thus we have not changed the behavior of the circuit. Next, since voltages are measured between nodes, we choose a datum node for each separate part. If we choose nodes ③ and ⑤ as the datum nodes for the separate parts, we may "solder" together node ③ and node ⑤ as shown in Fig. 5.13*b* to make them the common datum. The graph so obtained is called a *hinged graph*. With the introduction of the concept of a hinged graph, we have generalized our treatment so far to include two-ports and multiports, that is, we can always assume without loss of generality that any lumped circuit and its circuit graph are *connected*.

"Grounded" two-ports If a common connection exists between nodes ① and ② of a two-port as shown by the low-pass filter in Fig. 5.14*a*, we call it, by tradition, a "*grounded*" *two-port*. The word "grounded" does not necessarily mean that the node is always set to zero potential. Rather, a "grounded" two-port is essentially a three-terminal element with its datum node specified as the common node of the two-port. Obviously, the element graph for a "grounded" two-port consists of two branches which are tied together at the common node shown in Fig. 5.14*b*.

Similarly, an n-terminal element can be viewed as a "grounded" $(n-1)$-port if the datum is specified.

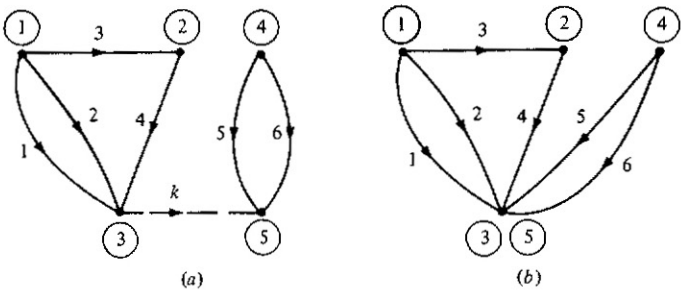

Figure 5.13 (*a*) Connecting nodes ③ and ⑤ by a branch k. (*b*) Soldering together nodes ③ and ⑤ to obtain a hinged graph.

[6] An exception to this is, for example, in modeling a physical transformer; we may need to use additional elements to tie the windings together as shown in Fig. 5.12.

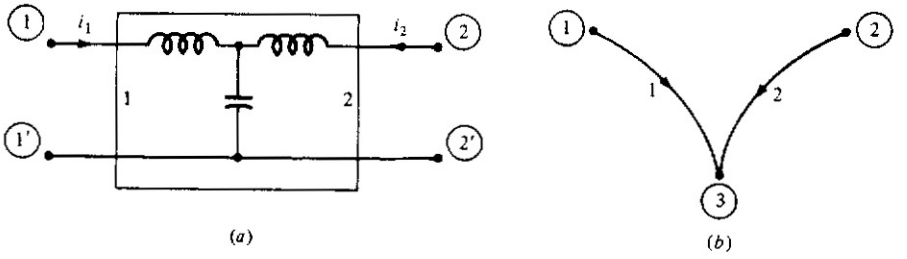

Figure 5.14 (*a*) A "grounded" two-port and (*b*) its element graph.

5.4 Cut Sets and KCL

A very useful graph-theoretic concept is the cut set. Given a *connected* digraph $\mathcal{G}$, a set of branches $\mathcal{C}$ of $\mathcal{G}$ is called a *cut set* iff[7] (*a*) the removal of all the branches of the cut set results in an *unconnected digraph*, which means that the resulting digraph is no longer connected, and (*b*) the removal of all but any one branch of $\mathcal{C}$ leaves the digraph *connected*. Stated in another way, (*b*) implies that if any branch in the set is left intact, the digraph remains connected.

For the digraph of Fig. 5.15, $\mathcal{C}_1 = \{\beta_1, \beta_3\}$, $\mathcal{C}_2 = \{\beta_4, \beta_5, \beta_6\}$, and $\mathcal{C}_3 = \{\beta_4, \beta_5, \beta_7\}$ form cut sets. Here, β_k denotes "branch k."

Exercise Refer to Fig. 5.15.
(*a*) Is $\{\beta_1, \beta_3, \beta_4, \beta_5, \beta_6\}$ a cut set?
(*b*) List all cut sets of the digraph shown in Fig. 5.15.

REMARKS
1. Any cut set creates a partition of the set of nodes in the graph into two subsets.
2. To any cut set corresponds a gaussian surface which cuts precisely the same branches.
3. Similarly, to any gaussian surface corresponds *either* one cut set *or* a union of cut sets (see $\mathcal{S}_1$ in Fig. 5.15).
4. To each cut set we can define arbitrarily a *reference direction*, as shown by the arrows attached to the cut sets in Fig. 5.15.

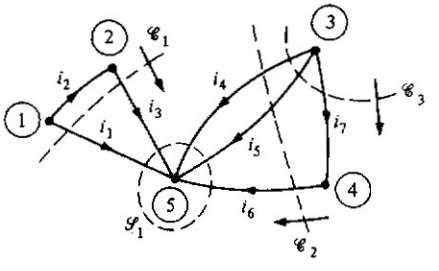

Figure 5.15 Digraph illustrating cut sets.

[7] "iff" means "if and only if."

KCL (cut-set law) For all lumped circuits, for all time t, the algebraic sum of the currents associated with any cut set is equal to zero.

Example For the digraph shown in Fig. 5.16, the cut set $\mathscr{C} = \{\beta_1, \beta_2, \beta_3\}$ is indicated by the dashed line cutting through these branches. Let us assign a reference direction to $\mathscr{C}$ as shown by the arrow; then the KCL applied to $\mathscr{C}$ gives

$$i_1(t) + i_2(t) - i_3(t) = 0$$

The $-i_3$ comes about because the reference direction of i_3 disagrees with the reference direction of the cut set $\mathscr{C}$.

By now we have learned three forms of KCL, namely, in terms of (1) gaussian surfaces, (2) nodes, and (3) cut sets.

KCL theorem The three forms of the KCL are equivalent. Symbolically,[8]

$$\left(\begin{matrix}\text{KCL} \\ \text{gaussian surface}\end{matrix}\right) \Leftrightarrow \left(\begin{matrix}\text{KCL} \\ \text{node law}\end{matrix}\right) \Leftrightarrow \left(\begin{matrix}\text{KCL} \\ \text{cut sets}\end{matrix}\right)$$

PROOF

(1) $\Rightarrow$ (2) Simply use a gaussian surface that surrounds only the node in question. For example, consider node ⑤ in Fig. 5.15: For gaussian surface $\mathscr{S}_1$, KCL applied to $\mathscr{S}_1$ is identical with KCL applied to node ⑤, namely,

$$-i_1 - i_3 - i_4 - i_5 - i_6 = 0$$

(2) $\Rightarrow$ (3) Any cut set partitions the set of nodes into two subsets. Writing the KCL equation for each node in such a subset and adding the results, we obtain the cut-set equation, except for maybe a -1 factor. For example, consider the cut set $\mathscr{C}_2$ in Fig. 5.15: If we

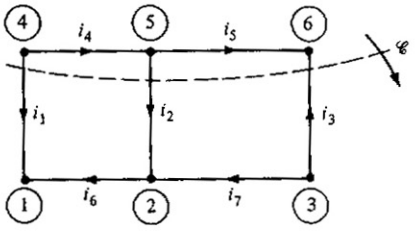

Figure 5.16 Digraph illustrating the reference direction of a cut set.

[8] $\Rightarrow$ means "implies"; $\Leftarrow$ means "is implied by"; $\Leftrightarrow$ means "is equivalent to."

add the KCL equations applied to nodes ③ and ④, we obtain

$$i_4 + i_5 + i_6 = 0$$

(note that i_7 cancels out in the addition!), which is the cut-set equation for $\mathscr{C}_2$.

(3)⇒(1) It is easy to demonstrate that the set of branches cut by a gaussian surface is either a cut set or a disjoint union of cut sets. So given any gaussian surface, let us write the KCL equation for each of these cut sets; then adding or subtracting these equations, we obtain the KCL equation for the gaussian surface. For example, consider gaussian surface $\mathscr{S}_1$ of Fig. 5.15. It is the union of cut set $\{\beta_1, \beta_3\}$ and cut set $\{\beta_4, \beta_5, \beta_6\}$ whose equations are, respectively,

$$-i_1 - i_3 = 0$$

$$+i_4 + i_5 + i_6 = 0$$

Subtracting the second equation from the first gives

$$-i_1 - i_3 - i_4 - i_5 - i_6 = 0$$

which is the KCL equation for gaussian surface $\mathscr{S}_1$. ∎

6 MATRIX FORMULATION OF KIRCHHOFF'S LAWS

6.1 Linear Independence

Consider a set of m linear algebraic equations in n unknowns: For $j = 1, 2, \ldots, m$

$$f_j(x_1, x_2, \ldots, x_n) = \alpha_{j1}x_1 + \alpha_{j2}x_2 + \cdots + \alpha_{jn}x_n = 0 \qquad (6.1)$$

where the α_{jk}'s are real or complex numbers. It is important to decide whether or not each equation brings new information not contained in the others; equivalently, it is important to decide whether the equations are linearly independent. These m equations are said to be *linearly dependent* iff there are constants $k_1, k_2, \ldots, k_m$ and *not all zero* such that

$$\sum_{j=1}^{m} k_j f_j(x_1, x_2, \ldots, x_n) = 0 \qquad \text{for all } x_1, x_2, \ldots, x_n \qquad (6.2)$$

Clearly if these m equations are linearly dependent, then at least one equation may be written as a linear combination of the others; in other words, that equation repeats the information contained in the others!

It is crucial to note that the left-hand side of Eq. (6.2) must be zero *for all* values of $x_1, x_2, \ldots, x_n$.

Example Consider an example where $m = 3$ and $n = 4$:

$$\begin{aligned} x_1 - x_2 + x_3 + 3x_4 &= 0 \\ 2x_1 + 3x_2 - x_3 - 4x_4 &= 0 \\ -4x_1 - 11x_2 + 5x_3 + 18x_4 &= 0 \end{aligned}$$

Direct calculation shows that with $k_1 = 2$, $k_2 = -3$, and $k_3 = -1$ the condition for Eq. (6.2) holds; in other words, these three equations are linearly dependent.

The set of m linear algebraic equations (6.1) is said to be *linearly independent* iff it is not linearly dependent.

In practice, we use gaussian elimination to decide whether or not a given set of linear equations is linearly dependent.

6.2 Independent KCL Equations

For a given circuit, we can write many KCL equations by the node law, the cut-set law, or using gaussian surfaces. How many of them are linearly independent and how to write a complete set that contains all the necessary information as far as KCL is concerned are the subjects of this subsection. We will give a systematic treatment by means of the digraph of the circuit under consideration: in particular, a list of nodes, a list of branches, and for each branch the specification of the node it leaves and of the node it enters. This is done by the *incidence matrix* $\mathbf{A}_a$ of the digraph.

Let digraph $\mathcal{G}$ have n nodes and b branches, then $\mathbf{A}_a$ has n rows—one row to each node—and b columns—one column to each branch. To see how the matrix is built up consider the four-node six-branch digraph shown in Fig. 6.1. Let us write the KCL equations for each node:

$$\begin{aligned} i_1 + i_2 \qquad\qquad - i_6 &= 0 \\ -i_1 \quad - i_3 + i_4 \qquad\quad &= 0 \\ - i_2 + i_3 \quad + i_5 \quad &= 0 \\ - i_4 - i_5 + i_6 &= 0 \end{aligned} \tag{6.3}$$

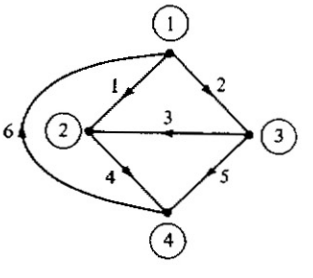

Figure 6.1 A digraph with four nodes and six branches.

In matrix form it reads

$$\begin{matrix} ①\rightarrow \\ ②\rightarrow \\ ③\rightarrow \\ ④\rightarrow \end{matrix}\begin{bmatrix} 1 & 1 & 0 & 0 & 0 & -1 \\ -1 & 0 & -1 & 1 & 0 & 0 \\ 0 & -1 & 1 & 0 & 1 & 0 \\ 0 & 0 & 0 & -1 & -1 & 1 \end{bmatrix}\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \\ i_5 \\ i_6 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{6.4}$$

branch 1 branch 6

The 4×6 matrix just obtained is called the *incidence matrix* $\mathbf{A}_a$ of $\mathcal{G}$.

Exercise

(*a*) Demonstrate that the four equations in (6.3) are linearly dependent.
(*b*) Demonstrate that any three of the four equations in (6.3) are linearly independent.

In general, for an n-node b-branch *connected* digraph $\mathcal{G}$ which does *not* contain *self-loops*[9] the matrix $\mathbf{A}_a$ is specified as follows: For $i = 1, 2, \ldots, n$ and $k = 1, 2, \ldots, b$

$$a_{ik} = \begin{cases} +1 \text{ if branch } k \textit{ leaves} \text{ node } ⓘ \\ -1 \text{ if branch } k \textit{ enters} \text{ node } ⓘ \\ 0 \text{ if branch } k \text{ does not touch node } ⓘ \end{cases} \tag{6.5}$$

and the n node equations of $\mathcal{G}$ read

$$\mathbf{A}_a\mathbf{i} = \mathbf{0} \tag{6.6}$$

where $\mathbf{i} = (i_1, i_2, \ldots, i_b)^T$ is called the *branch current vector*.

REMARK Each column of $\mathbf{A}_a$ has precisely a single $+1$ and a single -1; consequently, if we add together the n equations in (6.6), all the variables $i_1, i_2, \ldots, i_b$ cancel out; equivalently the n KCL equations are linearly dependent.

Suppose that for the *connected* digraph $\mathcal{G}$ we choose a datum node and we throw away the corresponding KCL equation, then the remaining $n-1$ equations are linearly independent. Since this is important we state it formally:

Independence property of KCL equations For any *connected* digraph $\mathcal{G}$ with n nodes, the KCL equations for *any* $n-1$ of these nodes form a set of $n-1$ *linearly independent equations*.

[9] The digraph of circuits containing multiterminal elements will contain *self-loops* whenever one or more terminals are connected to the datum, as in the last exercise of Sec. 5.2.

PROOF We prove it by contradiction. Suppose that the first k of these $n-1$ equations are *linearly dependent*. More precisely, there are k real constants $\gamma_1, \gamma_2, \ldots, \gamma_k$, *not all zero*, such that

$$\sum_{j=1}^{k} \gamma_j f_j(i_1, i_2, \ldots, i_n) = 0 \qquad \text{for all } i_1, i_2, \ldots, i_n \tag{6.7}$$

Without loss of generality, we may assume that $\gamma_j \neq 0$ for $j = 1, 2, \ldots, k$, i.e., there are exactly k equations in the sum of Eq. (6.7).

Consider the two sets of nodes in $\mathcal{G}$, namely, the set which corresponds to the k equations and that of the remaining nodes. Since the digraph is connected, there is at least one branch which connects a node in the first set to a node in the second set. Clearly the current in that branch appears only *once* in the first k node equations, hence that current cannot cancel out in the sum of Eq. (6.7). This contradiction shows that for any $k \leq n-1$ it is not the case that a subset of k of the KCL equations is linearly dependent. That is, these $n-1$ equations are linearly independent. ■

If in $\mathbf{A}_a$, the incidence matrix of the connected digraph $\mathcal{G}$, we delete the row corresponding to the datum node, we obtain the *reduced incidence matrix* $\mathbf{A}$ which is of dimension $(n-1) \times b$. The corresponding KCL equations read

$$\mathbf{Ai} = \mathbf{0} \tag{6.8}$$

As a consequence of the independence property just proved, we may state that the $(n-1) \times b$ matrix $\mathbf{A}$ is full rank, i.e., its $n-1$ rows are linearly independent vectors in the b-dimensional space. Stated in another way, (6.8) consists of $n-1$ linearly independent KCL equations.

6.3 Independent KVL Equations

Similarly, to write a set of complete linearly independent KVL equations in a systematic way is of crucial importance. Let us write KVL for the four-node six-branch digraph of Fig. 6.1. Using *associated reference directions* and choosing node ④ as the datum node, we obtain

$$\begin{aligned}
v_1 &= e_1 - e_2 \\
v_2 &= e_1 \qquad - e_3 \\
v_3 &= \qquad - e_2 + e_3 \\
v_4 &= \qquad e_2 \\
v_5 &= \qquad\qquad e_3 \\
v_6 &= -e_1
\end{aligned} \tag{6.9}$$

or in matrix form

$$\mathbf{v} = \mathbf{Me} \tag{6.10}$$

where $\mathbf{v} = (v_1, v_2, \ldots, v_b)^T$ is the *branch voltage vector*, $\mathbf{e} = (e_1, e_2, \ldots, e_{n-1})^T$ is the *node-to-datum voltage vector*, and $\mathbf{M}$ is a $b \times (n-1)$ matrix. Thinking in terms of KVL, we see that for $k = 1, 2, \ldots, b$ and $i = 1, 2, \ldots, n-1$

$$m_{ki} = \begin{cases} +1 \text{ if branch } k \textit{ leaves} \text{ node } \textcircled{i} \\ -1 \text{ if branch } k \textit{ enters} \text{ node } \textcircled{i} \\ \ \ 0 \text{ if branch } k \text{ does not touch node } \textcircled{i} \end{cases} \tag{6.11}$$

Comparing Eq. (6.11) with (6.5), we conclude that

$$\mathbf{M} = \mathbf{A}^T$$

and more usefully, KVL is expressed by the equation

$$\mathbf{v} = \mathbf{A}^T\mathbf{e} \tag{6.12}$$

With a *connected* digraph $\mathcal{G}$ $\mathbf{A}$ has $n-1$ linearly independent rows, and consequently $\mathbf{A}^T$ has $n-1$ linearly independent columns.

REMARKS

1. Note that, in the digraph, (*a*) we choose current reference directions, (*b*) we choose a datum node and define the reduced incidence matrix $\mathbf{A}$, (*c*) we write KCL as $\mathbf{Ai} = \mathbf{0}$, (*d*) then we use associated reference directions to find that KVL reads $\mathbf{v} = \mathbf{A}^T\mathbf{e}$. Thus whenever we invoke this last equation, we automatically use associated reference directions for the branch voltages. We also assume the same datum node is used in writing KCL and KVL.
2. When we deal with digraphs which are not connected, we could either use the concept of the hinged graph to make the digraph connected or treat each separate part independently. In the latter, each separate part will have its own incidence matrix and datum node.

7 TELLEGEN'S THEOREM

Tellegen's theorem is a very general and very useful theorem. We'll use it repeatedly in this text. Tellegen's theorem is a direct consequence of Kirchhoff's laws.

7.1 Theorem, Proof, and Remarks

Example Consider the digraph shown in Fig. 7.1. Choose *arbitrarily* the

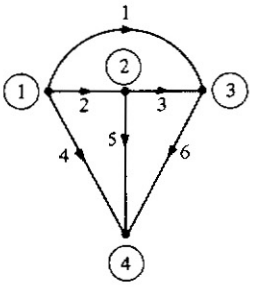

Figure 7.1 A digraph with four nodes and six branches.

values of the currents i_1, i_2, i_3 and calculate i_4, i_5, i_6 so that KCL is satisfied: Let

$$i_1 = 1 \qquad i_2 = 2 \qquad i_3 = 3$$

hence $$i_4 = -3 \qquad i_5 = -1 \qquad i_6 = 4$$

Now choose *arbitrarily* v_4, v_5, and v_6 and calculate v_1, v_2, v_3 so that KVL is satisfied (note that we use associated reference directions). Let

$$v_4 = 4 \qquad v_5 = 5 \qquad v_6 = 6$$

hence $$v_1 = -2 \qquad v_2 = -1 \qquad v_3 = -1$$

Note that $i_1, i_2, \ldots, i_6$ obey KCL and $v_1, v_2, \ldots, v_6$ obey KVL for the circuit under consideration. Now it is easy to verify that

$$\sum_{k=1}^{6} v_k i_k = 0$$

This result is surprising since the i_k's and the v_k's seem to bear so little relation to each other.

Tellegen's theorem Consider an arbitrary circuit. Let the digraph $\mathcal{G}$ have b branches. Let us use associated reference directions. Let $\mathbf{i} = (i_1, i_2, \ldots, i_b)^T$ be *any* set of branch currents satisfying KCL for $\mathcal{G}$ and let $\mathbf{v} = (v_1, v_2, \ldots, v_b)^T$ be *any* set of branch voltages satisfying KVL for $\mathcal{G}$, then

$$\sum_{k=1}^{b} v_k i_k = 0 \qquad \text{or equivalently} \qquad \mathbf{v}^T\mathbf{i} = 0 \tag{7.1}$$

PROOF For the connected digraph $\mathcal{G}$,[10] choose a datum node; hence its reduced matrix $\mathbf{A}$ is defined unambiguously. Since $\mathbf{i}$ satisfies KCL, we have

$$\mathbf{Ai} = \mathbf{0} \tag{7.2}$$

[10] We again use a hinged graph to take care of graphs which are not connected.

Since $\mathbf{v}$ satisfies KVL and since we use associated reference directions, for some node-to-datum voltage vector $\mathbf{e}$, we have

$$\mathbf{v} = \mathbf{A}^T\mathbf{e} \tag{7.3}$$

Using these two equations we obtain successively,

$$\mathbf{v}^T\mathbf{i} = (\mathbf{A}^T\mathbf{e})^T\mathbf{i} = \mathbf{e}^T(\mathbf{A}^T)^T\mathbf{i} = \mathbf{e}^T(\mathbf{A}\mathbf{i}) = 0 \tag{7.4}$$

where in the last step we used Eq. (7.2). ∎

REMARKS

1. The $\mathbf{v}$ and the $\mathbf{i}$ in the theorem need not bear any relation to each other: $\mathbf{v}$ must *only* satisfy KVL and $\mathbf{i}$ must *only* satisfy KCL, and we must use associated reference directions.
2. Suppose that for the given connected digraph $\mathcal{G}$, let $\mathbf{v}'$ and $\mathbf{v}''$ satisfy KVL, and let $\mathbf{i}'$ and $\mathbf{i}''$ satisfy KCL. Then Tellegen's theorem asserts that

$$\mathbf{v}'^T\mathbf{i}' = 0 \qquad \mathbf{v}'^T\mathbf{i}'' = 0 \qquad \mathbf{v}''^T\mathbf{i}' = 0 \qquad \mathbf{v}''^T\mathbf{i}'' = 0 \tag{7.5}$$

Equation (7.5) is of particular interest. Note that $\mathbf{v}'$, $\mathbf{v}''$, $\mathbf{i}'$, and $\mathbf{i}''$ are not related other than by the fact that they pertain to the same digraph and that they each independently satisfy Kirchhoff's laws. Clearly, Tellegen's theorem depicts only the interconnection properties of the circuit or the *topology* of the digraph. We will demonstrate later that this general form of Tellegen's theorem can be used to prove some general results in circuit theory.

7.2 Tellegen's Theorem and Conservation of Energy

Consider a lumped connected circuit and let us measure, at some time t, all its branch voltages $v_k(t)$ and all its branch currents $i_k(t)$, $k = 1, 2, \ldots, b$. Obviously $\mathbf{v}(t)$ and $\mathbf{i}(t)$ satisfy KVL and KCL, hence, by Tellegen's theorem

$$\mathbf{v}(t)^T\mathbf{i}(t) = \sum_{k=1}^{b} v_k(t)\, i_k(t) = 0 \tag{7.6}$$

Now, since we use associated reference directions, $v_k(t)i_k(t)$ is the power delivered, at time t, *to* branch k *by* the remainder of the circuit; equivalently, $v_k(t)i_k(t)$ is the *rate* at which energy is delivered, at time t, *to* branch k *by* the remainder of the circuit. Hence Eq. (7.6) asserts that the energy is conserved. Thus, for *lumped circuits*, conservation of energy is a consequence of Kirchhoff's laws.

To appreciate the fact that Tellegen's theorem is far more general than conservation of energy, work out the following exercise:

Exercise Consider an arbitrary circuit with digraph $\mathcal{G}$. Suppose that, for all $t \geq 0$, $\mathbf{v}(t)$ satisfies KVL for $\mathcal{G}$ and $\mathbf{i}(t)$ satisfies KCL for $\mathcal{G}$. Show that for all $t_1, t_2 \geq 0$

$$\sum_{k=1}^{b} v_k(t_1) i_k(t_2) = 0 \qquad \sum_{k=1}^{b} v_k(t_2) i_k(t_1) = 0 \tag{7.7a}$$

$$\sum_{k=1}^{b} v_k(t_1) \dot{i}_k(t_2) = 0 \qquad \sum_{k=1}^{b} \dot{v}_k(t_1) i_k(t_2) = 0 \tag{7.7b}$$

$$\sum_{k=1}^{b} v_k(t_2) \dot{i}_k(t_1) = 0 \qquad \sum_{k=1}^{b} \dot{v}_k(t_2) i_k(t_1) = 0 \tag{7.7c}$$

where $\dot{v}_k(t)$ denotes $dv_k/dt(t)$ and $\dot{i}_k(t)$ denotes $di_k/dt(t)$.

7.3 The Relation between Kirchhoff's Laws and Tellegen's Theorem

In circuit theory there are two fundamental postulates: KCL and KVL. We have proved that KCL and KVL imply Tellegen's theorem. It is interesting to note that any one of Kirchhoff's laws together with Tellegen's theorem implies the other. More precisely we have the following properties:

Properties

1. If, for all $\mathbf{v}$ satisfying KVL, $\mathbf{v}^T\mathbf{i} = 0$ then $\mathbf{i}$ satisfies KCL.
2. If, for all $\mathbf{i}$ satisfying KCL, $\mathbf{v}^T\mathbf{i} = 0$, then $\mathbf{v}$ satisfies KVL.

PROOF

1. For all $\mathbf{e}$ let $\mathbf{v} = \mathbf{A}^T\mathbf{e}$, and thus $\mathbf{v}$ satisfies KVL. By assumption,

$$0 = \mathbf{v}^T\mathbf{i} = \mathbf{e}^T\mathbf{A}\mathbf{i}$$

   Now since $\mathbf{e}$ is an arbitrary node-to-datum voltage vector, the last equality implies $\mathbf{A}\mathbf{i} = 0$, i.e., $\mathbf{i}$ satisfies KCL.

2. Let ℓ be an arbitrary loop in the graph $\mathcal{G}$. Consider the $\mathbf{i}$ obtained by assigning zero current to all branches of $\mathcal{G}$ except for those of loop ℓ; depending on whether the reference direction of branch j in loop ℓ agrees with that of loop ℓ, we assign i_j to be 1 A or -1 A. The resulting $\mathbf{i}$ satisfies KCL at all nodes of $\mathcal{G}$. Tellegen's theorem gives

$$\sum_{j=1}^{b} v_j i_j = \sum_{\substack{\text{over} \\ \text{branches} \\ \text{in loop } \ell}} \pm v_j = 0$$

   thus the algebraic sum of the branch voltages around loop ℓ is zero, i.e., KVL holds for loop ℓ. Since ℓ is arbitrary, we have shown that KVL holds for all loops of $\mathcal{G}$. ∎

7.4 Geometric Interpretation[11]

In this section we shall use linear vector space to interpret the significance of Kirchhoff's laws and Tellegen's theorem. We will use the standard notations. For example, "$\mathbb{R}^b$" means "a b-dimensional vector space," "$\in$" means "is a member of," etc.

Tellegen's theorem requires that $\mathbf{v}$ satisfy KVL and $\mathbf{i}$ satisfy KCL for the given digraph $\mathcal{G}$. Let $\mathcal{G}$ be connected and have b branches and n nodes. From Sec. 6.3, we have

KCL: $$\mathbf{Ai} = \mathbf{0} \tag{7.8}$$

KVL: $$\mathbf{v} = \mathbf{A}^T\mathbf{e} \tag{7.9}$$

We state the following properties based on the discussion of linear independence of equations.

KCL properties

1. The $(n-1) \times b$ matrix $\mathbf{A}$ is full rank, i.e., its $n-1$ rows are linearly independent vectors in the b-dimensional space $\mathbb{R}^b$. (7.10)
2. $\mathbf{Ai}(t) = \mathbf{0} \Leftrightarrow$ the b-dimensional current vector $\mathbf{i}(t)$ satisfies KCL. (7.11)
3. The set of all branch current vectors $\mathbf{i}$ that satisfy KCL form a subspace, called the *KCL solution space*, and we label it K_i. (7.12)
4. Since K_i is obtained by imposing $n-1$ linearly independent constraints on the b-dimensional current vector $\mathbf{i}$, the *dimension* of K_i is $b-n+1$. (7.13)

The above implies

$$\begin{pmatrix} \mathbf{i} \in \mathbb{R}^b \\ \text{satisfies} \\ \text{KCL} \end{pmatrix} \Leftrightarrow (\mathbf{Ai} = \mathbf{0}) \Leftrightarrow (\mathbf{i} \in K_i) \tag{7.14}$$

KVL properties

1. $\mathbf{A}^T$ has full column rank, i.e., its $n-1$ columns are linearly independent vectors in the b-dimensional space $\mathbb{R}^b$. (7.15)
2. For some $(n-1)$-dimensional vector $\mathbf{e}(t)$, $\mathbf{v}(t) = \mathbf{A}^T\mathbf{e}(t) \Leftrightarrow$ the b-dimensional vector $\mathbf{v}(t)$ satisfies KVL. (7.16)
3. The set of all $\mathbf{v}$'s satisfying KVL form a $(n-1)$-dimensional subspace which we call the *KVL solution space* K_v. (7.17)
4. Since the subspace K_v is spanned by $n-1$ linearly independent vectors, the dimension of K_v is $n-1$. (7.18)

[11] Advanced topic, may be omitted without loss of continuity.

The above implies

$$\begin{pmatrix} \mathbf{v} \in \mathbb{R}^b \\ \text{satisfies} \\ \text{KVL} \end{pmatrix} \Leftrightarrow \begin{pmatrix} \mathbf{v} = \mathbf{A}^T\mathbf{e} \\ \text{for some } \mathbf{e} \\ \text{in } \mathbb{R}^{n-1} \end{pmatrix} \Leftrightarrow (\mathbf{v} \in K_v) \tag{7.19}$$

Now Tellegen's theorem says that for *any* such $\mathbf{v} \in \mathbb{R}^b$ and *any* such $\mathbf{i} \in \mathbb{R}^b$, $\mathbf{v}^T\mathbf{i} = 0$, i.e., the vectors $\mathbf{v}$ and $\mathbf{i}$ are *orthogonal.*

So viewing the subspaces K_v and K_i as subspaces of the *same* vector space $\mathbb{R}^b$, Tellegen's theorem asserts that *every vector in* K_v *is orthogonal to every vector of* K_i. This is denoted by

$$K_v \perp K_i \tag{7.20}$$

i.e., the subspaces K_v and K_i are orthogonal. The orthogonality of K_v and K_i is illustrated in Fig. 7.2.

Recalling that the dimension of K_i is $b - n + 1$ and that of K_v is $n - 1$, the sum of their dimensions is b. Consequently the subspaces K_i and K_v are not only orthogonal, but also have their direct sum equal to $\mathbb{R}^b$. In other words, any vector in $\mathbb{R}^b$ can be written uniquely as the sum of a vector in K_i and a vector in K_v.

To illustrate the equivalences in Eqs. (7.14) and (7.19) we consider two simple examples.

Example 1 $\mathcal{G}$ is the digraph of a two-node three-branch circuit shown in Fig. 7.3; we see that $\mathbf{A}$ is a 1×3 matrix, namely,

$$\mathbf{A} = [1 \;\; 1 \;\; 1]$$

So

$$\mathbf{Ai} = \mathbf{0} \Leftrightarrow i_1 + i_2 + i_3 = 0 \tag{7.21}$$

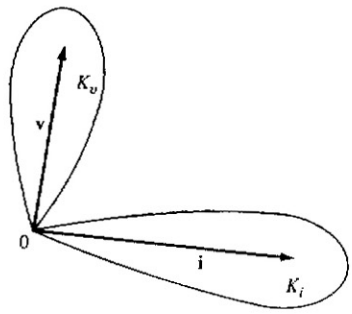

Figure 7.2 Figure illustrating the orthogonality of the subspaces K_i and K_v, where K_i is the set of all i's satisfying KCL and K_v is the set of all v's satisfying KVL.

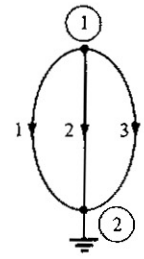

Figure 7.3 A digraph with two nodes and three branches.

$$\mathbf{v} = \mathbf{A}^T\mathbf{e} \Leftrightarrow \begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} = \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} e_1 \tag{7.22}$$

K_i is a two-dimensional subspace; i_1, i_2, i_3 are constrained by one equation, the KCL at node ①, Eq. (7.21). K_i is shown in Fig. 7.4.

K_v is a one-dimensional subspace: There is only one degree of freedom, namely, the node voltage e_1. [See Eq. (7.22).] K_v is shown in Fig. 7.5. Note that the vector $(1, 1, 1)^T$ which spans K_v is orthogonal to K_i, as required by Tellegen's theorem.

Example 2 $\mathcal{G}$ is the digraph of a three-node four-branch circuit shown in Fig. 7.6. Now **A** is a 2×4 matrix, namely

$$\mathbf{A} = \begin{bmatrix} 1 & 0 & 1 & 1 \\ 0 & 1 & -1 & -1 \end{bmatrix} \tag{7.23}$$

KCL, namely $\mathbf{Ai} = \mathbf{0}$, reads

$$\begin{aligned} i_1 + i_3 + i_4 &= 0 \\ i_2 - i_3 - i_4 &= 0 \end{aligned} \tag{7.24}$$

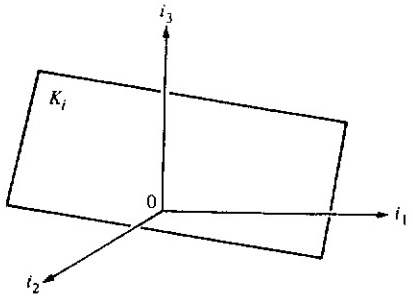

Figure 7.4 The two-dimensional KCL solution space of Example 1.

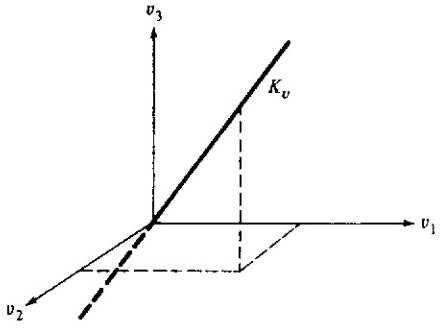

Figure 7.5 The one-dimensional KVL solution space of Example 1.

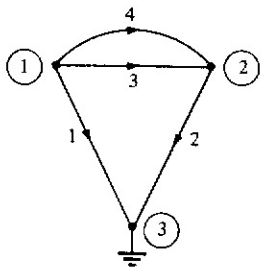

Figure 7.6 A digraph with three modes and four branches considered in Example 2.