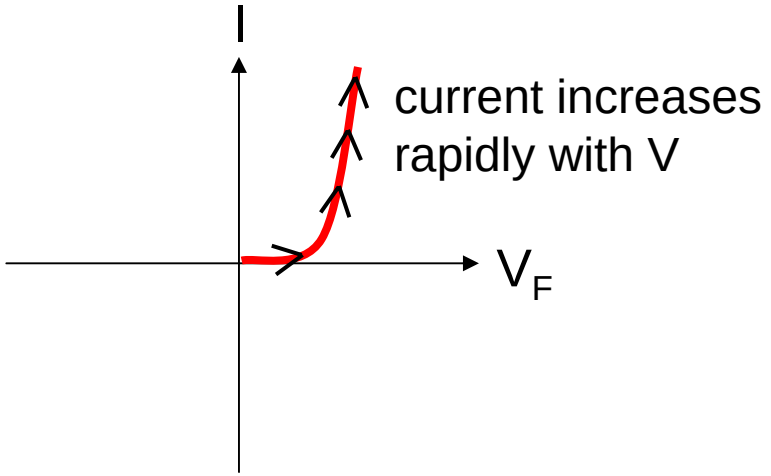
Chapters 2, 4 and 5 from Reader

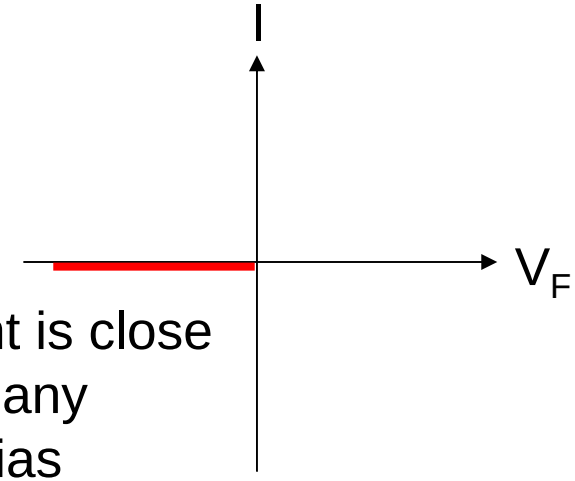
- OUTLINE
  - Diode Current and Equation
  - Some Interesting Circuit Applications
  - Load Line Analysis
  - Solar Cells, Detectors, Zener Diodes
  - Circuit Analysis with Diodes
  - Half-wave Rectifier
  - Clamps and Voltage Doublers using Capacitors
  - MOSFETs
  - Transistor small signal amplifier circuits
- Reading
  - Reader: Chapter 2, Chapter 4 and 5

I-V Characteristics

In forward bias (+ on p-side) we have almost unlimited flow (very low resistance). Qualitatively, the I-V characteristics must look like:



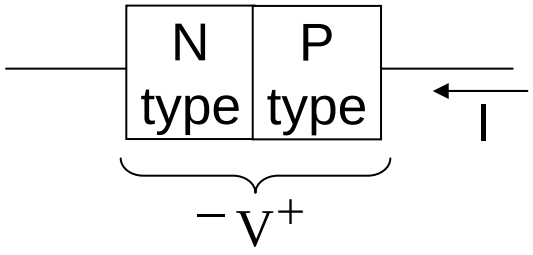
In reverse bias (+ on n-side) almost no current can flow. Qualitatively, the I-V characteristics must look like:



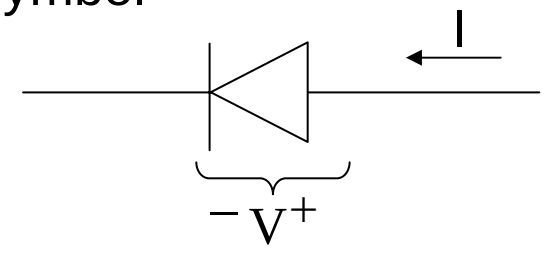
The current is close to zero for any negative bias

Diode Physical Behavior and Equation

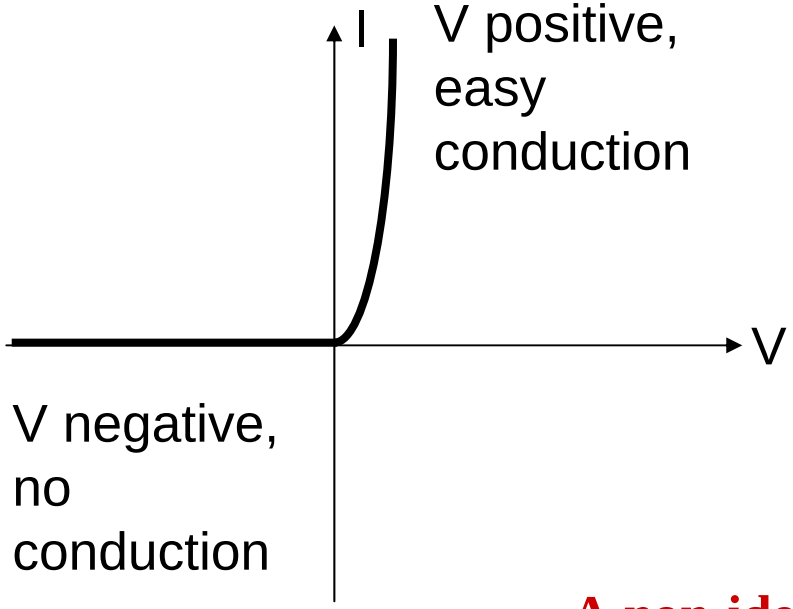
Schematic Device



Symbol



Qualitative I-V characteristics:



Quantitative I-V characteristics:

$$I = I_0(e^{qV/kT} - 1)$$

In which kT/q is 0.026V and I_O is a constant depending on diode area. Typical values: 10^{-12} to 10^{-16} A. Interestingly, the graph of this equation looks just like the figure to the left.

A non-ideality factor n times kT/q is often included.

The pn Junction I vs. V Equation

I-V characteristic of PN junctions

In EECS 105, 130, and other courses you will learn why the I vs. V relationship for PN junctions is of the form

$$I = I_0(e^{qV/kT} - 1)$$

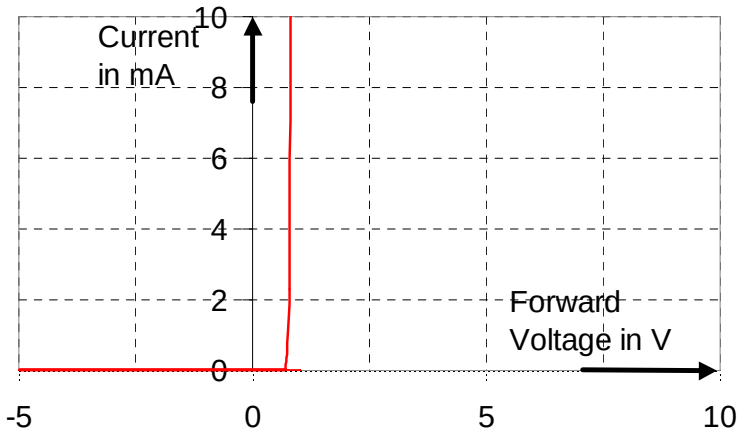
where I_0 is a constant proportional to junction area and depending on doping in P and N regions, $q = \text{electronic charge} = 1.6 \times 10^{-19}$,
k is Boltzman constant, and T is absolute temperature.
$KT/q = 0.026\text{V at} 300°\text{K}$, a typical value for I_0 is $10^{-12} - 10^{-15}\,\text{A}$

We note that in forward bias, I increases **exponentially** and is in the μA-mA range for voltages typically in the range of 0.6-0.8V.
In reverse bias, the current is essentially zero.

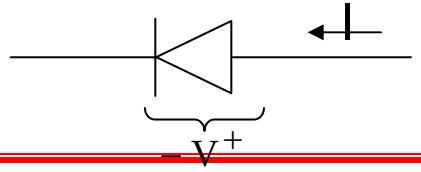
Diode Ideal (Perfect Rectifier) Model

The equation $I = I_0 \exp(^{qV}/_{kT} - 1)$

is graphed below for $I_0 = 10^{-15}\,A$

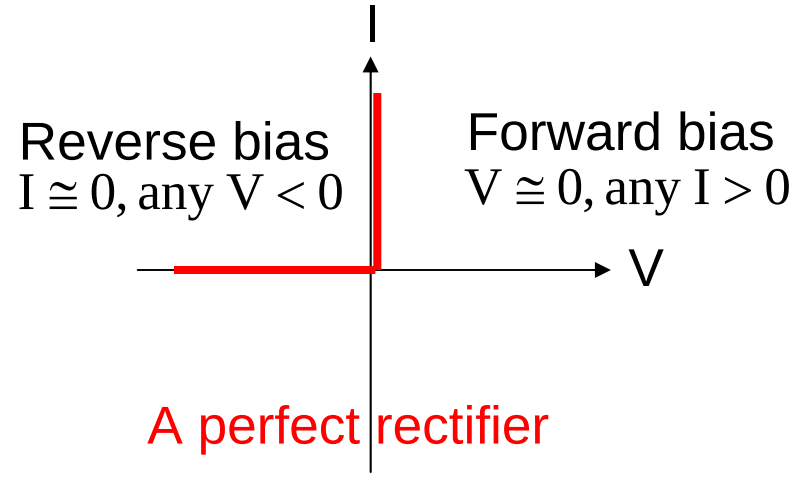


The characteristic is described as a "rectifier" – that is, a device that permits current to pass in only one direction. (The hydraulic analog is a "check value".) Hence the symbol:



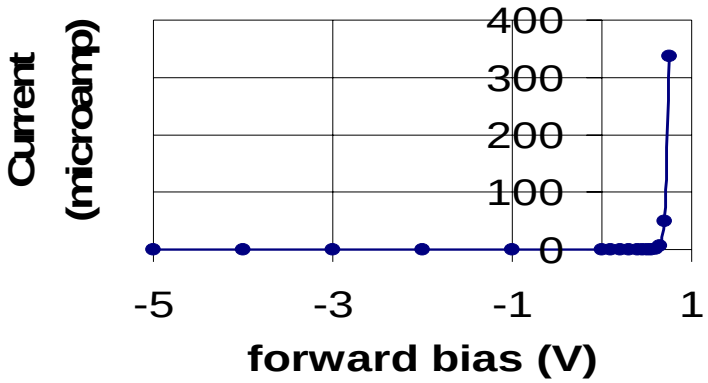
Simple "Perfect Rectifier" Model

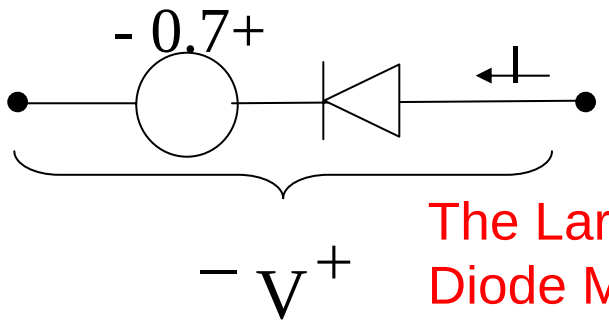
If we can ignore the small forward-bias voltage drop of a diode, a simple effective model is the "perfect rectifier," whose I-V characteristic is given below:



A perfect rectifier

Diode Large-Signal Model (0.7 V Drop)

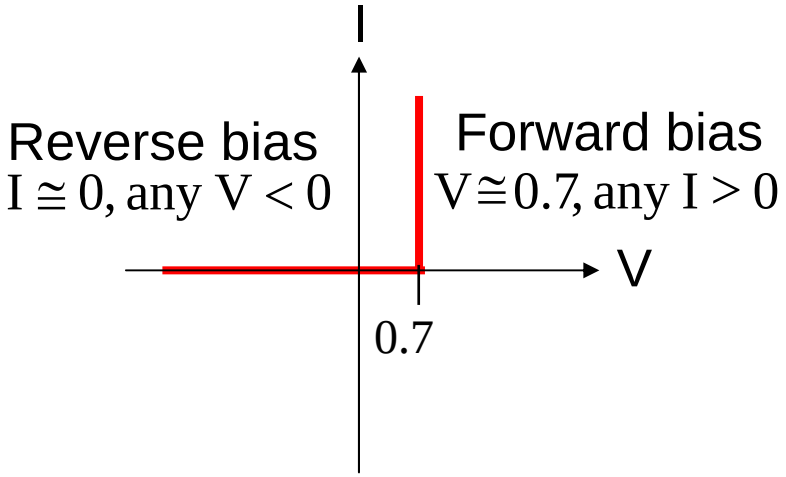




The Large-Signal Diode Model

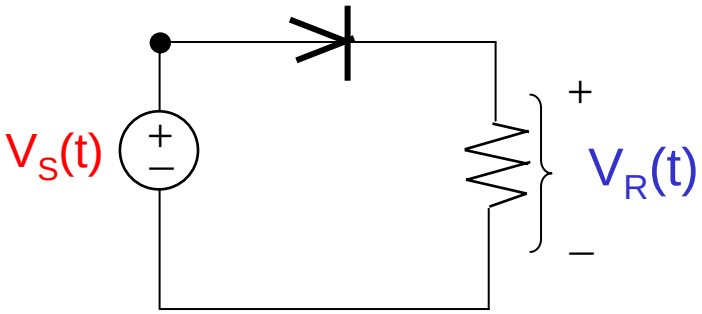
Improved "Large-Signal Diode" Model:

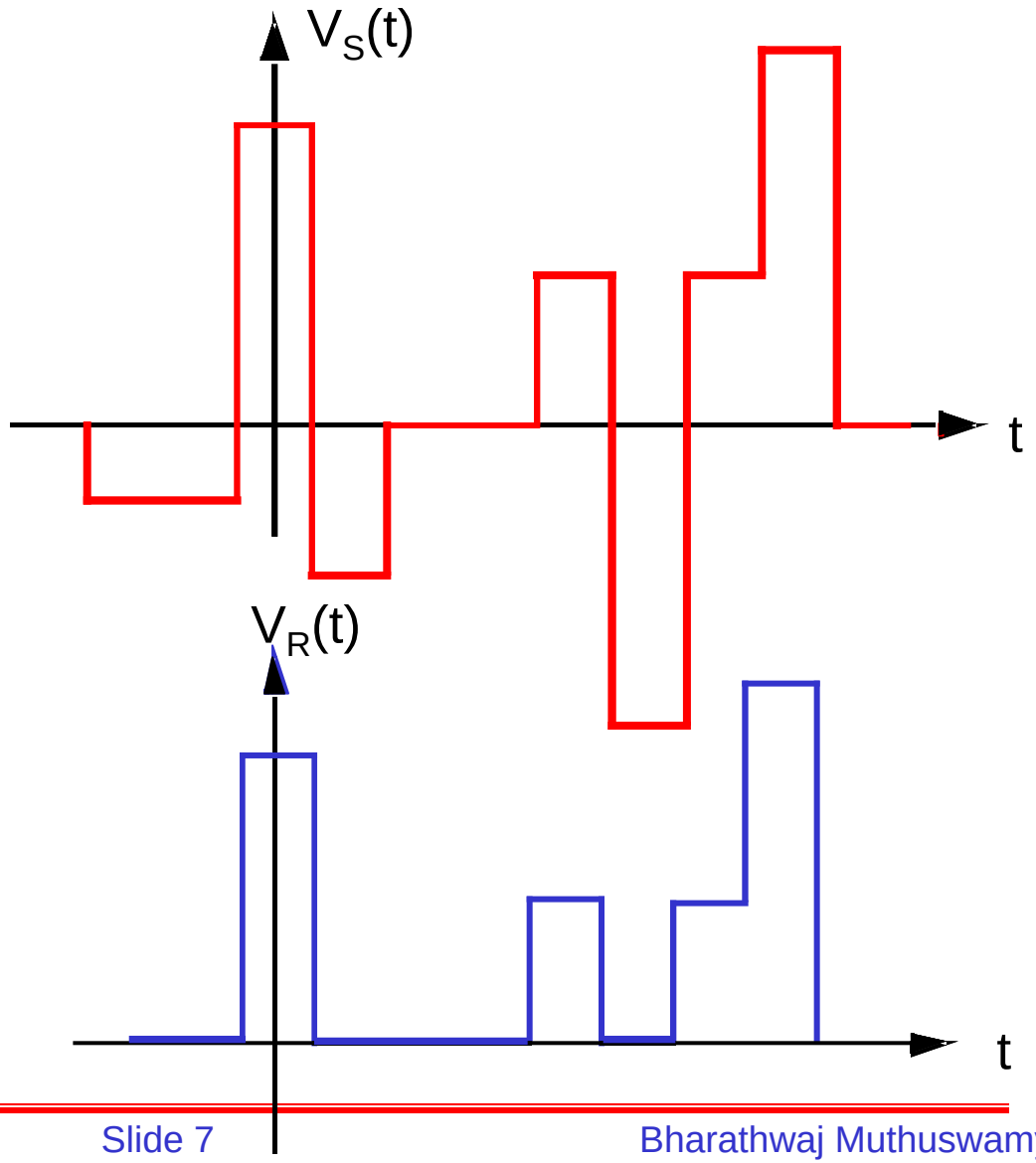
If we choose not to ignore the small forward-bias voltage drop of a diode, it is a very good approximation to regard the voltage drop in forward bias as a constant, about 0.7V. the "Large signal model" results.



Rectifier Circuit

Assume the ideal (perfect rectifier) model.

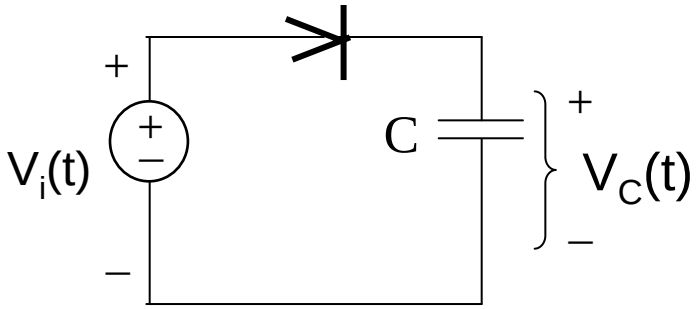


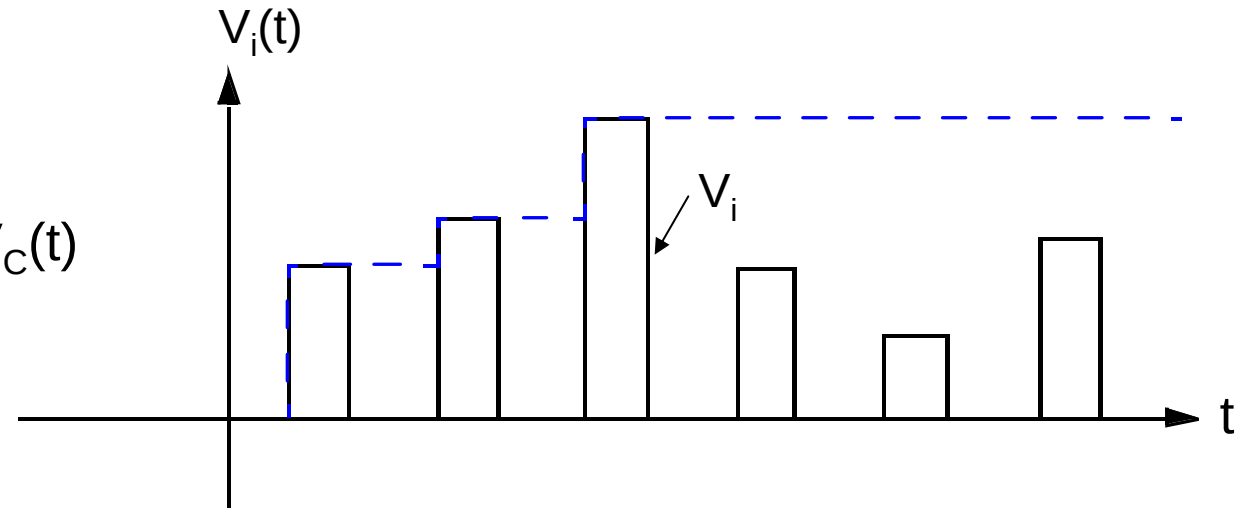


"rectified" version of input waveform

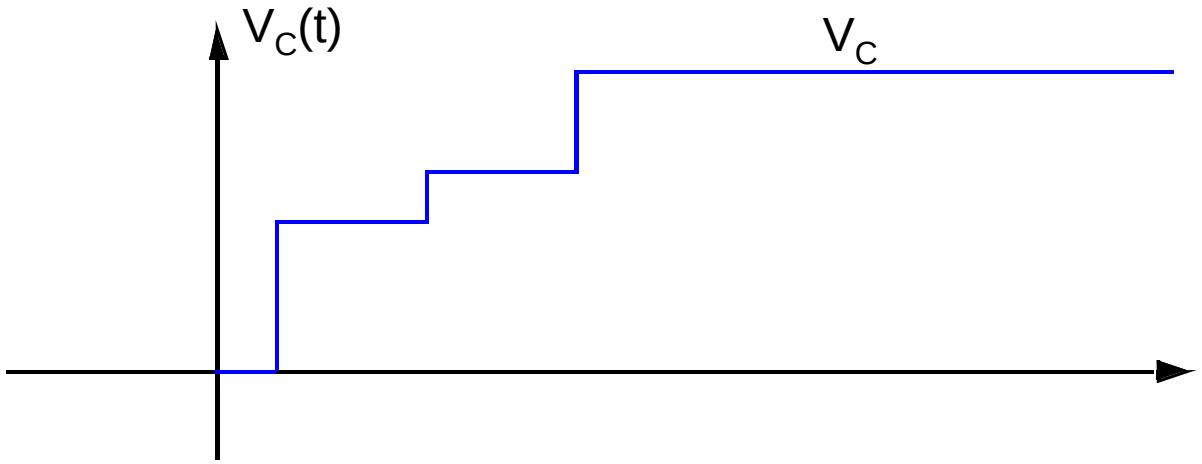
Peak Detector Circuit

Assume the ideal (perfect rectifier) model.



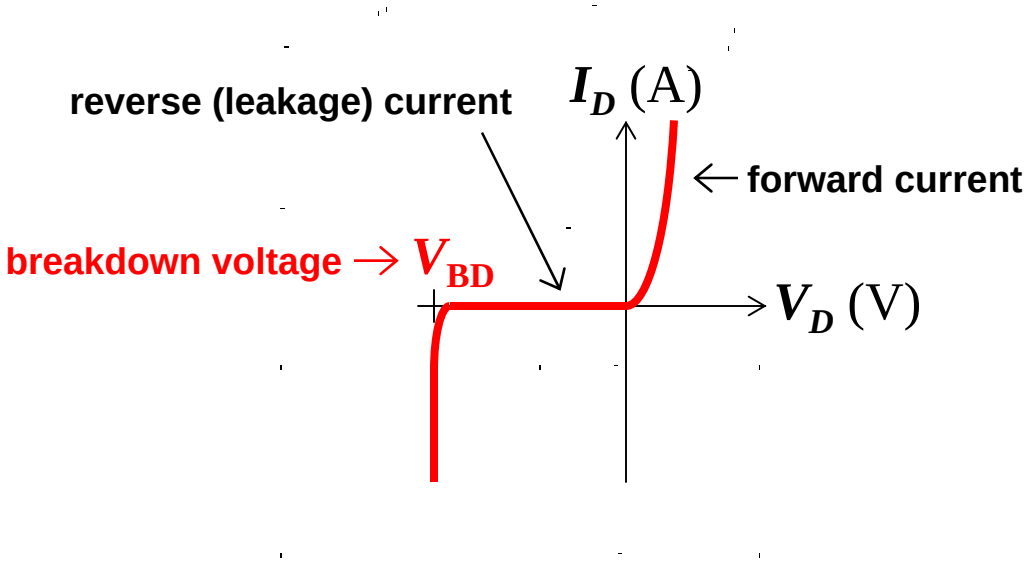


Key Point:
The capacitor charges due to one way current behavior of the diode.



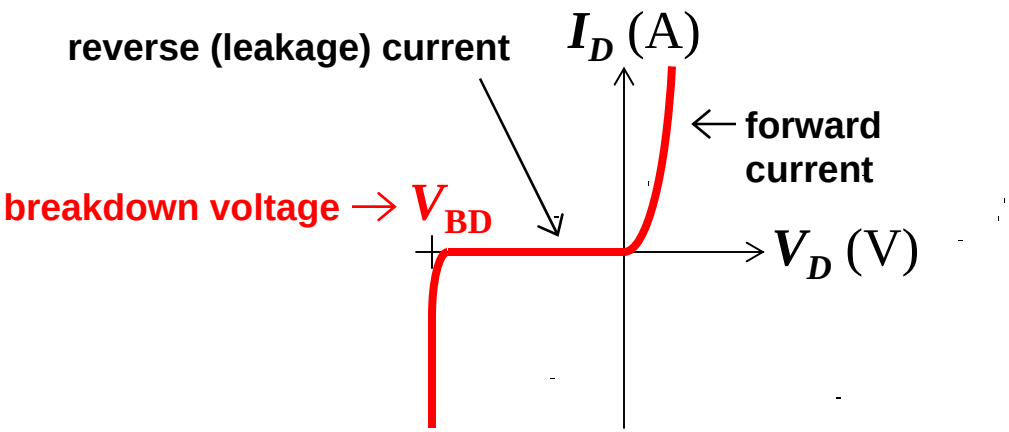
pn-Junction Reverse Breakdown

- As the reverse bias voltage increases, the peak electric field in the depletion region increases. When the electric field exceeds a critical value ($E_{crit} \cong 2\text{x}10^5$ V/cm), the reverse current shows a dramatic increase:

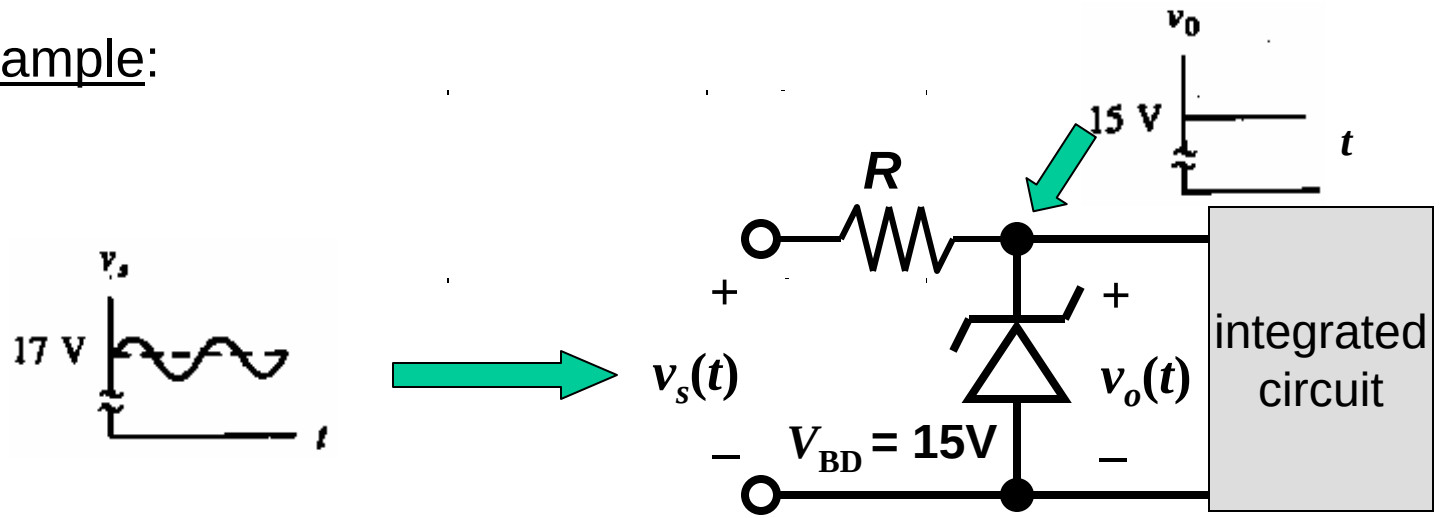


Zener Diode

A ***Zener diode*** is designed to operate in the breakdown mode.

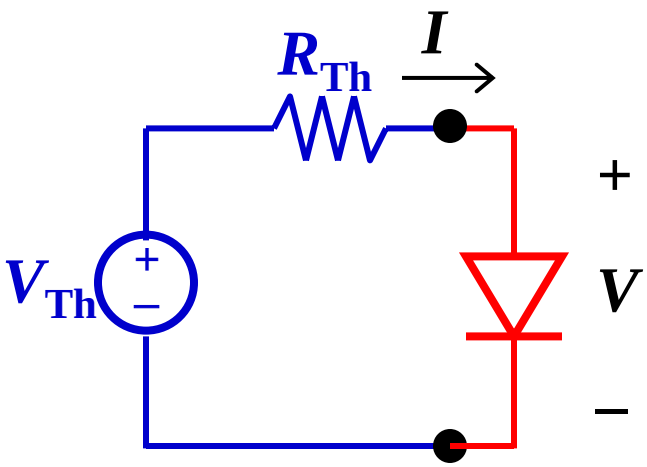


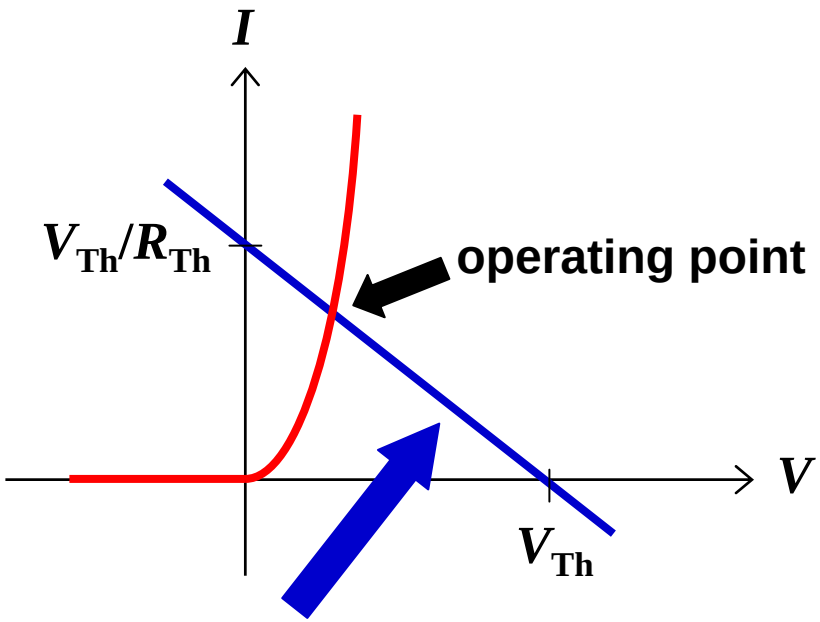
Example:



Load Line Analysis Method

1. Graph the *I-V* relationships for the non-linear element and for the rest of the circuit
2. The operating point of the circuit is found from the intersection of these two curves.

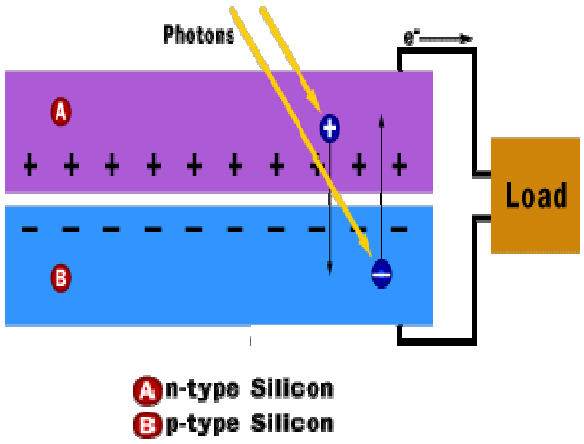




The *I-V* characteristic of all of the circuit except the non-linear element is called the *load line*

Solar cell: Example of simple PN junction

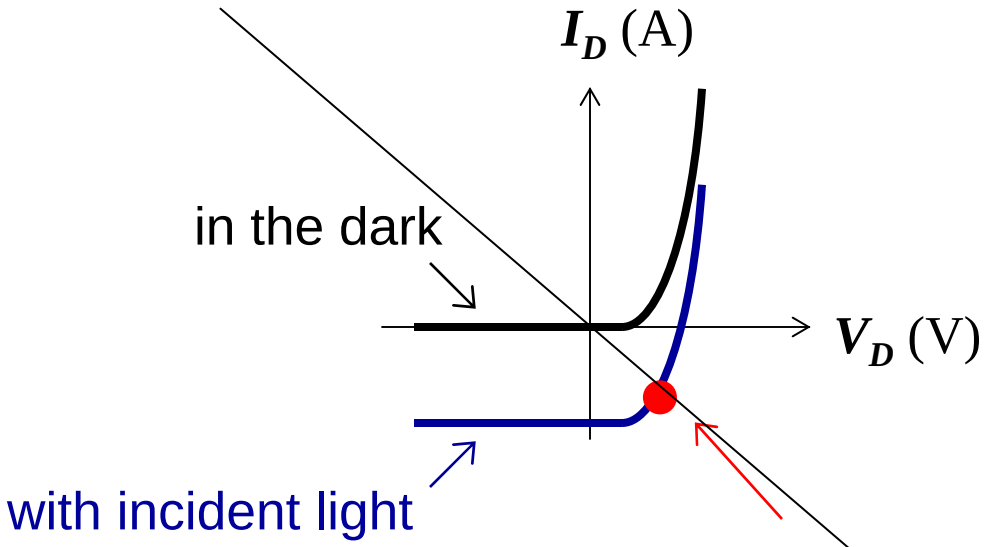
- What is a solar cell?
  - Device that converts sunlight into electricity
- How does it work?
  - In simple configuration, it is a diode made of PN junction
  - Incident light is absorbed by material
  - Creates electron-hole pairs that transport through the material through
    - Diffusion (concentration gradient)
    - Drift (due to electric field)



PN Junction Diode

Photovoltaic (Solar) Cell

$$I_D = I_S(e^{qV_D/kT} - 1) - I_{optical}$$



Operating point

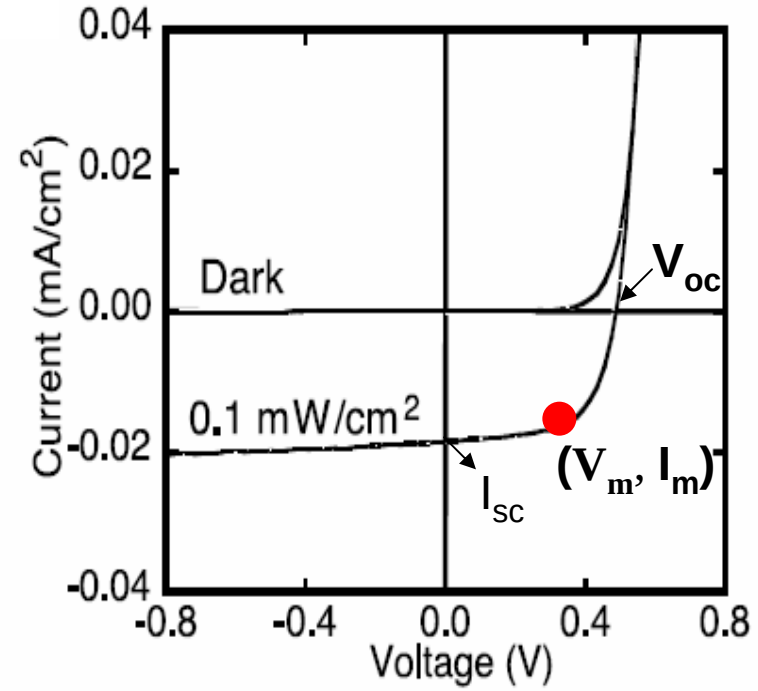
The load line a simple resistor.

I-V characteristics of the device

- I-V characteristics of a PN junction is given by

$$I = I_S\left[\exp(\frac{eV}{kT}) - 1\right] - I_L$$

where I_s is the saturation intensity depending on band gap and doping of the material and I_L is the photocurrent generated due to light



- Efficiency is defined as

$$\eta = \frac{I_m.V_m}{Light\ Intensity} = \frac{FF * V_{oc} * I_{sc}}{Light\ Intensity}$$

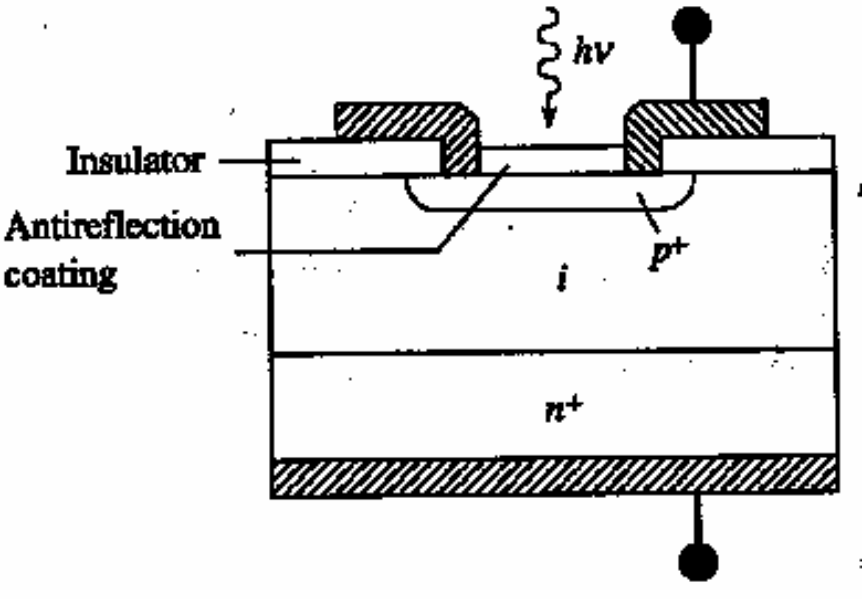
FF is the Fill Factor

V_{oc} - Open circuit voltage

I_{sc} - Short circuit current

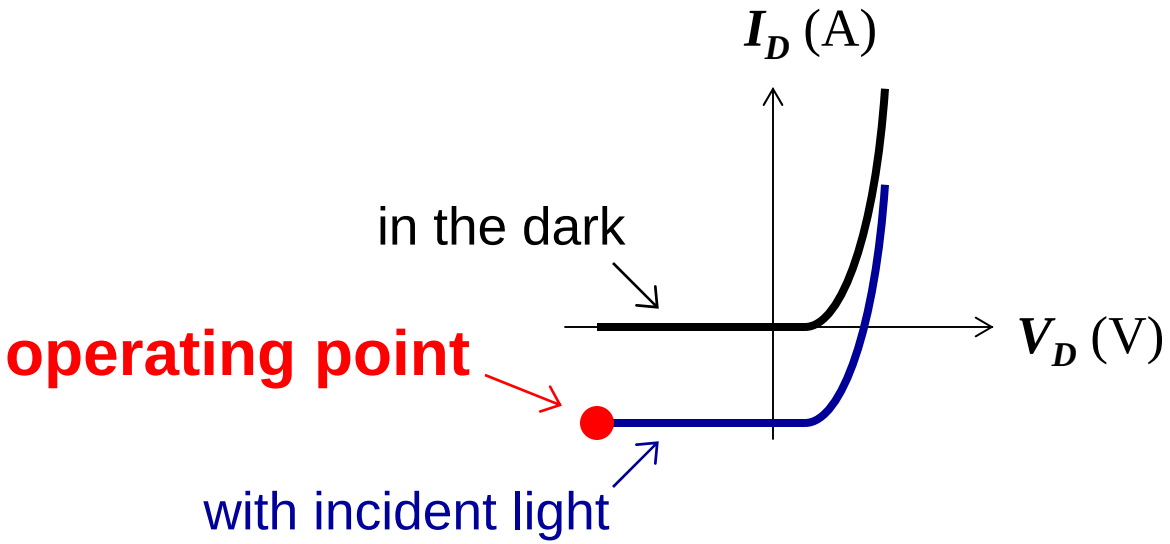
I_{mp}, V_{mp}- Current and voltage at maximum power

Example 2: Photodiode

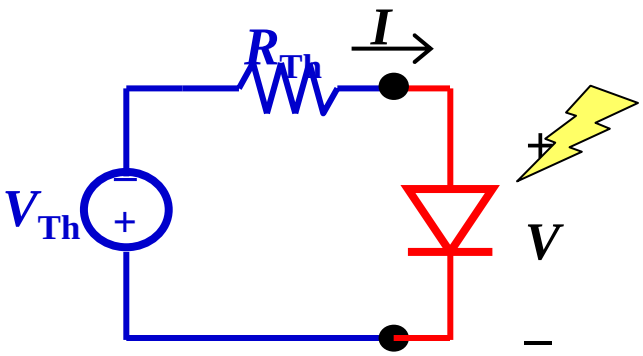


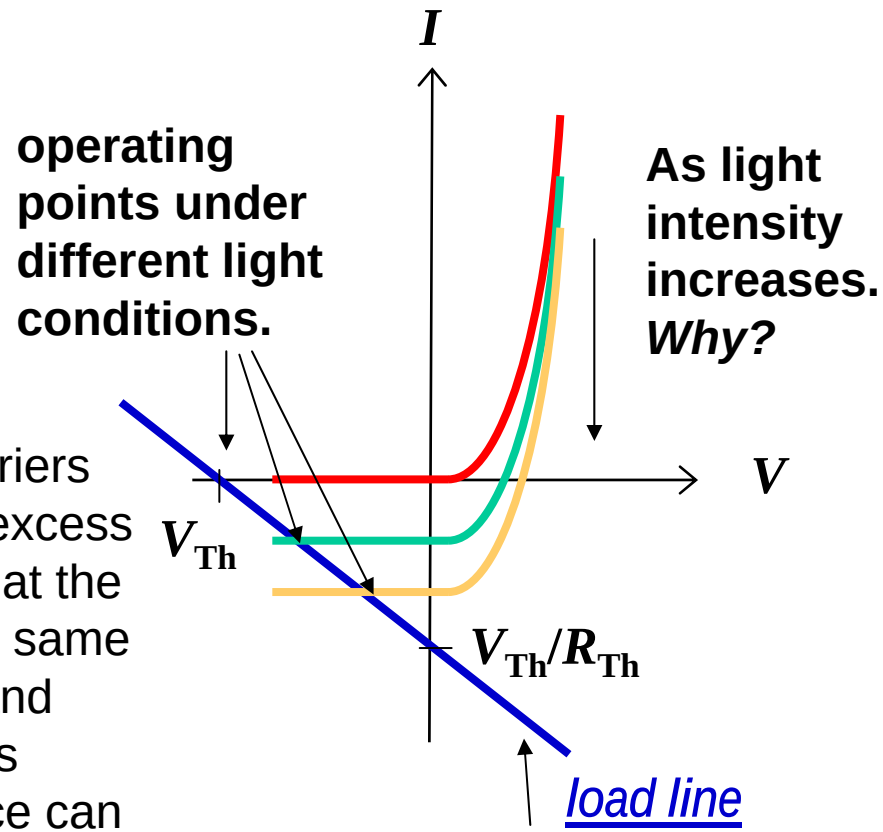
- An intrinsic region is placed between the p-type and n-type regions
  - $W_j \cong W_{\text{i-region}}$, so that most of the electron-hole pairs are generated in the depletion region

    → faster response time (~10 GHz operation)



Photodetector Circuit Using Load Line



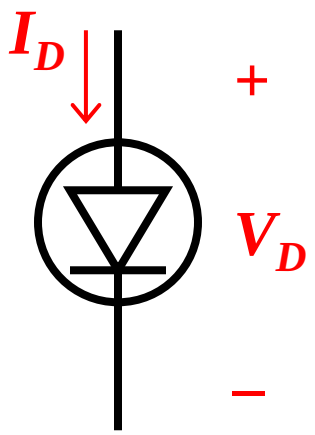


As light shines on the photodiode, carriers are generated by absorption. These excess carriers are swept by the electric field at the junction creating drift current, which is same direction as the reverse bias current and hence negative current. The current is proportional to light intensity and hence can provide a direct measurement of light intensity → photodetector.

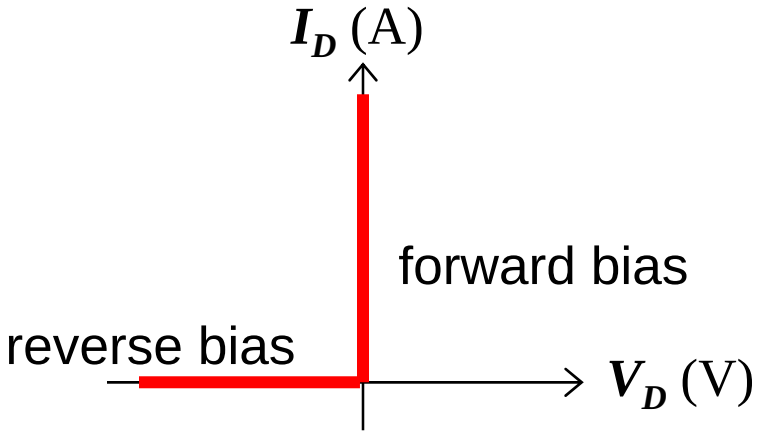
- What happens when R_{th} is too large?
- Why use Vth?

Ideal Diode Model of PN Diode

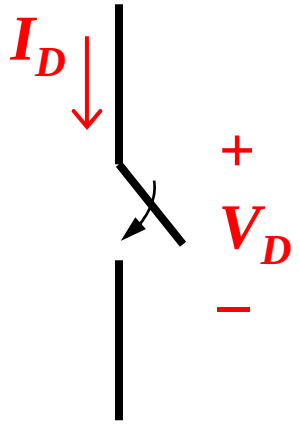
Circuit symbol



***I-V* characteristic**



Switch model

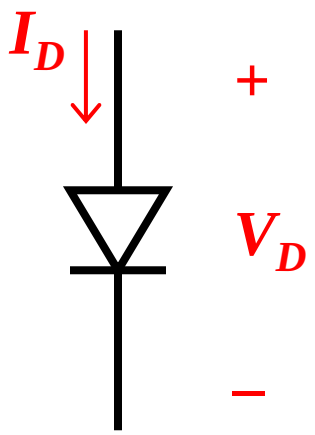


- An ideal diode passes current only in one direction.
- An ***ideal diode*** has the following properties:
  - when $I_D > 0$, $V_D = 0$
  - when $V_D < 0$, $I_D = 0$

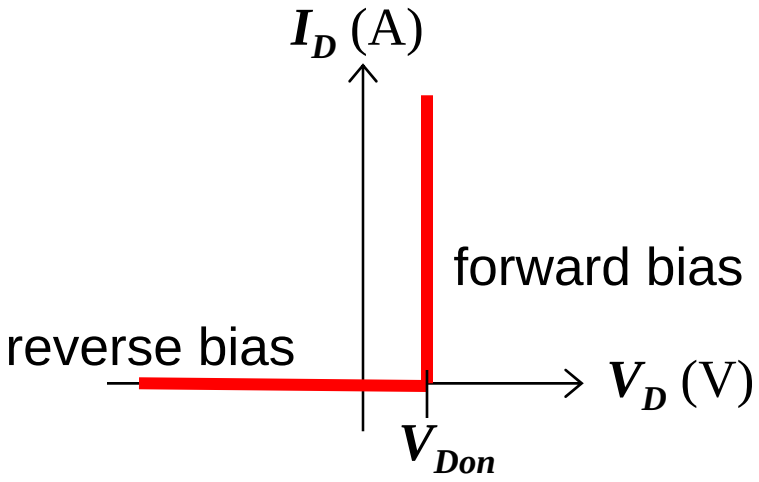
Diode behaves like a switch:
- closed in forward bias mode
- open in reverse bias mode

Large-Signal Diode Model

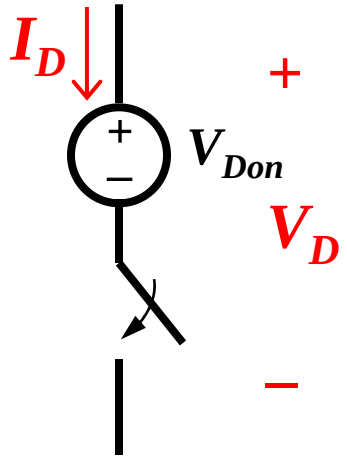
Circuit symbol



***I-V* characteristic**



Switch model



For a Si pn diode, $V_{Don} \cong 0.7$ V

RULE 1: When $I_D > 0$, $V_D = V_{Don}$

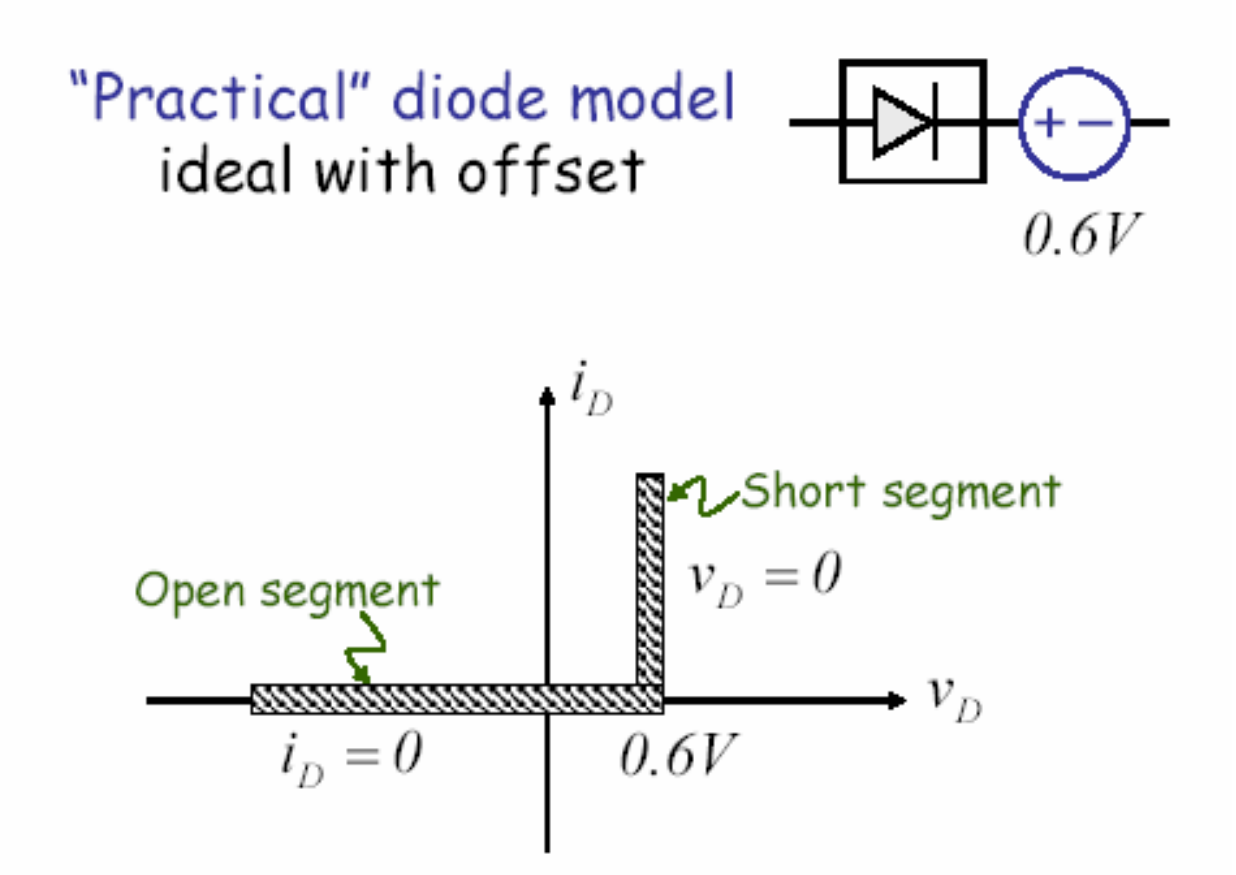
RULE 2: When $V_D < V_{Don}$, $I_D = 0$

Diode behaves like a voltage source in series with a switch:

- closed in forward bias mode
- open in reverse bias mode

Diode: Large Signal Model

- Use piece-wise linear model



How to Analyze Circuits with Diodes

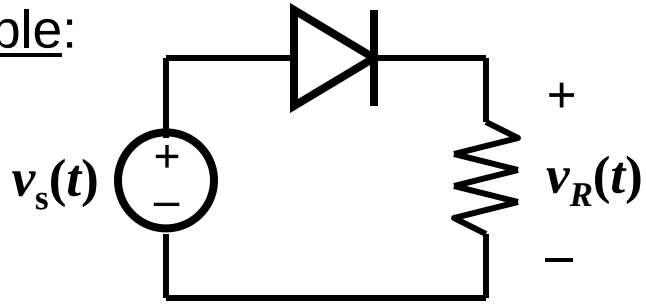
A diode has only two states:

- **forward biased:** $I_D > 0$, $V_D = 0$ V (or 0.7 V)
- **reverse biased:** $I_D = 0$, $V_D < 0$ V (or 0.7 V)

Procedure:

1. Guess the state(s) of the diode(s)
2. Check to see if KCL and KVL are obeyed.
3. If KCL and KVL are not obeyed, refine your guess
4. Repeat steps 1-3 until KCL and KVL are obeyed.

Example:



If $v_s(t) > 0$ V, diode is forward biased (else KVL is disobeyed – try it)

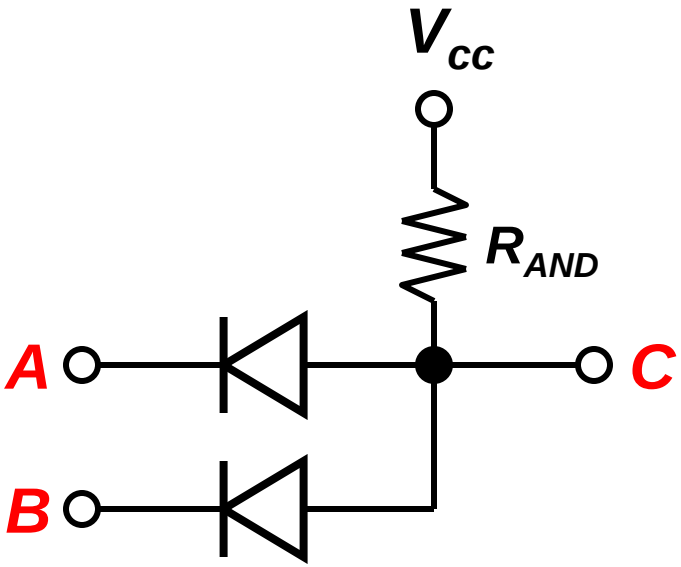
If $v_s(t) < 0$ V, diode is reverse biased (else KVL is disobeyed – try it)

Diode Logic: AND Gate

- Diodes can be used to perform logic functions:

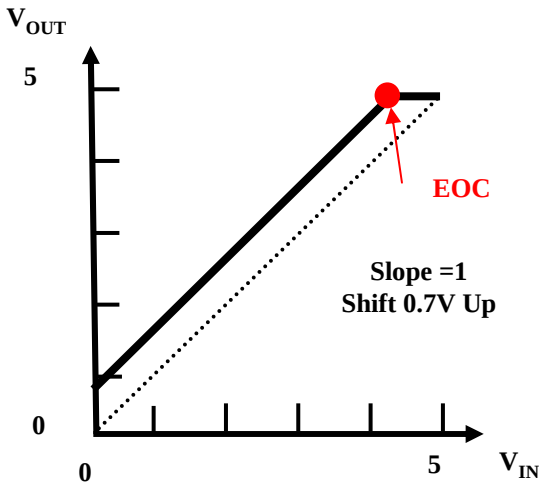
AND gate

output voltage is high only if both A and B are high



Inputs A and B vary between 0 Volts ("low") and V_{cc} ("high")

Between what voltage levels does C vary?

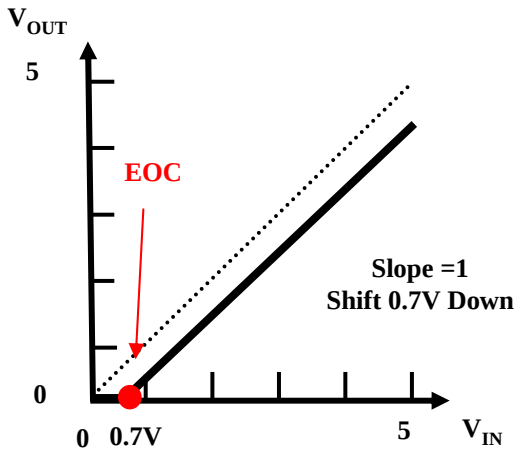


Diode Logic: OR Gate

- Diodes can be used to perform logic functions:

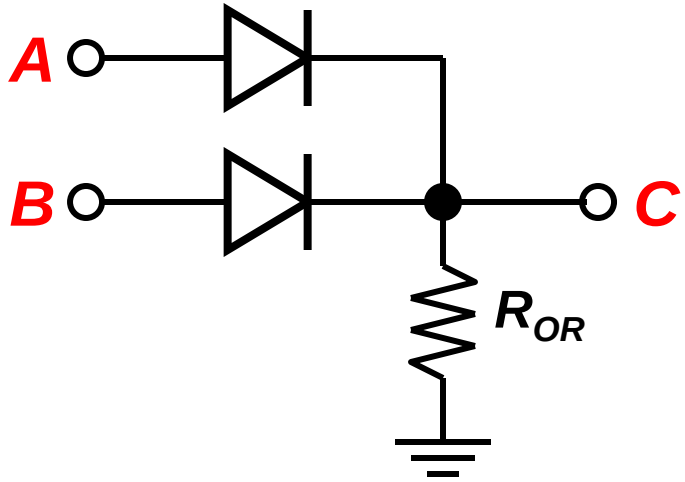
Inputs A and B vary between 0 Volts ("low") and V_{cc} ("high")

Between what voltage levels does C vary?



OR gate

output voltage is high if
either (or both) A and B are high



Diode Logic: Incompatibility and Decay

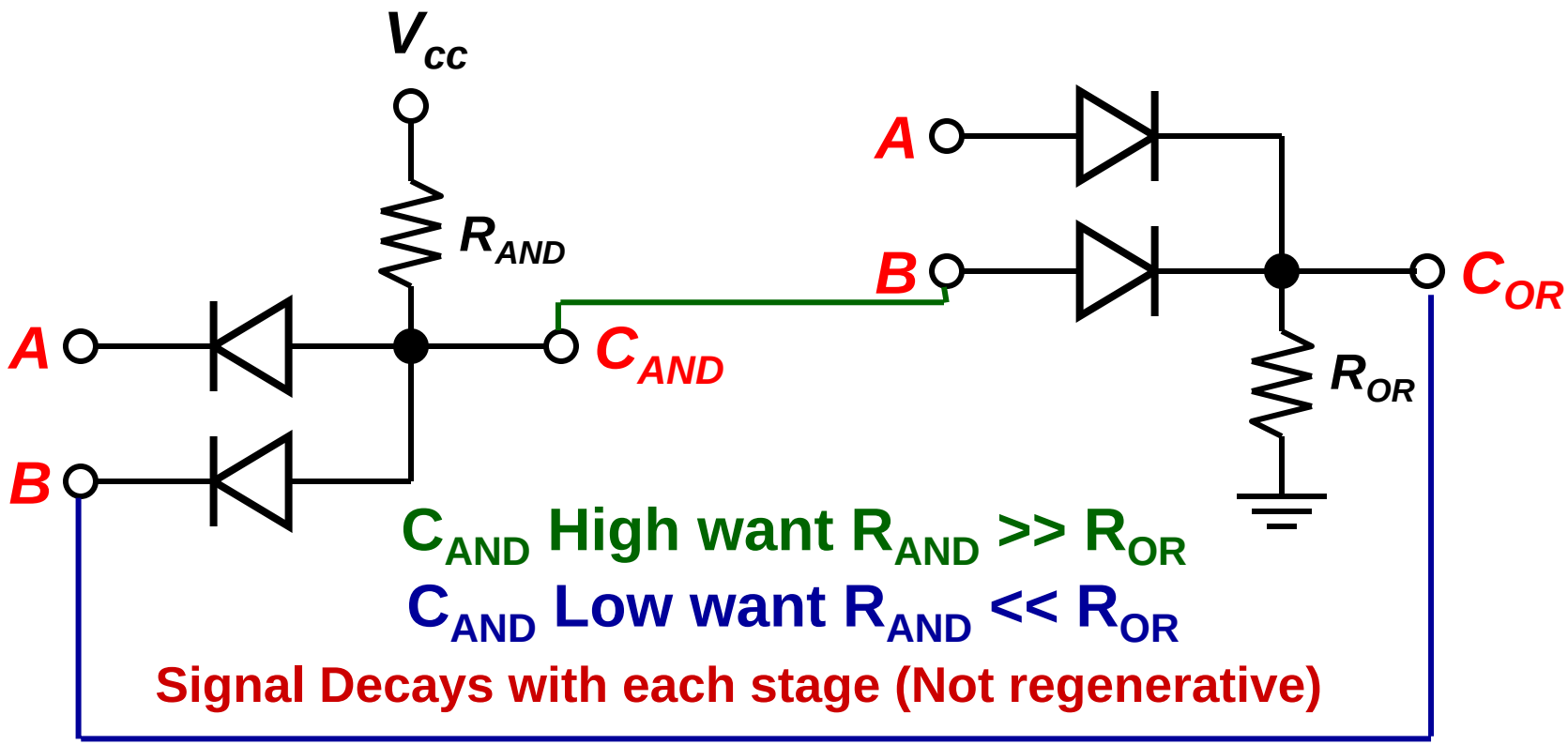
- Diode Only Gates are Basically Incompatible:

AND gate

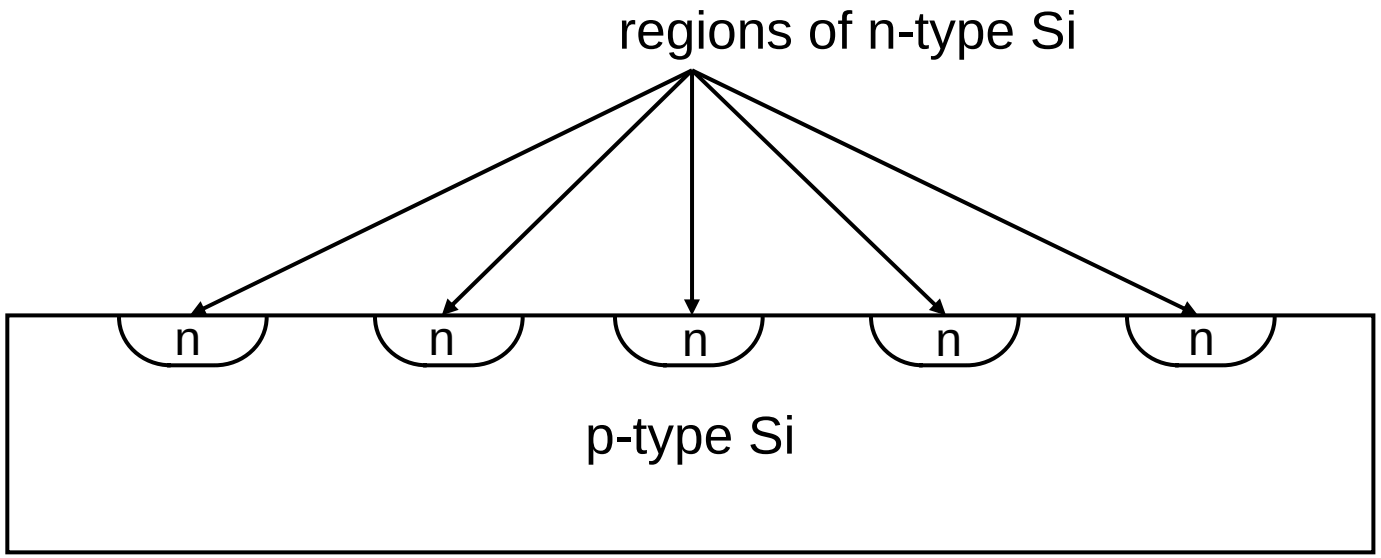
output voltage is high only if both A and B are high

OR gate

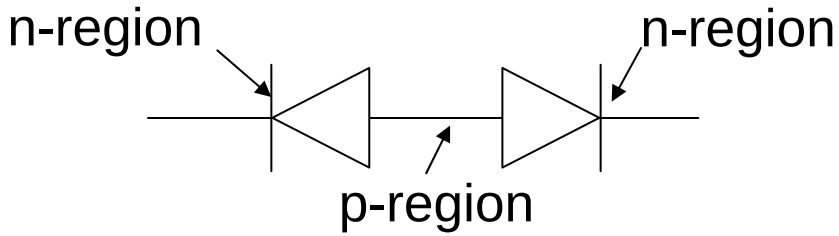
output voltage is high if either (or both) A and B are high



Device Isolation using pn Junctions



No current flows if voltages are applied between n-type regions, because two pn junctions are “back-to-back”



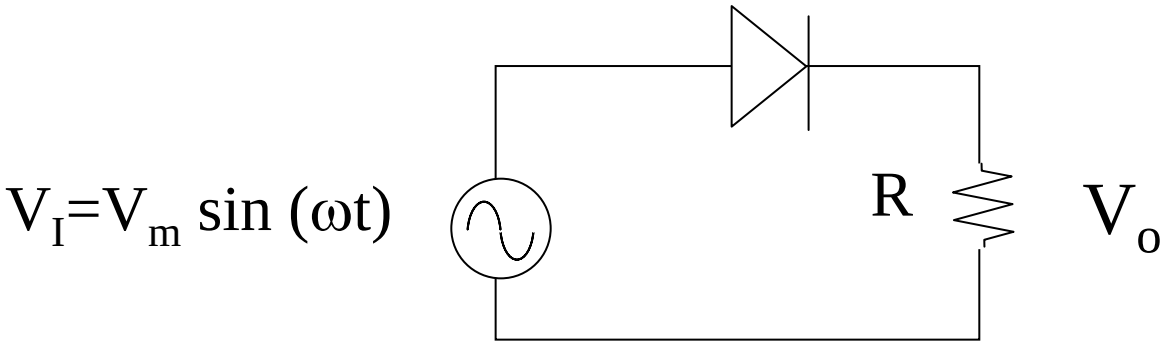
=> n-type regions **isolated** in p-type substrate and vice versa

Why are pn Junctions Important for ICs?

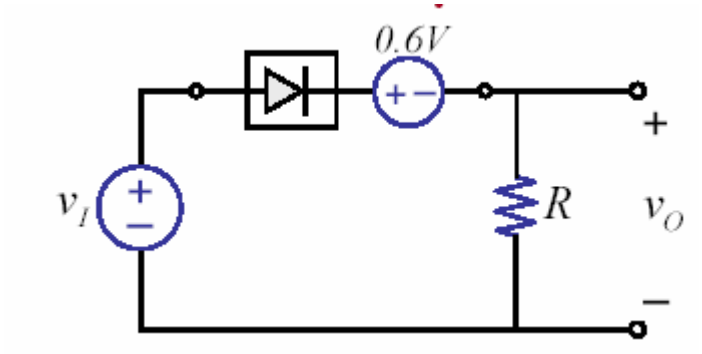
- The basic building block in digital ICs is the MOS transistor, whose structure contains reverse-biased diodes.
  - pn junctions are important for electrical isolation of transistors located next to each other at the surface of a Si wafer.
  - The junction capacitance of these diodes can limit the performance (operating speed) of digital circuits

Power Conversion Circuits

- Converting AC to DC
- Potential applications: Charging a battery



Rectifier Equivalent circuit

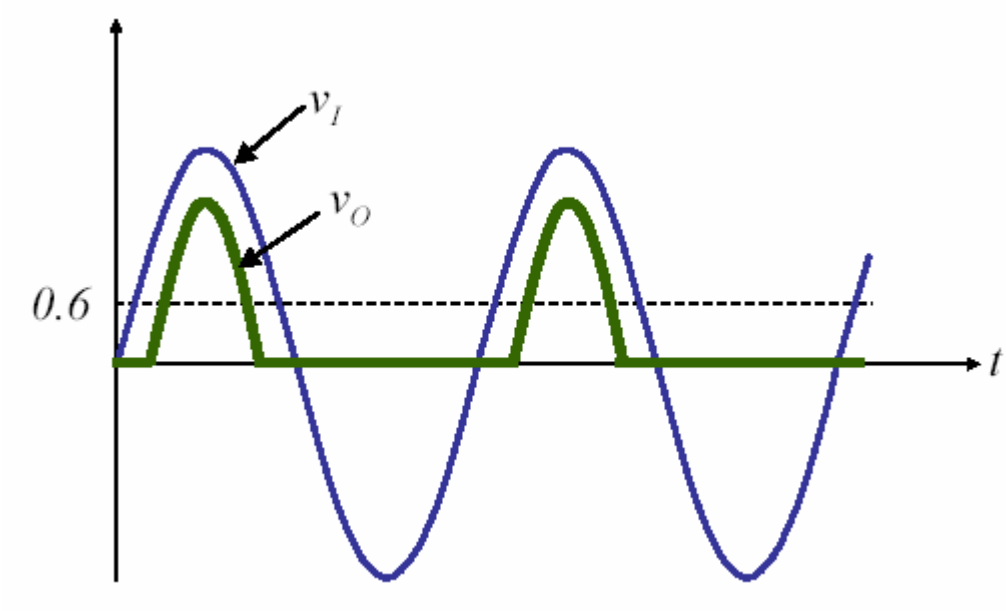


V>0.6V, diode = short circuit

→ $V_o=V_I-0.6$

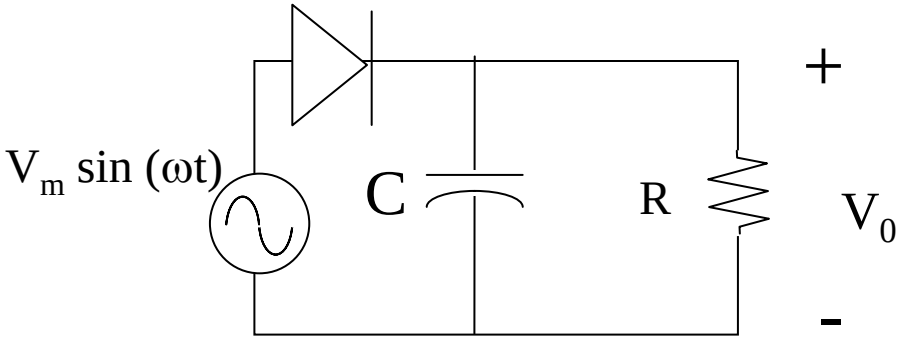
V<0.6V, diode = open circuit

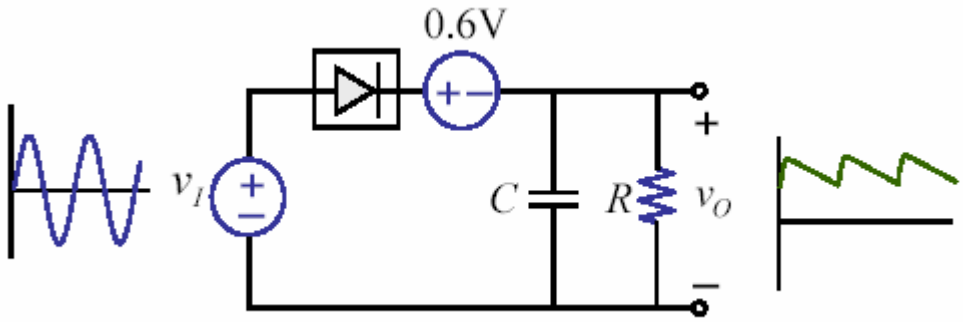
→ Vo=0



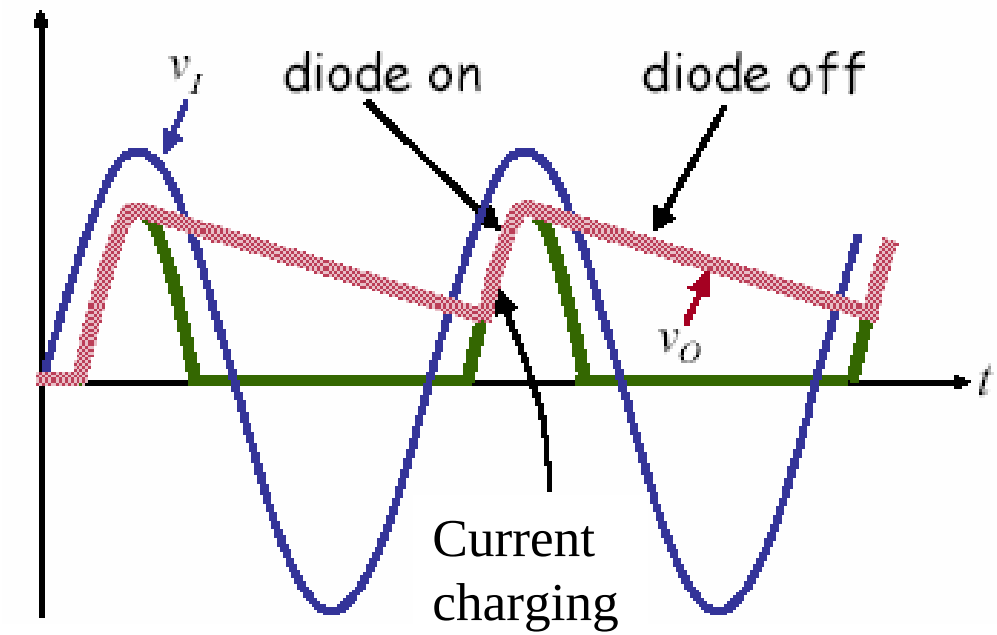
Half-wave Rectifier Circuits

- Adding a capacitor: what does it do?



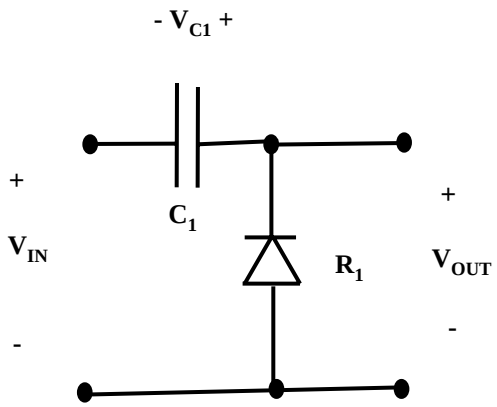


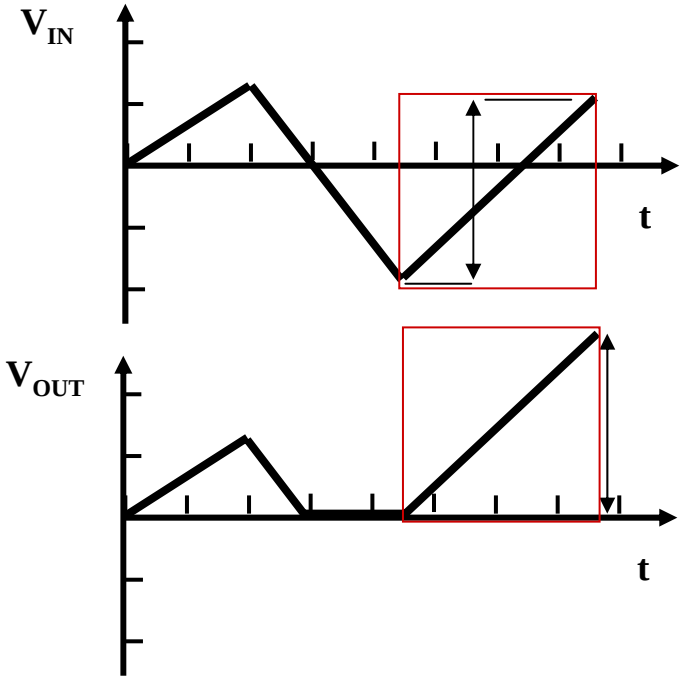
Half-Wave Rectifier



Current charging up capacitor

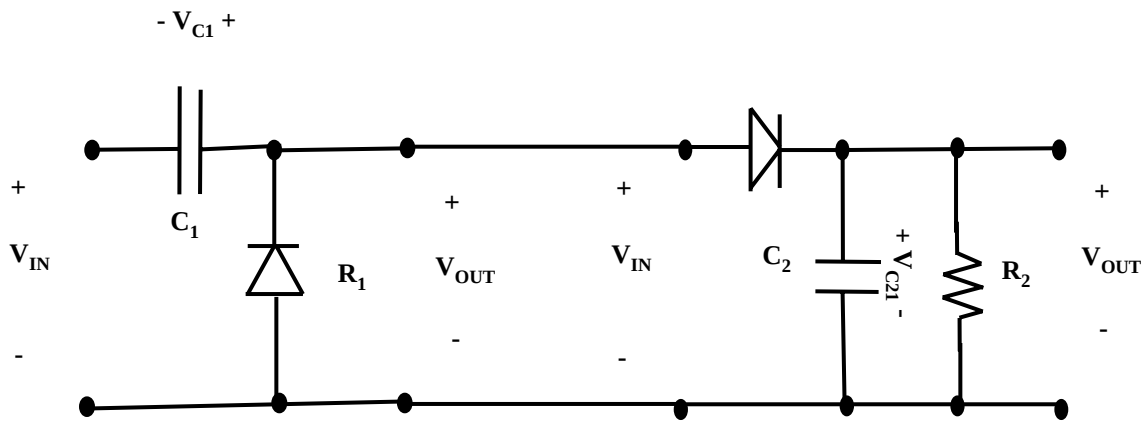
Level Shift Circuit





Once the capacitor is charged by the negative most voltage the rest of the signal is shifted up by that amount.

Voltage Doubler Circuit



Level Shift

Peak Detect

The final output is the peak to peak voltage of the input.

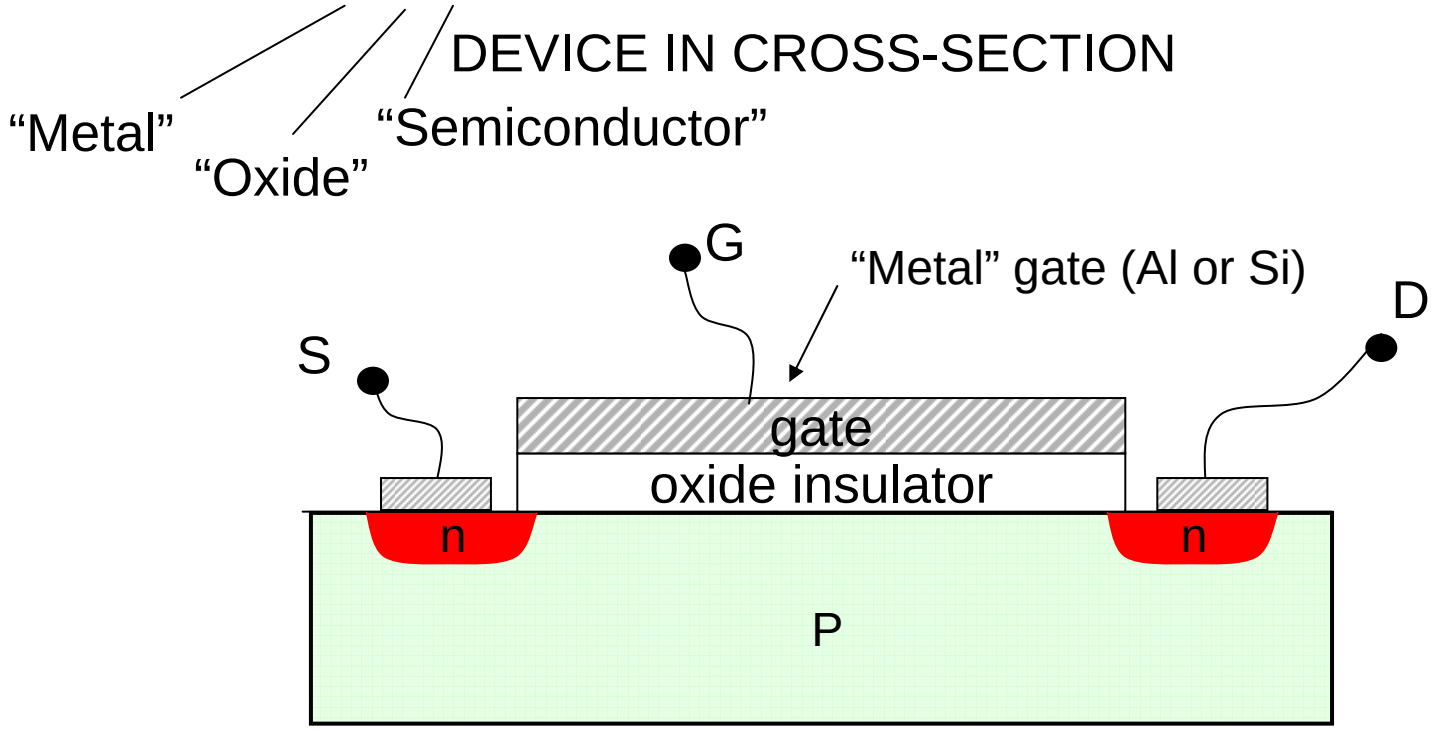
MOSFETs: Detailed outline

- OUTLINE
  - The MOSFET as a controlled resistor
  - Pinch-off and current saturation
  - MOSFET ID vs. VGS characteristic
  - NMOS and PMOS I-V characteristics
  - Load-line analysis; Q operating point; Bias circuits
  - Small-signal equivalent circuits
  - Common source amplifier
  - Source follower
  - Common gate amplifier
  - Gain
- Reading
  - Reader: Chapters 4 and 5

MOSFET Terminals

- The voltage applied to the GATE terminal determines whether current can flow between the SOURCE & DRAIN terminals.
  - For an n-channel MOSFET, the SOURCE is biased at a *lower* potential (often 0 V) than the DRAIN
    (Electrons flow from SOURCE to DRAIN when $V_G > V_T$)
  - For a p-channel MOSFET, the SOURCE is biased at a *higher* potential (often the supply voltage V_{DD}) than the DRAIN
    (Holes flow from SOURCE to DRAIN when $V_G < V_T$)
- The BODY terminal is usually connected to a fixed potential.
  - For an n-channel MOSFET, the BODY is connected to 0 V
  - For a p-channel MOSFET, the BODY is connected to V_{DD}

MOSFET Structure



- In the absence of gate voltage, no current can flow between S and D.
- Above a certain gate to source voltage V_t (the "threshold"), electrons are induced at the surface beneath the oxide. (Think of it as a capacitor.)
- These electrons can carry current between S and D if a voltage is applied.

MOSFET

- Symbol and subscript convention
  - Upper case for both (e.g. V_D) = DC signal (often as bias)
  - Lower case for both (e.g. v_d) = AC signal (often small signal)
  - Lower symbol and upper sub (e.g. v_D) = total signal = V_D+v_d
- NMOS: Three regions of operation
  - V_{DS} and V_{GS} normally positive valus
  - $V_{GS}<V_t$:cut off mode, $I_{DS}=0$ for any V_{DS}
  - $V_{GS}>V_t$:transistor is turned on
    - $V_{DS}< V_{GS}-V_t$: Triode Region $i_D = K\left[2(v_{GS}-V_t)v_{DS}-{v_{DS}}^2\right]$
    - $V_{DS}> V_{GS}-V_t$: Saturation Region $i_D = K\left[2(v_{GS}-V_t)^2\right]$
    - Boundary $v_{GS}-V_t = v_{DS}$ $K = \frac{W}{L}\frac{KP}{2}$

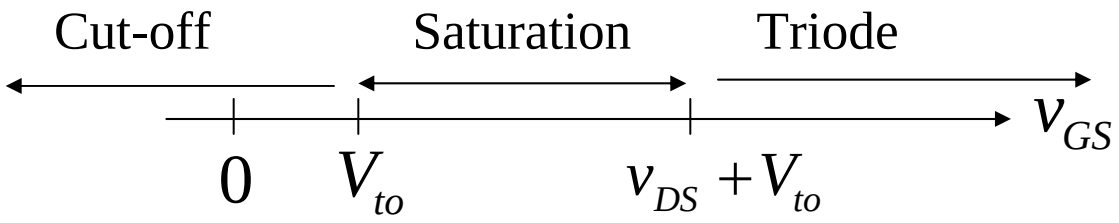
MOSFET

- PMOS: Three regions of operation (interchange > and < from NMOS)
  - V_{DS} and V_{GS} Normally negative values
  - $V_{GS} > V_t$:cut off mode, $I_{DS}=0$ for any V_{DS}
  - $V_{GS} < V_t$:transistor is turned on
    - $V_{DS} > V_{GS}-V_t$: Triode Region $i_D = K\left[2(v_{GS}-V_t)v_{DS} - {v_{DS}}^2\right]$
    - $V_{DS} < V_{GS}-V_t$: Saturation Region $i_D = K\left[2(v_{GS}-V_t)^2\right]$
    - Boundary $v_{GS} - V_t = v_{DS}$

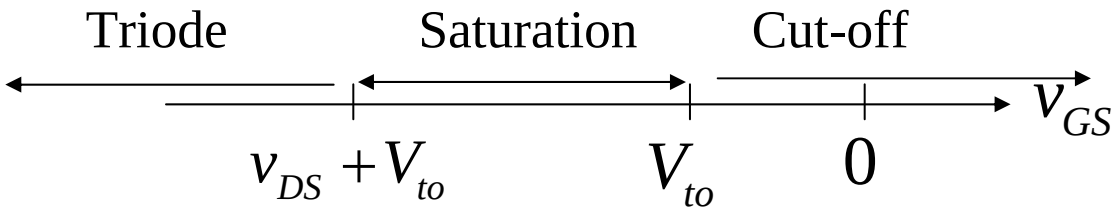
$$K = \frac{W}{L}\frac{KP}{2}$$

MOSFET Operating Regions

NMOS

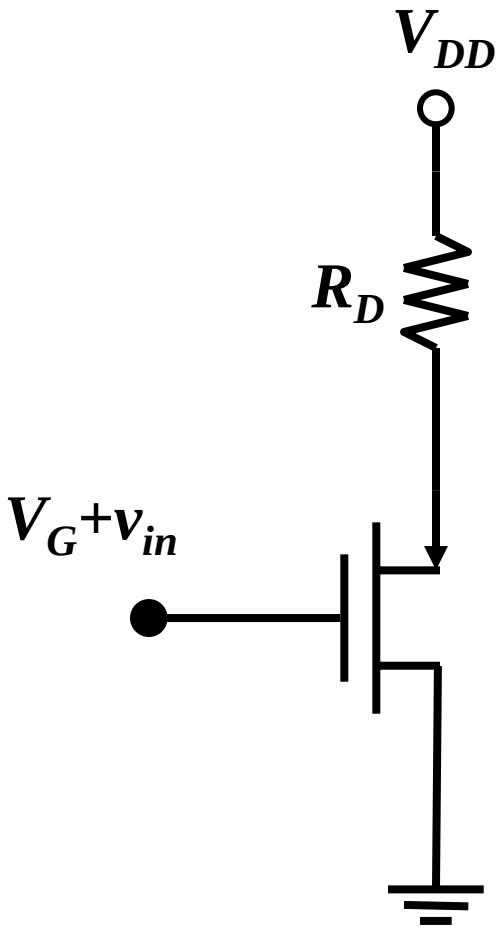


PMOS

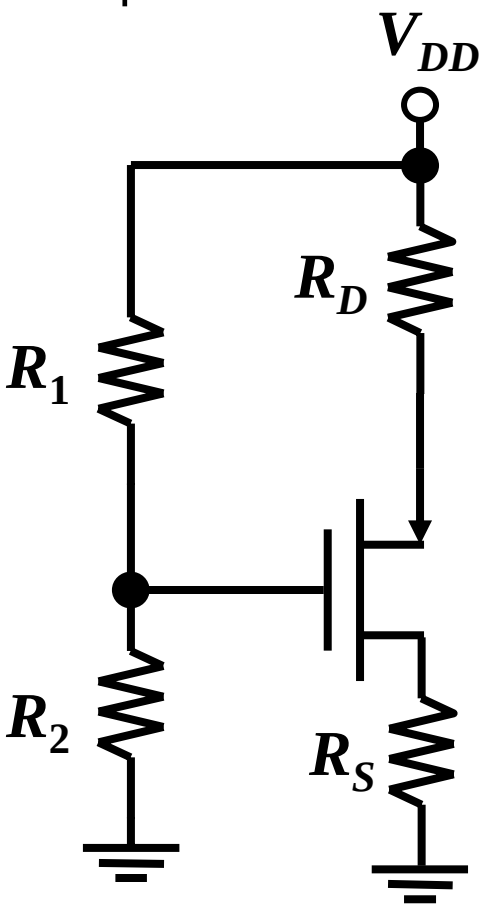


Bias Circuits

- Use load line to find Quiescent operating point.
- Remember no current flow through the gate.



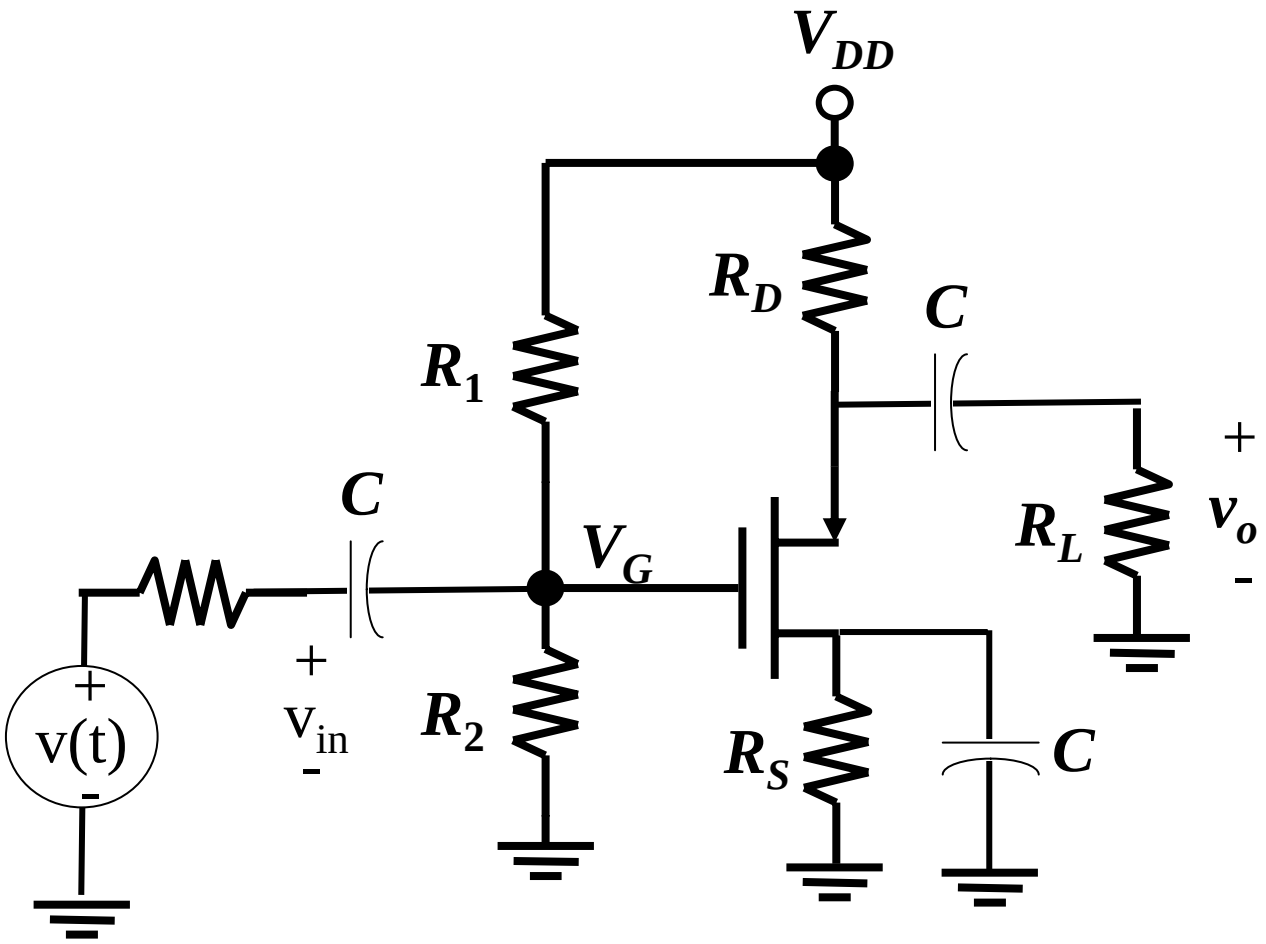
Fixed-plus Self-Bias CKT



MOSFET Circuit

- First look at DC case to find Q point
  - Use load line technique
  - All capacitors are open circuit
  - From Q-point, get g_m and r_d for small signal AC model
- AC Small signal analysis
  - DC source is AC ground (because there is no AC signal variation).
  - All capacitors are short circuit (unless otherwise specified).

Common Source Amplifier

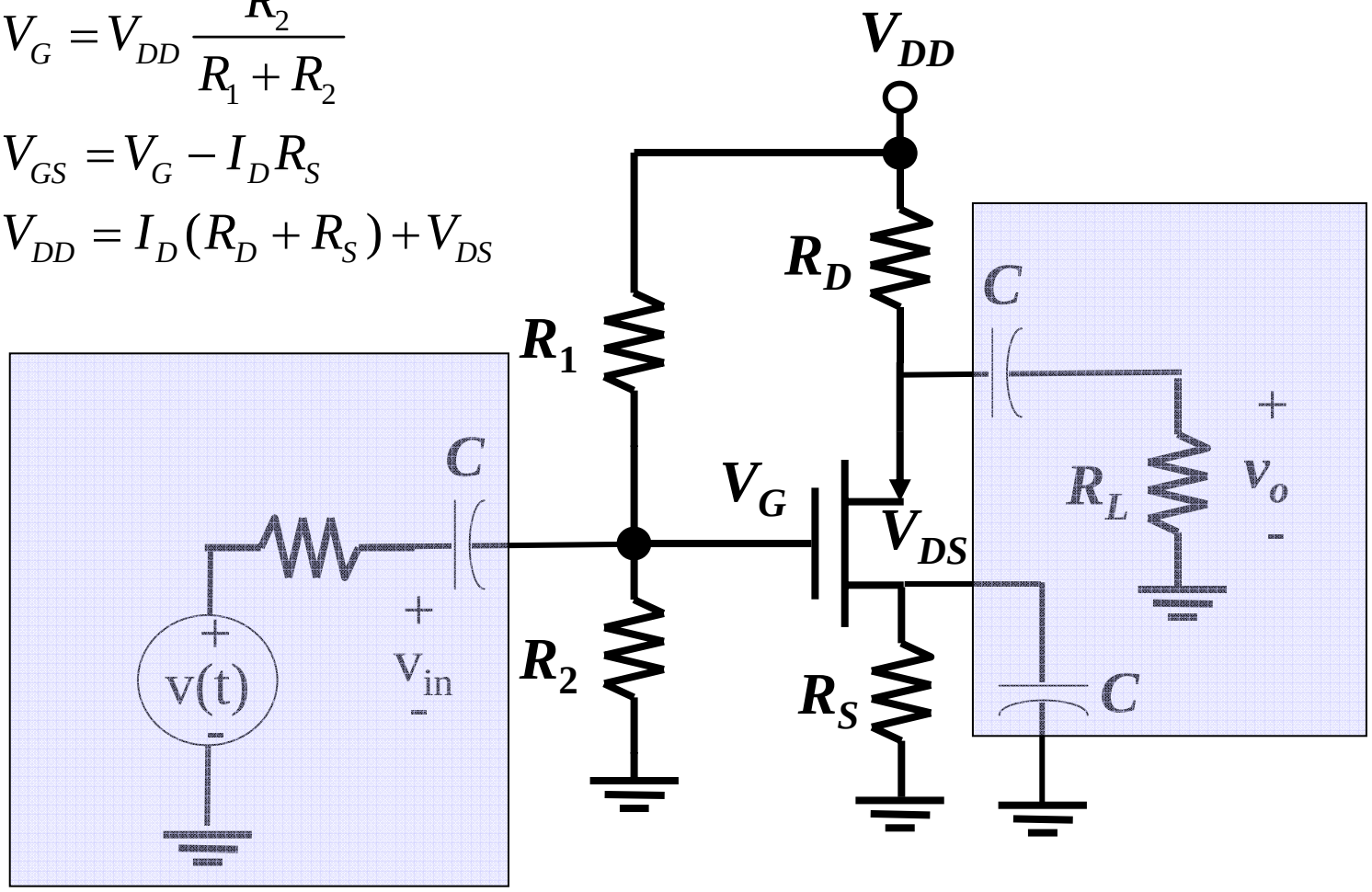


Step 1: find Q point

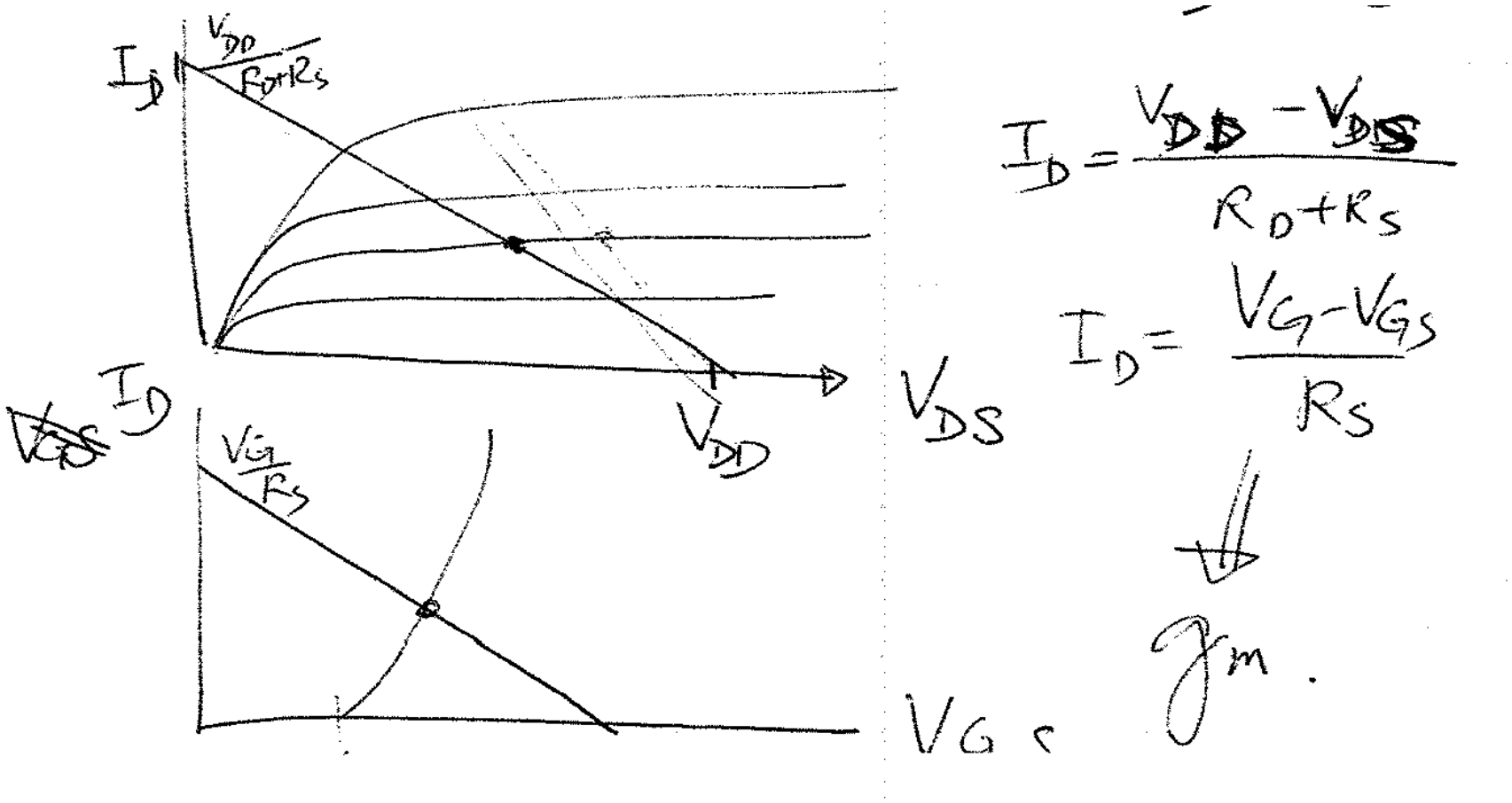
$$V_G = V_{DD}\frac{R_2}{R_1 + R_2}$$

$$V_{GS} = V_G - I_D R_S$$

$$V_{DD} = I_D(R_D + R_S) + V_{DS}$$

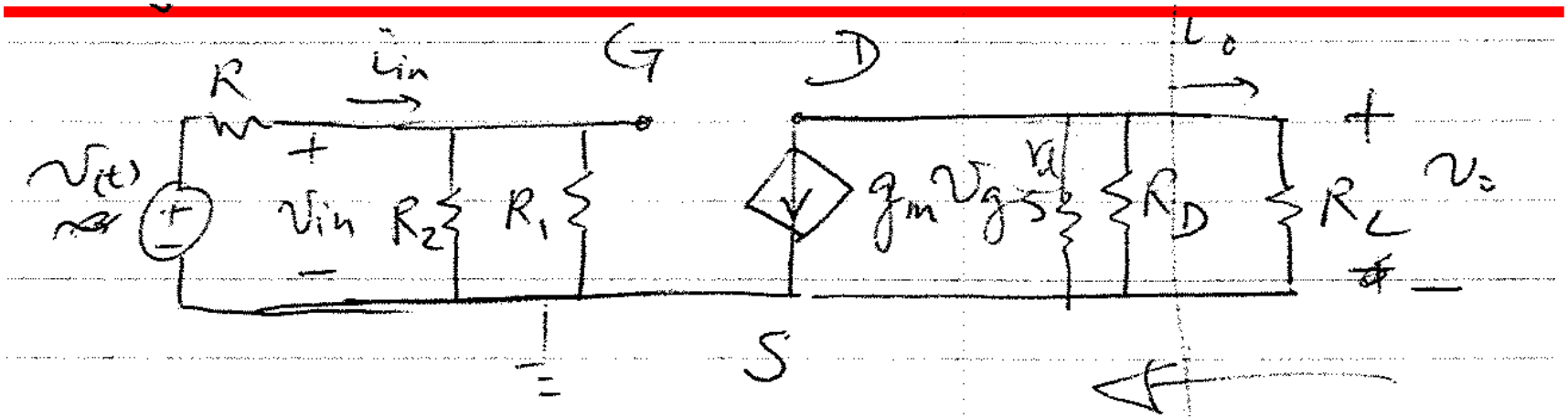


Load line



From load lines, we get I_D → and hence g_m and r_d

Small Signal Model



$$v_g = v_{in}, v_s = 0 \rightarrow v_{gs} = v_{in}$$

$$v_o = \frac{R_L R_D}{R_L + R_D}(-g_m v_{gs})$$

$$A_v = \frac{v_o}{v_{in}} = -g_m \frac{R_L R_D}{R_L + R_D}$$

$$R_{in} = \frac{v_{in}}{i_{in}} = \frac{R_1 R_2}{R_1 + R_2}$$

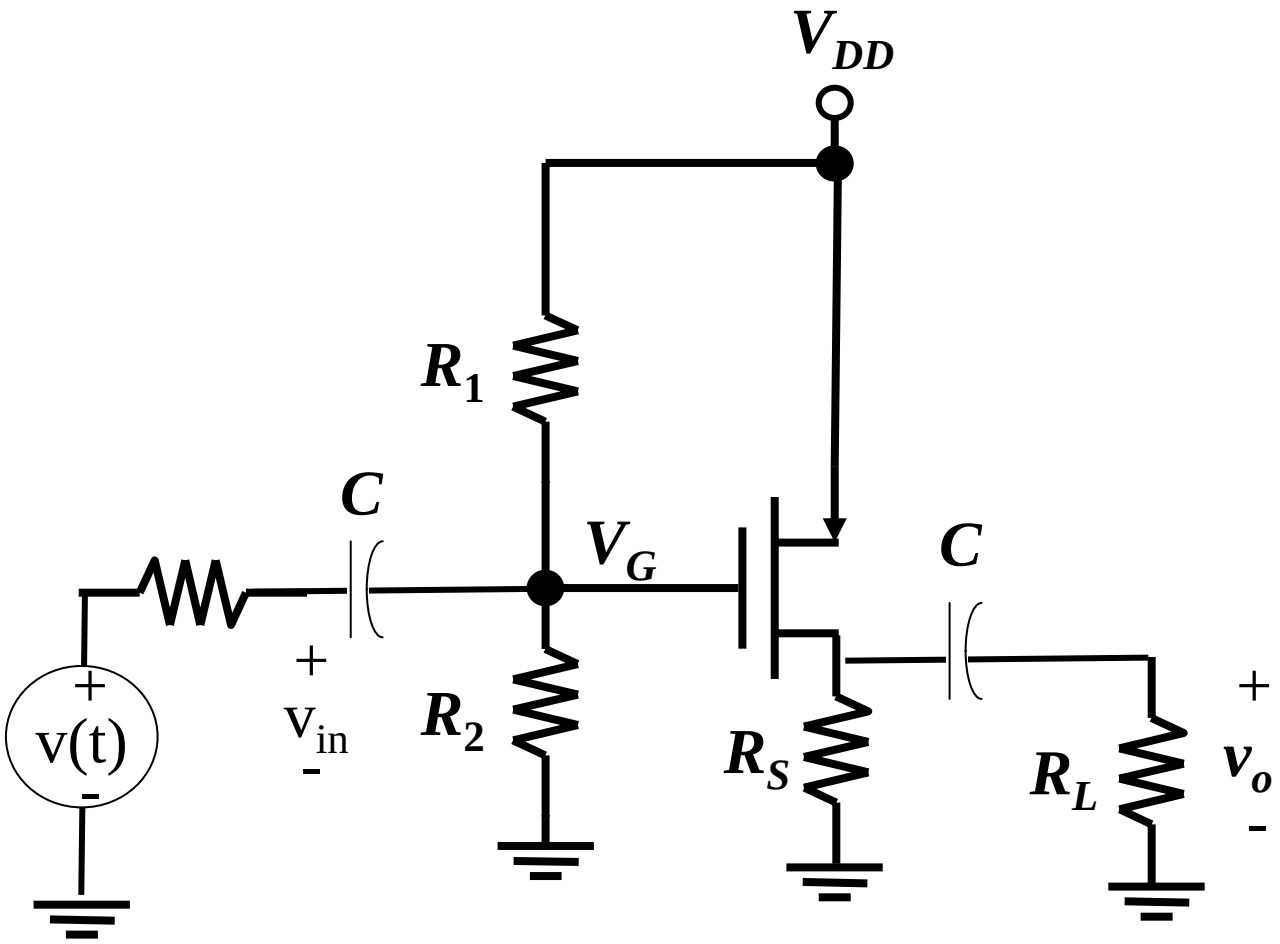
For output impedance R_{out}:

1. Turn off all independent sources.
2. Take away load impedance R_L

$$v_{in} = 0, v_{gs} = 0, g_m v_{gs} = 0$$

$$R_{out} = \frac{r_d R_D}{r_d + R_D}$$

Source Follower

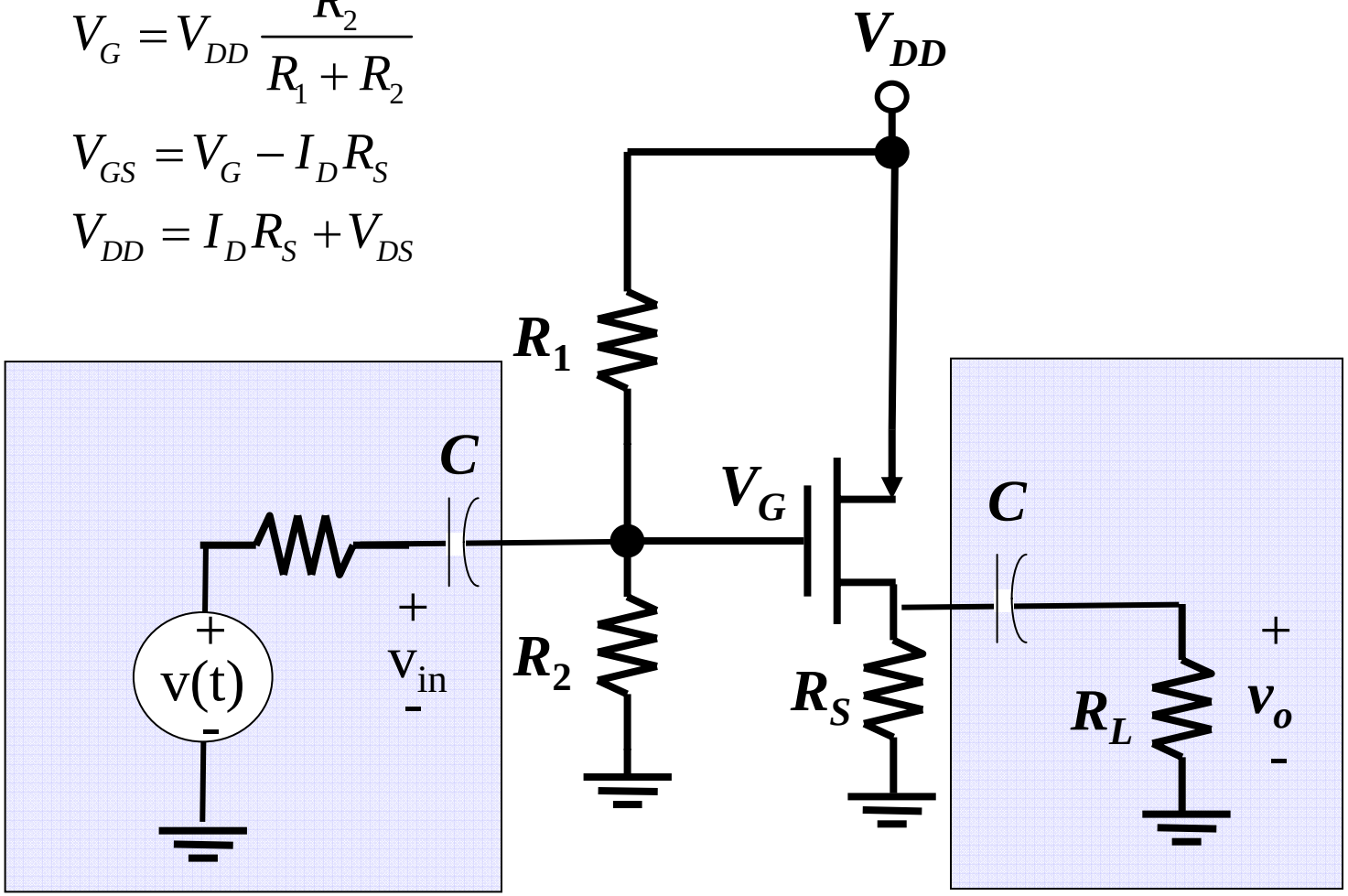


Step 1: find Q point

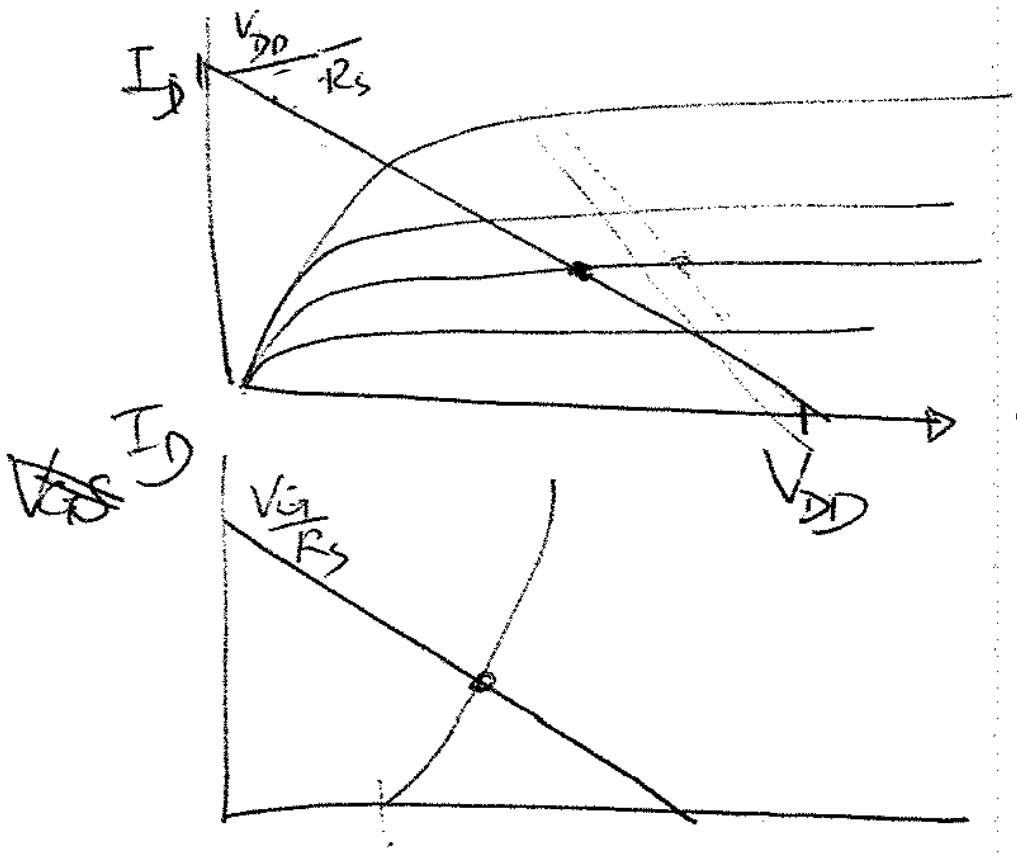
$$V_G = V_{DD}\frac{R_2}{R_1 + R_2}$$

$$V_{GS} = V_G - I_D R_S$$

$$V_{DD} = I_D R_S + V_{DS}$$



Load line



$$I_D = \frac{V_{DD} - V_{DS}}{R_S}$$

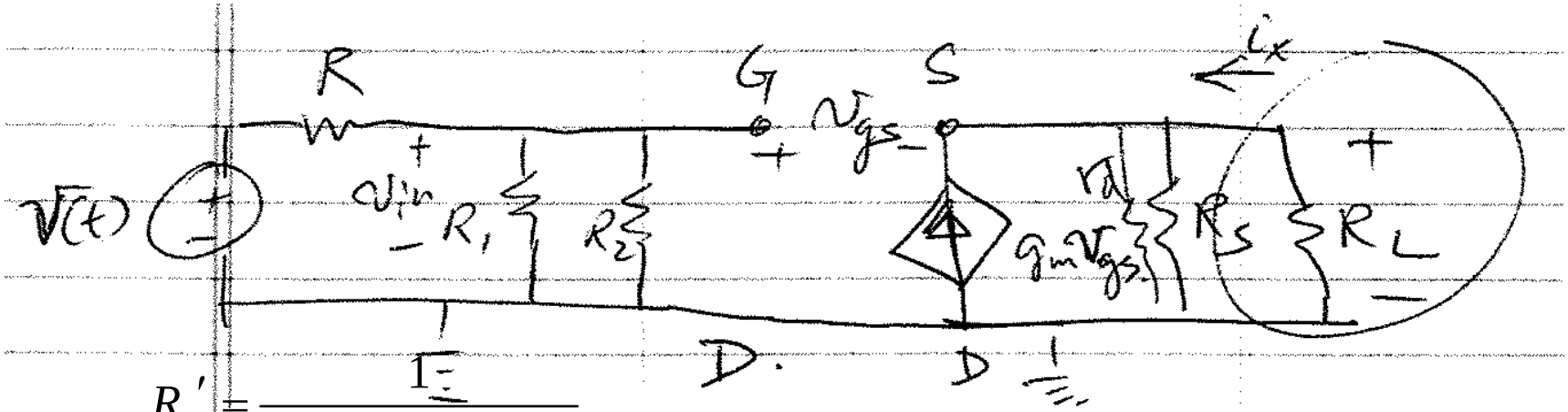
$$I_D = \frac{V_G - V_{GS}}{R_S}$$

$\Downarrow$

g_m.

From load lines, we get I_D → and hence g_m and r_d

Small Signal Model



$$R_L' = \frac{1}{r_d^{-1} + R_S^{-1} + R_L^{-1}}$$

$$v_{gs} = v_{in} - v_o$$

$$v_o = g_m v_{gs} R_L'$$

$$v_{in} = v_{gs}(1 + g_m R_L')$$

$$A_v = \frac{v_o}{v_{in}} = \frac{g_m R_L'}{1 + g_m R_L'}$$

$$R_{in} = \frac{v_{in}}{i_{in}} = \frac{R_1 R_2}{R_1 + R_2}$$

For output impedance R_{out}:

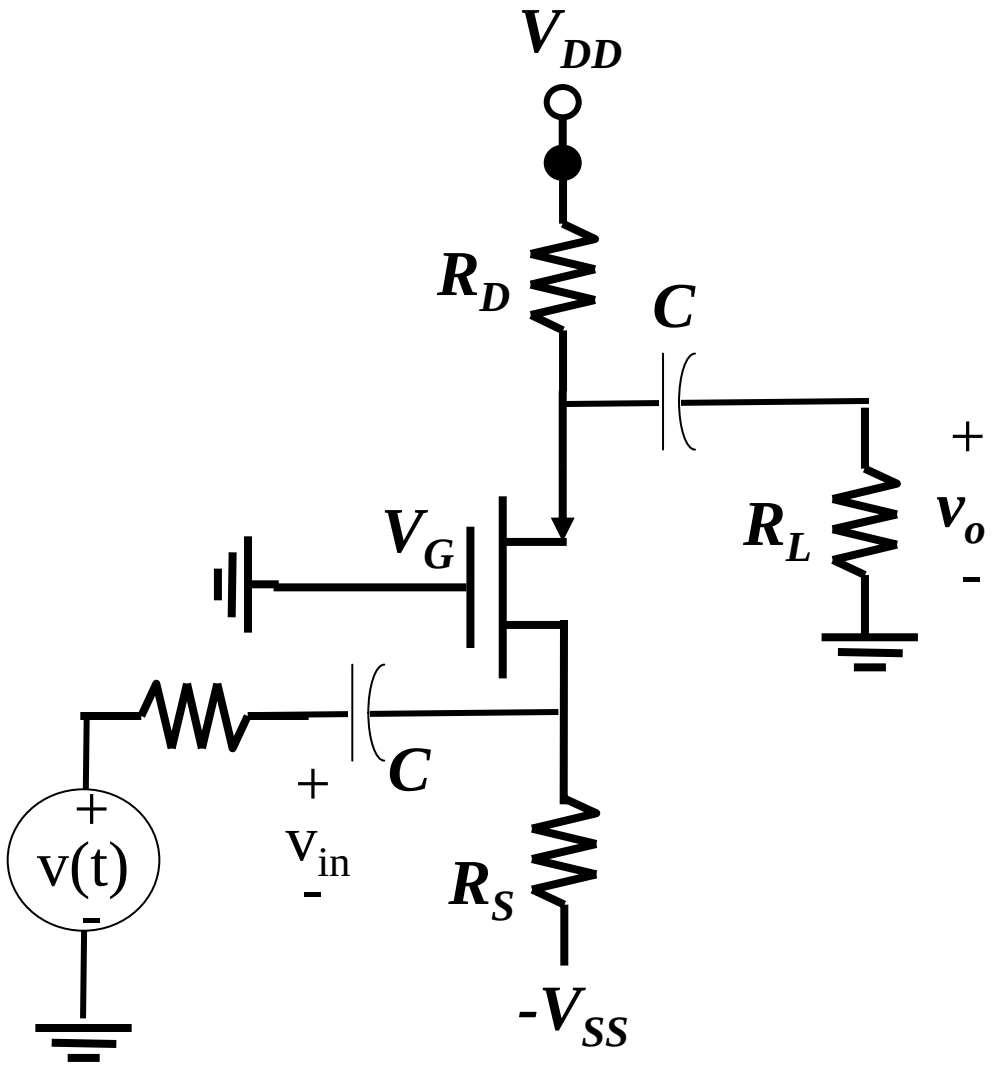
1. Turn off all independent sources.
2. Take away R_L
3. Add V_x and find i_x

$$v_x = v_s, v_g = 0, v_{gs} = -v_x$$

$$R_s' = \frac{r_d R_s}{r_d + R_s}, i_x = \frac{v_x}{R_s'} - g_m(-v_x) = v_x\left(R_s'^{-1} + g_m\right)$$

$$R_{out} = \frac{1}{g_m + r_d^{-1} + R_s^{-1}}$$

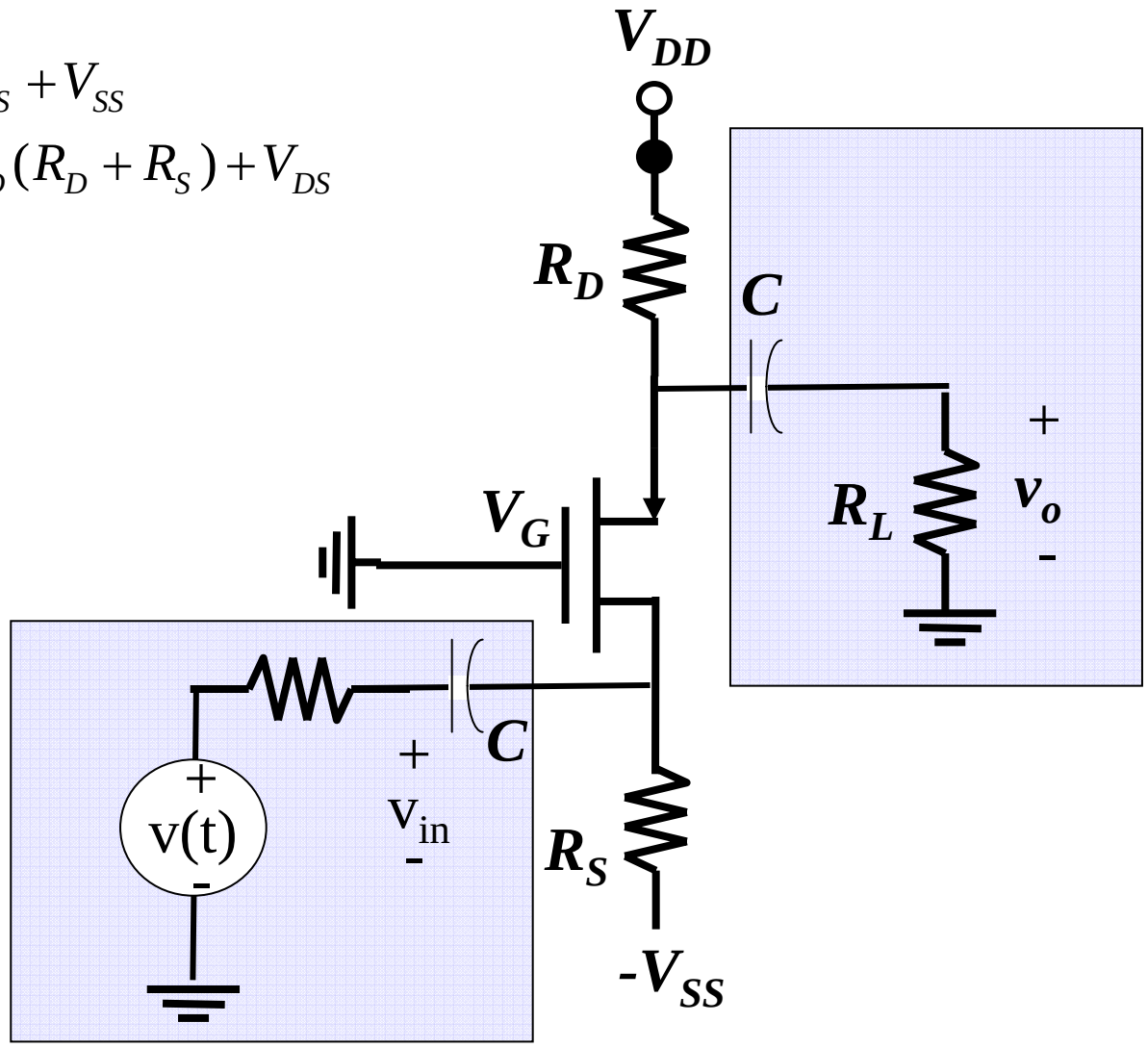
Common Gate Amplifier



Step 1: find Q point

$$V_{GS} = 0 - I_D R_S + V_{SS}$$

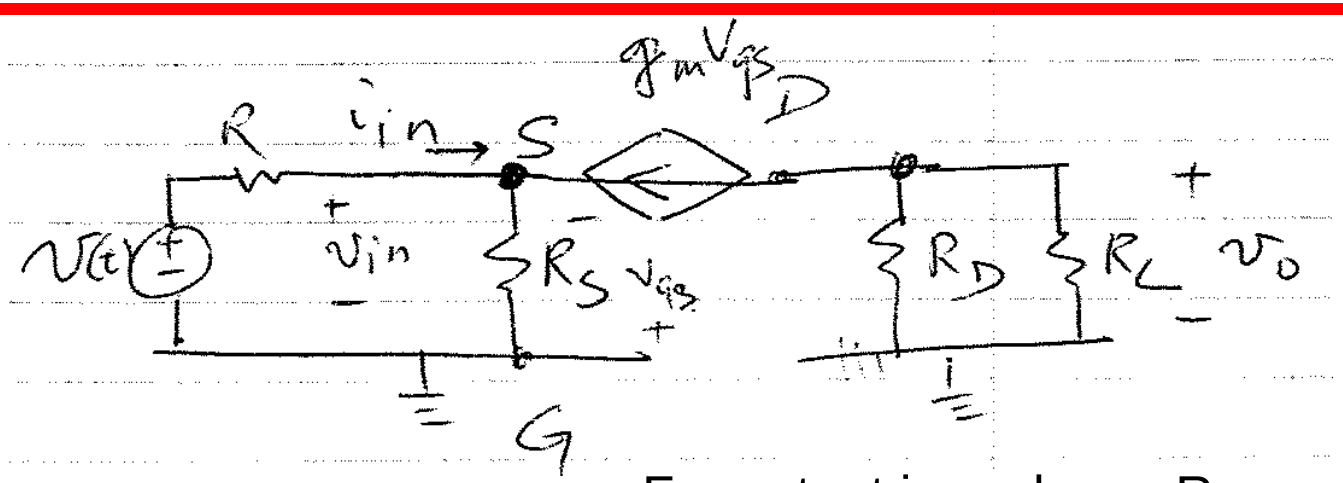
$$V_{DD} + V_{SS} = I_D (R_D + R_S) + V_{DS}$$



Load line

The only difference in all three circuits are the intercepts at the axes.
Again from load lines, we get I_D → and hence g_m and r_d

Small Signal Model



$$R_L' = \frac{1}{R_L^{-1} + R_D^{-1}}$$

$$v_{gs} = -v_{in}$$

$$v_o = -g_m v_{gs} R_L'$$

$$A_v = \frac{v_o}{v_{in}} = g_m R_L'$$

$$i_{in} = -(g_m v_{gs} + \frac{v_{gs}}{R_s})$$

$$R_{in} = \frac{v_{in}}{i_{in}} = \frac{1}{g_m + R_s^{-1}}$$

For output impedance R_{out}:

1. Turn off all independent sources.
2. Take away R_L
3. Add V_x and find i_x

$$R' = \frac{RR_s}{R + R_s}$$

$$i_x = \frac{v_x}{R_D} + g_m v_{gs}$$

$$v_{gs} = -g_m v_{gs} R', \ \ but \ \ g_m R' \neq 1 \therefore v_{gs} = 0$$

$$R_{out} = R_D$$

MOSFET Digital Circuits – Introduction

- Analog: signal amplitude is continuous with time.
- Digital: signal amplitude is represented by a restricted set of discrete numbers.
  - Binary: only two values are allowed to represent the signal: High or low (i.e. logic 1 or 0).
- Digital word:
  - Each binary digit is called a bit
  - A series of bits form a word
    - Byte is a word consisting of 8-bits
- Advantages of digital signal
  - Digital signal is more resilient to noise→ can more easily differentiate high (1) and low (0)
- Transmission
  - Parallel transmission over a bus containing n wires.
    - Faster but short distance (internal to a computer or chip)
  - Serial transmission (transmit bits sequentially)
    - Longer distance

Analog *vs.* Digital Signals

- **Most** (but not all) **observables are analog**

  think of analog vs. digital watches

but the most convenient way to represent & transmit information electronically is to use digital signals

think of telephony

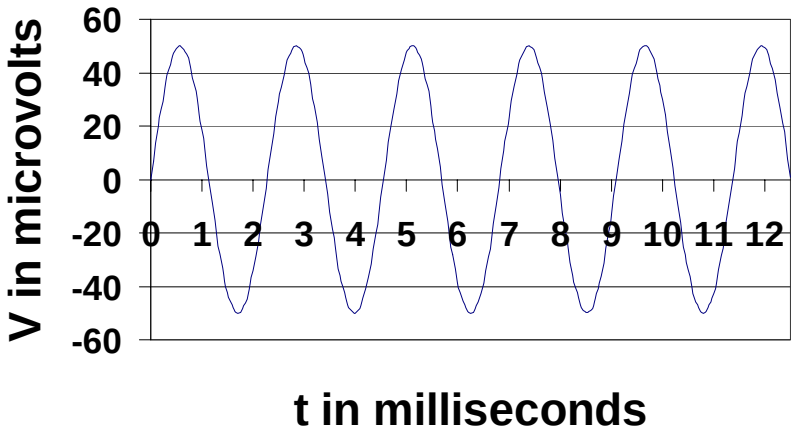
→ Analog-to-digital (A/D) & digital-to-analog (D/A) conversion is essential (and nothing new)

think of a piano keyboard

Analog Signal Example: Microphone Voltage

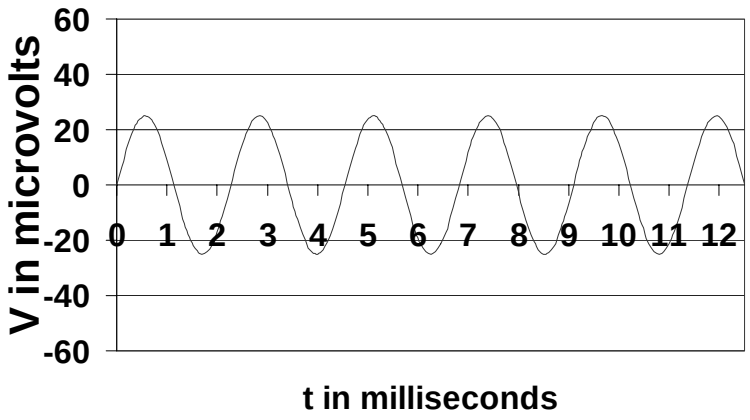
Voltage with normal piano key stroke

50 microvolt 440 Hz signal

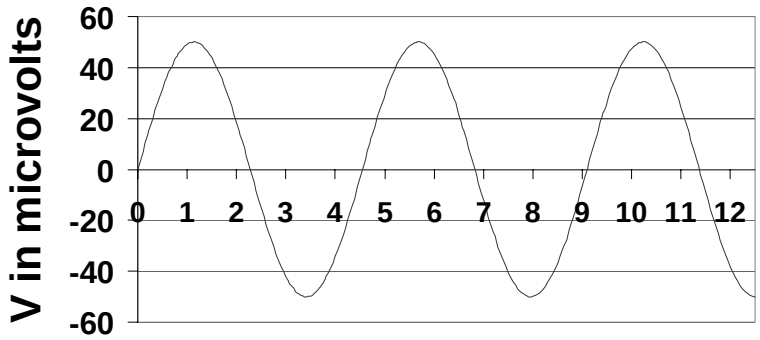


Voltage with soft pedal applied

25 microvolt 440 Hz signal



50 microvolt 220 Hz signal



Analog signal representing piano key A, below middle C (220 Hz)

Digital Signal Representations

Binary numbers can be used to represent any quantity.

We generally have to agree on some sort of "code", and the dynamic range of the signal in order to know the form and the number of binary digits ("bits") required.

Example 1: Voltage signal with maximum value 2 Volts

- Binary two (**10**) could represent a 2 Volt signal.
- To encode the signal to an accuracy of 1 part in 64 (1.5% precision), 6 binary digits ("bits") are needed

Example 2: Sine wave signal of known frequency and maximum amplitude 50 μV; 1 μV "resolution" needed.

Decimal Numbers: Base 10

Digits: 0, 1, 2, 3, 4, 5, 6, 7, 8, 9

Example:

$3271 = (3 \times 10^3) + (2 \times 10^2) + (7 \times 10^1) + (1 \times 10^0)$

This is a four-digit number. The left hand most number (3 in this example) is often referred as the most significant number and the right most the least significant number (1 in this example).

Numbers: positional notation

- Number Base B $\Rightarrow$ B symbols per digit:
  - Base 10 (Decimal): 0, 1, 2, 3, 4, 5, 6, 7, 8, 9
  - Base 2 (Binary): 0, 1
- Number representation:
  - $d_{31}d_{30}$ ... d_1d_0 is a 32 digit number
  - value = $d_{31} \times B^{31} + d_{30} \times B^{30} + ... + d_1 \times B^1 + d_0 \times B^0$
- Binary: 0,1 (In binary digits called "bits")

  11010 $= 1\times2^4 + 1\times2^3 + 0\times2^2 + 1\times2^1 + 0\times2^0$

  $= 16 + 8 + 2$

  $= 26$
  - Here 5 digit binary # turns into a 2 digit decimal #

Hexadecimal Numbers: Base 16

- Hexadecimal:
  0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F
  - –Normal digits + 6 more from the alphabet
- Conversion: Binary⇔Hex
  - –1 hex digit represents 16 decimal values
  - –4 binary digits represent 16 decimal values
  - ⇒1 hex digit replaces 4 binary digits

Digital Signal Representations

Binary numbers can be used to represent any quantity.

We generally have to agree on some sort of "code", and the dynamic range of the signal in order to know the form and the number of binary digits ("bits") required.

Example 1: Voltage signal with maximum value 2 V and minimum of 0 V.

- Binary two (**10**) could represent a 2 Volt signal.
- To encode the signal to an accuracy of 1 part in 64 (1.5% precision), 6 binary digits ("bits") are needed

Example 2: Sine wave signal of known frequency and maximum amplitude 50 μV; 1 μV "resolution" needed.

Resolution

- The size of the smallest element that can be separated from neighboring elements. The term is used to describe imaging systems, the frequency separation achieved by spectrometers, and so on.

Decimal-Binary Conversion

- Decimal to Binary
  - Repeated Division By 2
    - Consider the number 2671.
  - Subtraction – if you know your 2^N values by heart.
- Binary to Decimal conversion

$$110001_2 = 1x2^5 + 1x2^4 + 0x2^3 + 0x2^2 + 0x2^1 + 1x2^0$$

$$= 32_{10} + 16_{10} + 1_{10}$$

$$= 49_{10}$$

$$= 4x10^1 + 9x10^0$$

Example 2 (continued)

Possible digital representation for the sine wave signal:

Analog representation: Amplitude in μV	**Digital representation:** Binary number
1	000001
2	000010
3	000011
4	000100
5	000101
8	001000
16	010000
32	100000
50	**110010**
63	111111

Binary Representation

- N bit can represent 2^N values: typically from 0 to 2^N-1
  - 3-bit word can represent 8 values: e.g. 0, 1, 2, 3, 4, 5, 6, 7
- Conversion
  - Integer to binary
  - Fraction to binary ($13.5_{10}=1101.1_2$ and $0.392_{10}=0.011001_2$)
- Octal and hexadecimal

- Logic gates
  - Combine several logic variable inputs to produce a logic variable output
- Memory
  - Memoryless: output at a given instant depends the input values of that instant.
  - Momory: output depends on previous and present input values.

Boolean algebras

- Algebraic structures
  - "capture the essence" of the logical operations AND, OR and NOT
  - corresponding set for theoretic operations intersection, union and complement
  - named after George Boole, an English mathematician at University College Cork, who first defined them as part of a system of logic in the mid 19th century.
  - Boolean algebra was an attempt to use algebraic techniques to deal with expressions in the propositional calculus.
  - Today, Boolean algebras find many applications in electronic design. They were first applied to switching by Claude Shannon in the 20th century.

Boolean algebras

- The operators of Boolean algebra may be represented in various ways. Often they are simply written as AND, OR and NOT.
- In describing circuits, NAND (NOT AND), NOR (NOT OR) and XOR (eXclusive OR) may also be used.
- Mathematicians often use + for OR and · for AND (since in some ways those operations are analogous to addition and multiplication in other algebraic structures) and represent NOT by a line drawn above the expression being negated.

Boolean Algebra

- NOT operation (inverter)

$$A \bullet \overline{A} = 0$$

$$A + \overline{A} = 1$$

- AND operation

$$A \bullet A = A$$

$$A \bullet 1 = A$$

$$A \bullet 0 = 0$$

$$A \bullet B = B \bullet A$$

$$(A \bullet B) \bullet C = A \bullet (B \bullet C)$$

- OR operation

$$A + A = A$$

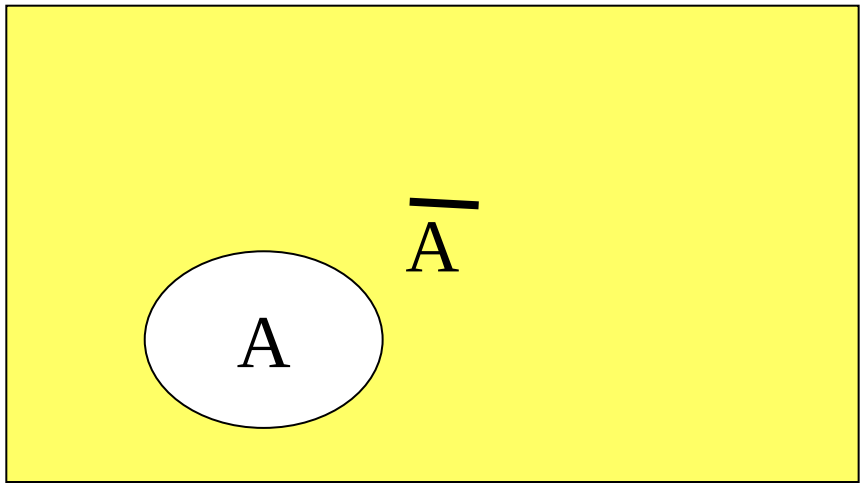
$$A + 1 = 1$$

$$A + 0 = A$$

$$A + B = B + A$$

$$(A + B) + C = A + (B + C)$$

Graphic Representation

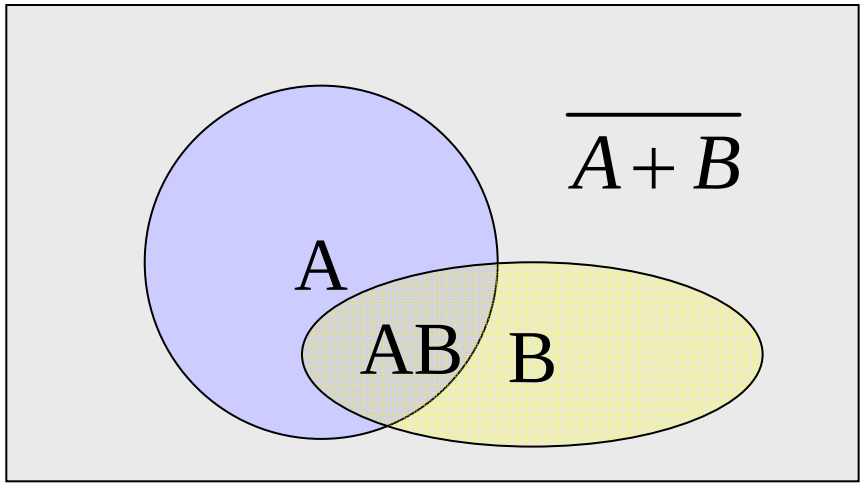


$$A \bullet \overline{A} = 0$$

$$A + \overline{A} = 1$$

Full square = complete set =1
Yellow part = NOT(A) =$\overline{A}$
White circle = A

Graphic Representation



$$A \oplus B = A\overline{B} + \overline{A}B = (A+B)\bullet(\overline{A}+\overline{B}) = \overline{A\bullet B + \overline{A+B}}$$

Exclusive OR=yellow and blue part – intersection/overlap part

=exactly when only one of the input is true

Boolean Algebra

- Distributive Property

$$A \bullet (B + C) = A \bullet B + A \bullet C$$

$$(A + B) \bullet C = (A + B) \bullet (A + C)$$

- De Morgan's laws

$$\overline{A + B} = \overline{A} \bullet \overline{B}$$

$$\overline{A \bullet B} = \overline{A} + \overline{B}$$

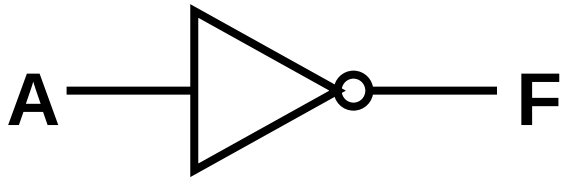
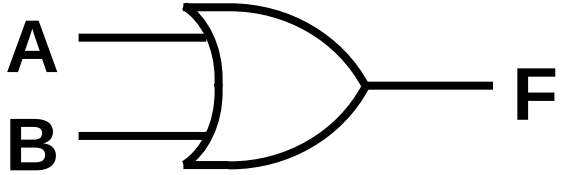
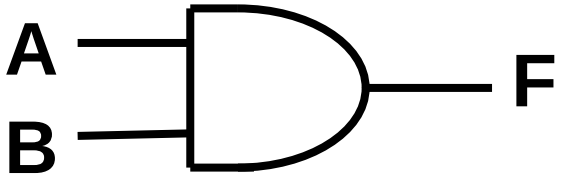
- An excellent web site to visit
  - http://en.wikipedia.org/wiki/Boolean_algebra

Examples

$$F = A \bullet \overline{B} \bullet C + A \bullet B \bullet C + (C+D) \bullet (\overline{D}+E)$$

$$F = C \bullet (A+\overline{D}+E) + D \bullet E$$

Logic Functions, Symbols, & Notation

NAME	SYMBOL	NOTATION	TRUTH TABLE
"NOT"		$F = \overline{A}$	
"OR"		F = A+B	
"AND"		F = A•B	

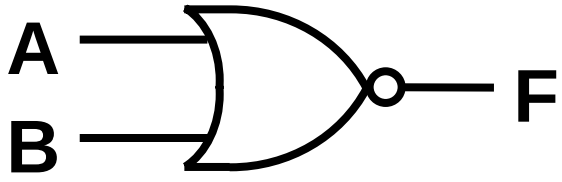
A	F
0	1
1	0

A	B	F
0	0	0
0	1	1
1	0	1
1	1	1

A	B	F
0	0	0
0	1	0
1	0	0
1	1	1

Logic Functions, Symbols, & Notation 2

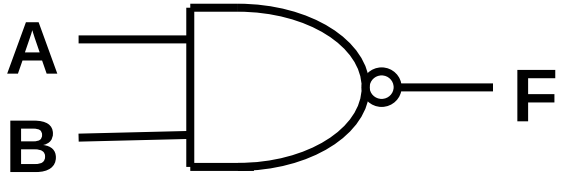
"NOR"



$F = \overline{A+B}$

A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

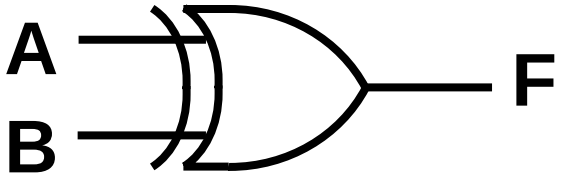
"NAND"



$F = \overline{A \cdot B}$

A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

"XOR"
(exclusive OR)

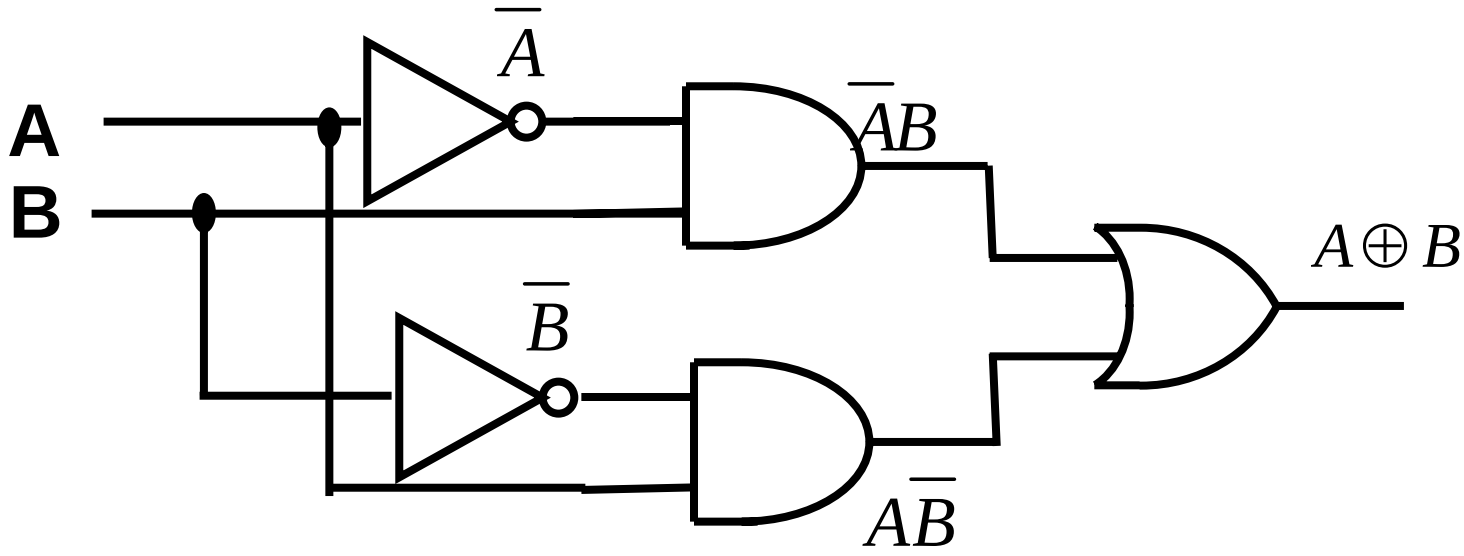


$F = A \oplus B$

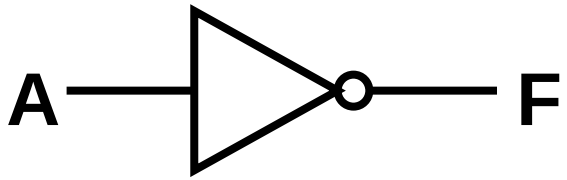
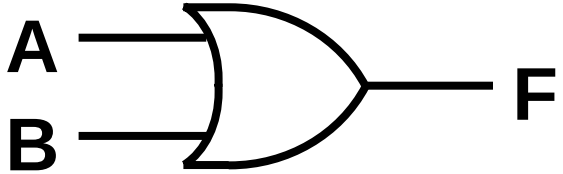
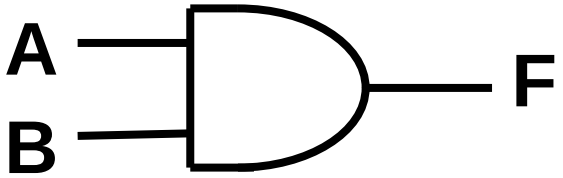
A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

Circuit Realization

$$A \oplus B = A\overline{B} + \overline{A}B = (A + B)\bullet(\overline{A} + \overline{B}) = \overline{\overline{A\bullet B} + \overline{A + B}}$$



Logic Functions, Symbols, & Notation

NAME	SYMBOL	NOTATION	TRUTH TABLE
"NOT"		$F = \overline{A}$	
"OR"		F = A+B	
"AND"		F = A•B	

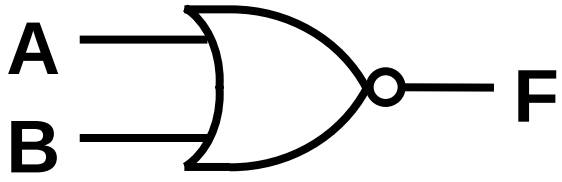
A	F
0	1
1	0

A	B	F
0	0	0
0	1	1
1	0	1
1	1	1

A	B	F
0	0	0
0	1	0
1	0	0
1	1	1

Logic Functions, Symbols, & Notation 2

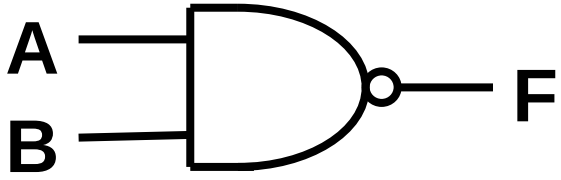
"NOR"



$F = \overline{A+B}$

A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

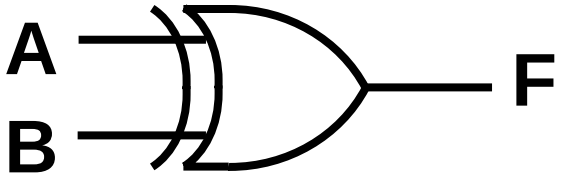
"NAND"



$F = \overline{A \cdot B}$

A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

"XOR"
(exclusive OR)



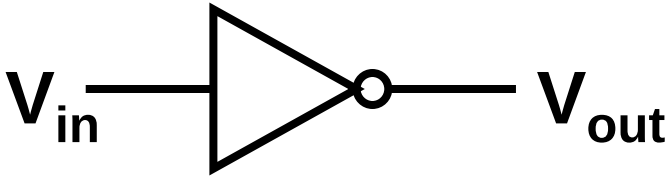
$F = A \oplus B$

A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

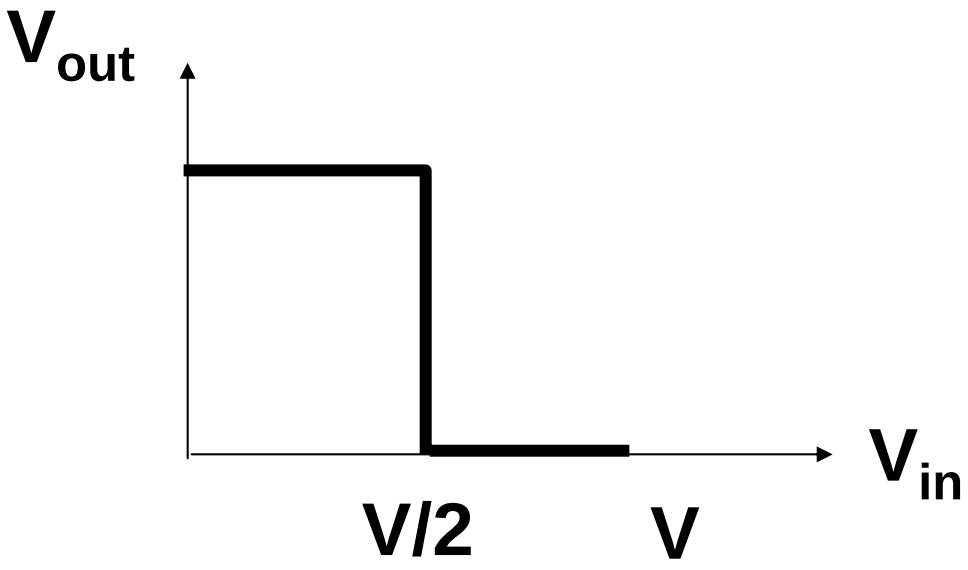
Fan in/Fan out

- Complex digital operations are formed with a variety of gates interconnected to yield the desired logic function.
- Sometimes a number of inputs are connected to one gate input and output of a gate may be connected to a number of gates.
- Fan-in: the maximum number of logic gates that can be connected at the input of a gate without altering its performance.
- Fan-out: the maximum number of logic gates that can be connected to the output of a gate without altering its performance.
- Typical fan-in and fan-out numbers are 3.

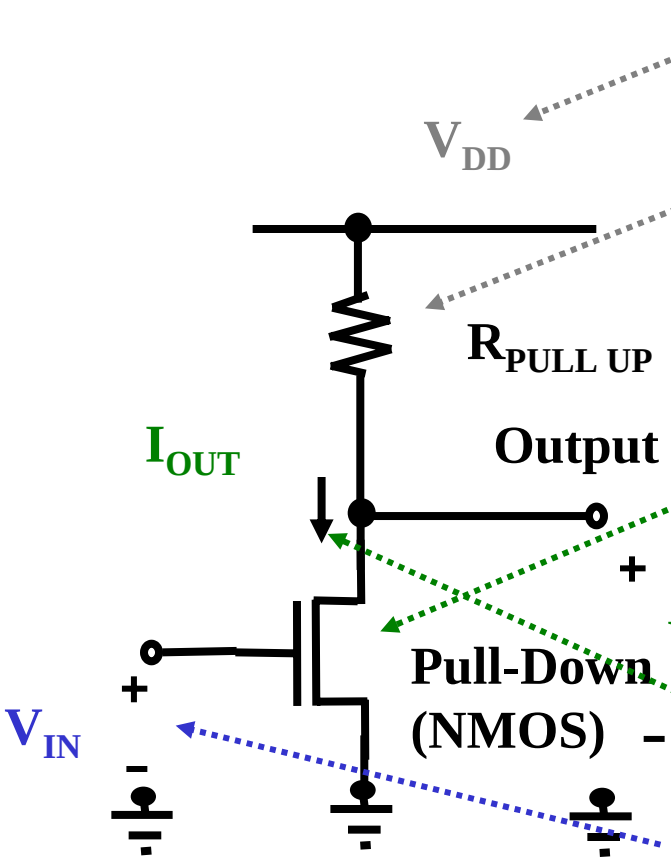
Inverter = NOT Gate



Ideal Transfer Characteristics



Terminology for a Logic Circuit



V_{DD} = Power supply voltage (D is from Drain) we do not draw the symbol.

Pull-Up Network = Set of devices used to carry current from the power supply to the output node to charge the output node to the power supply voltage.

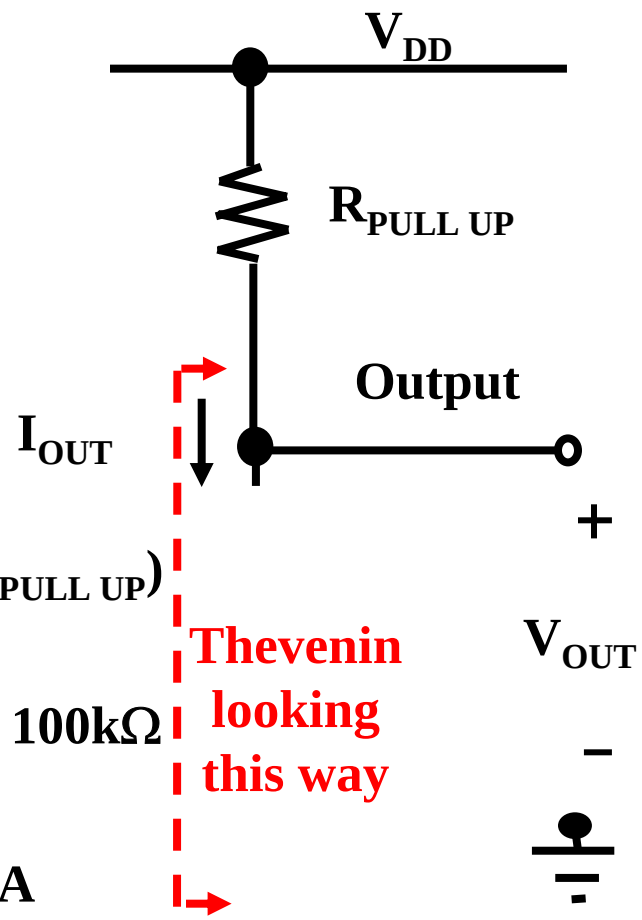
Pull-Down Network = Set of devices used to carry current from the output node to ground to discharge the output node to ground.

I_{OUT} = Current for the device under study.

V_{TD} = Threshold Voltage value of V_{IN} at which the Pull-Down (NMOS transistor) begins to conduct.

$V_{OUT-SAT-D}$ = Value of V_{OUT} beyond which the current I_{OUT-D} saturates at the (drain) current saturation value $I_{OUT-SAT-D}$.

Thevenin Model For Pull-Up Device



$V_{THEVENIN} = V_{DD}$

$I_{OUT\ SHORT\ CIRCUIT} = (V_{DD}/R_{PULL\ UP})$

Example:

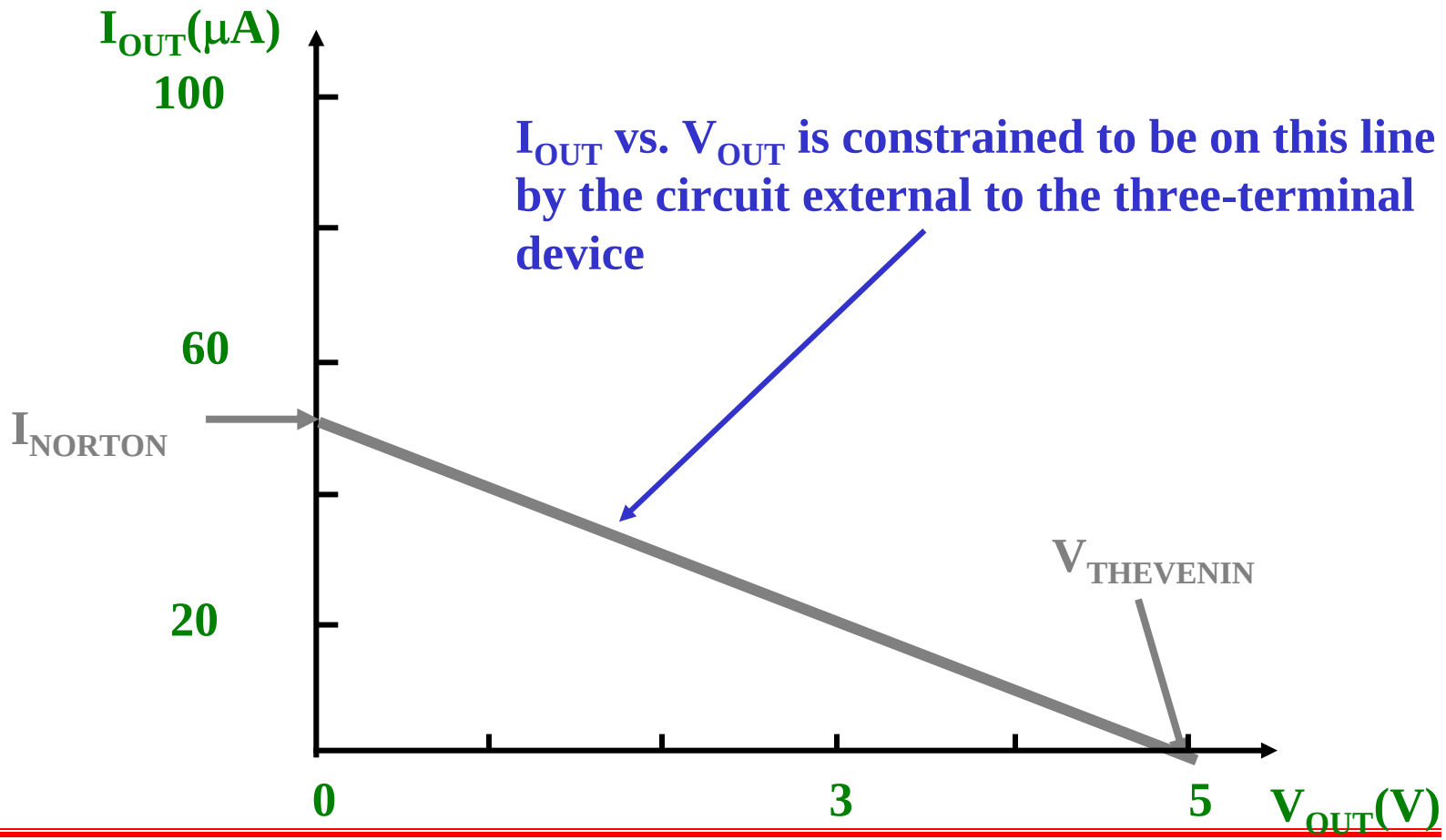
$V_{DD} = 5V$ and $R_{PULL\ UP} = 100k\Omega$

$V_{THEVENIN} = 5V$

$I_{OUT\ SHORT\ CIRCUIT} = 50\ \mu A$

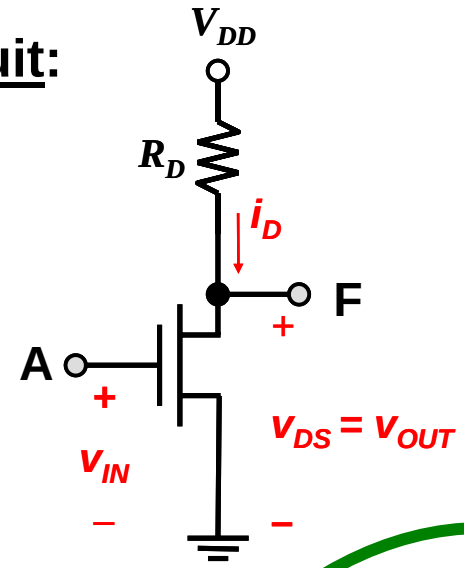
Load Line For Pull-Up Device

I_{OUT} vs. V_{OUT}
For the Pull-Up Resistor and V_{DD}

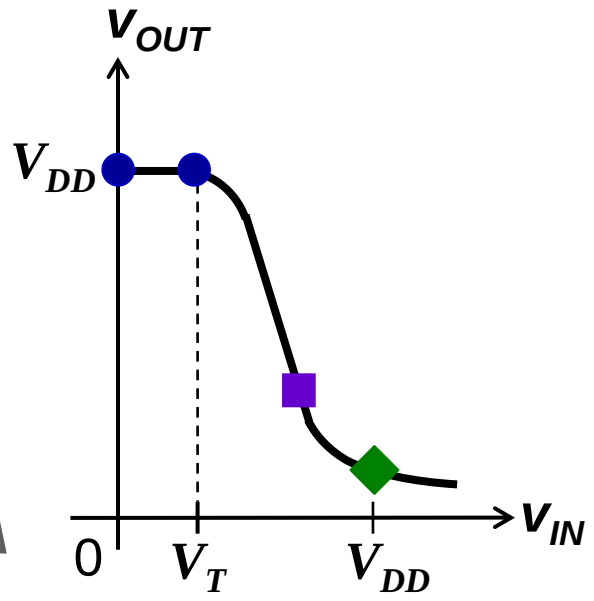


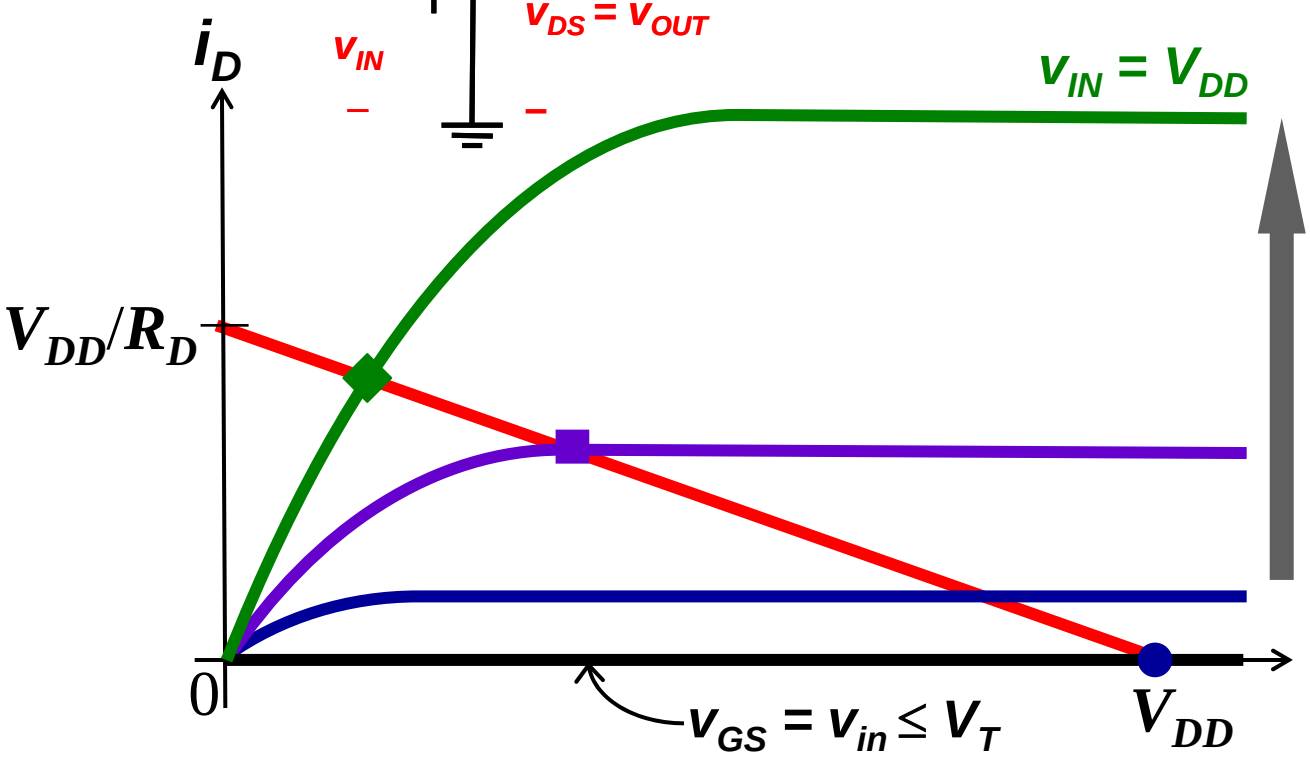
NMOS Resistor Pull-Up

Circuit:



Voltage-Transfer Characteristic





A	F
0	1
1	0

Disadvantages of NMOS Logic Gates

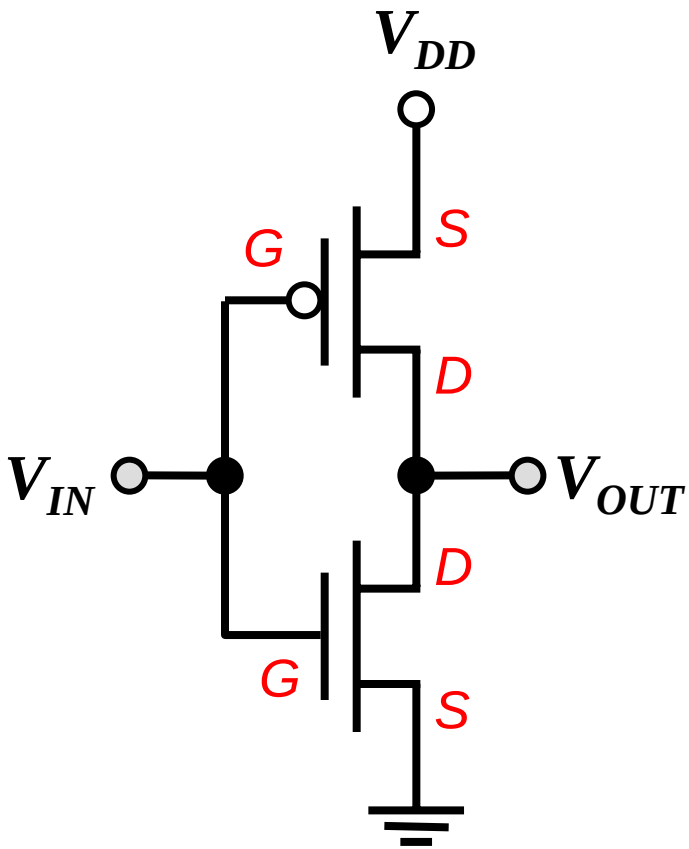
- Large values of $\boldsymbol{R_D}$ are required in order to
  - achieve a low value of V_{OL}
  - keep power consumption low

  → Large resistors are needed, but these take up a lot of space.

    - One solution is to replace the resistor with an NMOSFET that is always on.

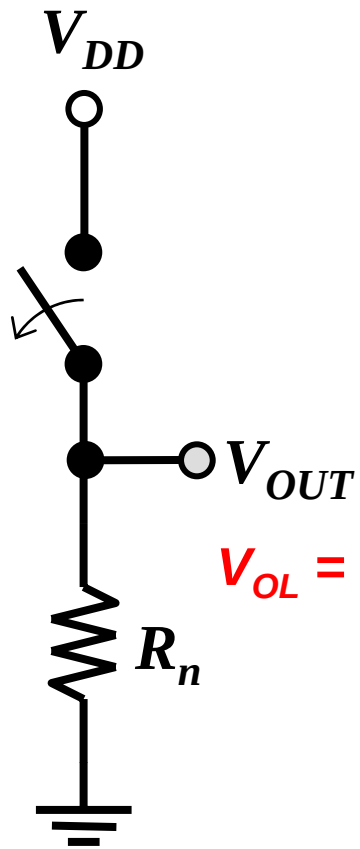
The CMOS Inverter: Intuitive Perspective

CIRCUIT



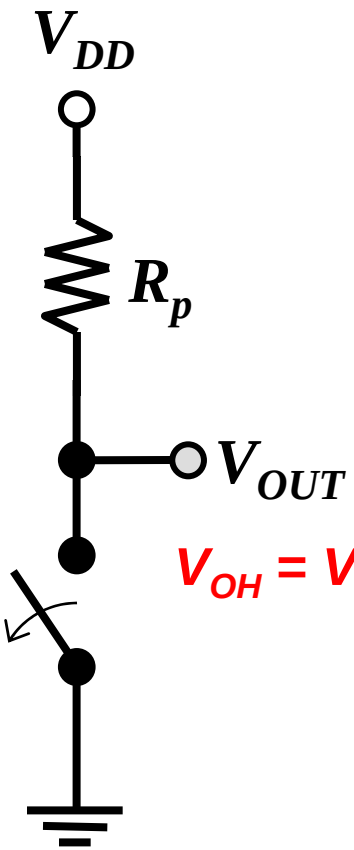
Low static power consumption, since one MOSFET is always off in steady state

SWITCH MODELS



$V_{OL} = 0$ V

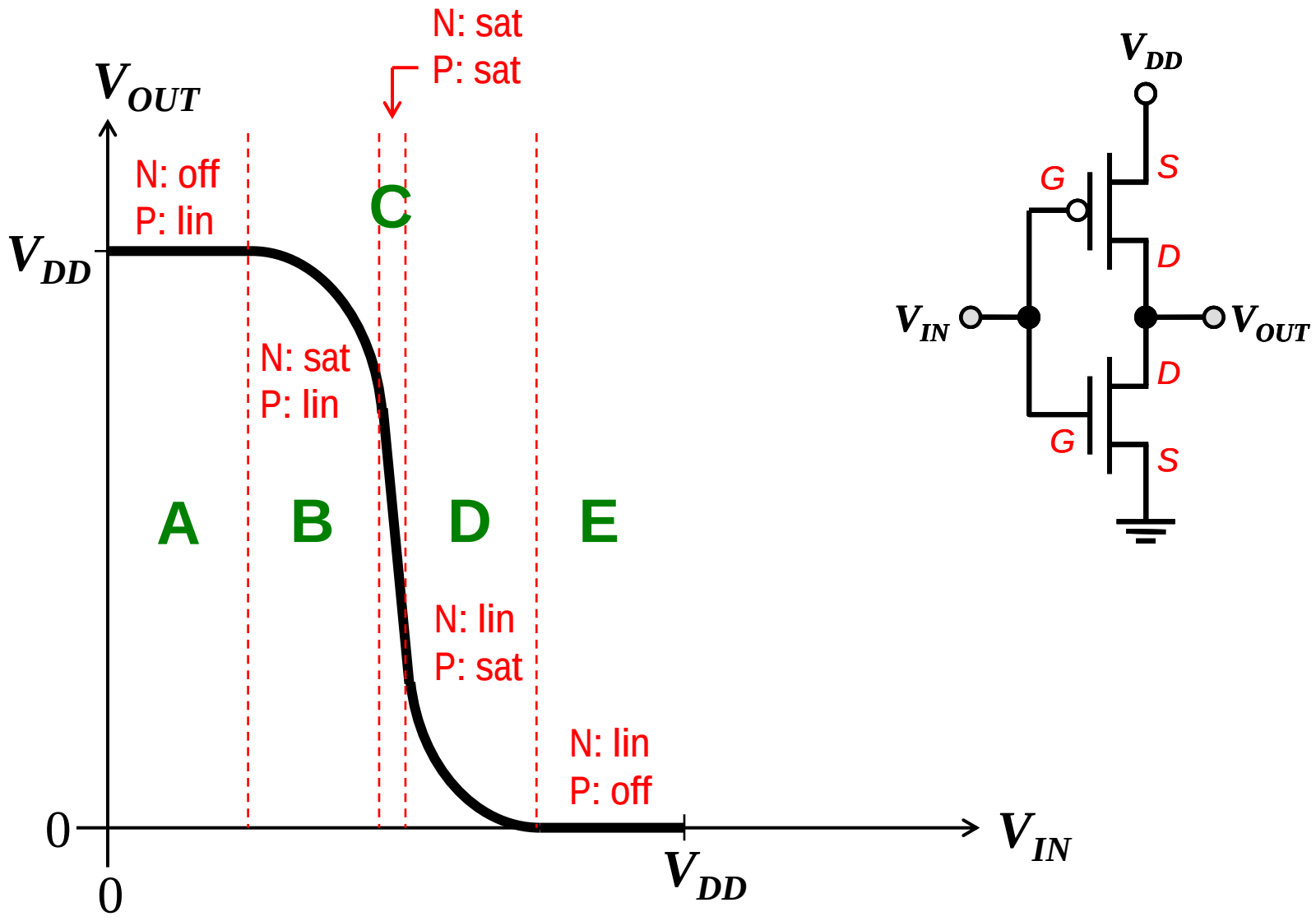
$V_{IN} = V_{DD}$



$V_{OH} = V_{DD}$

$V_{IN} = 0$ V

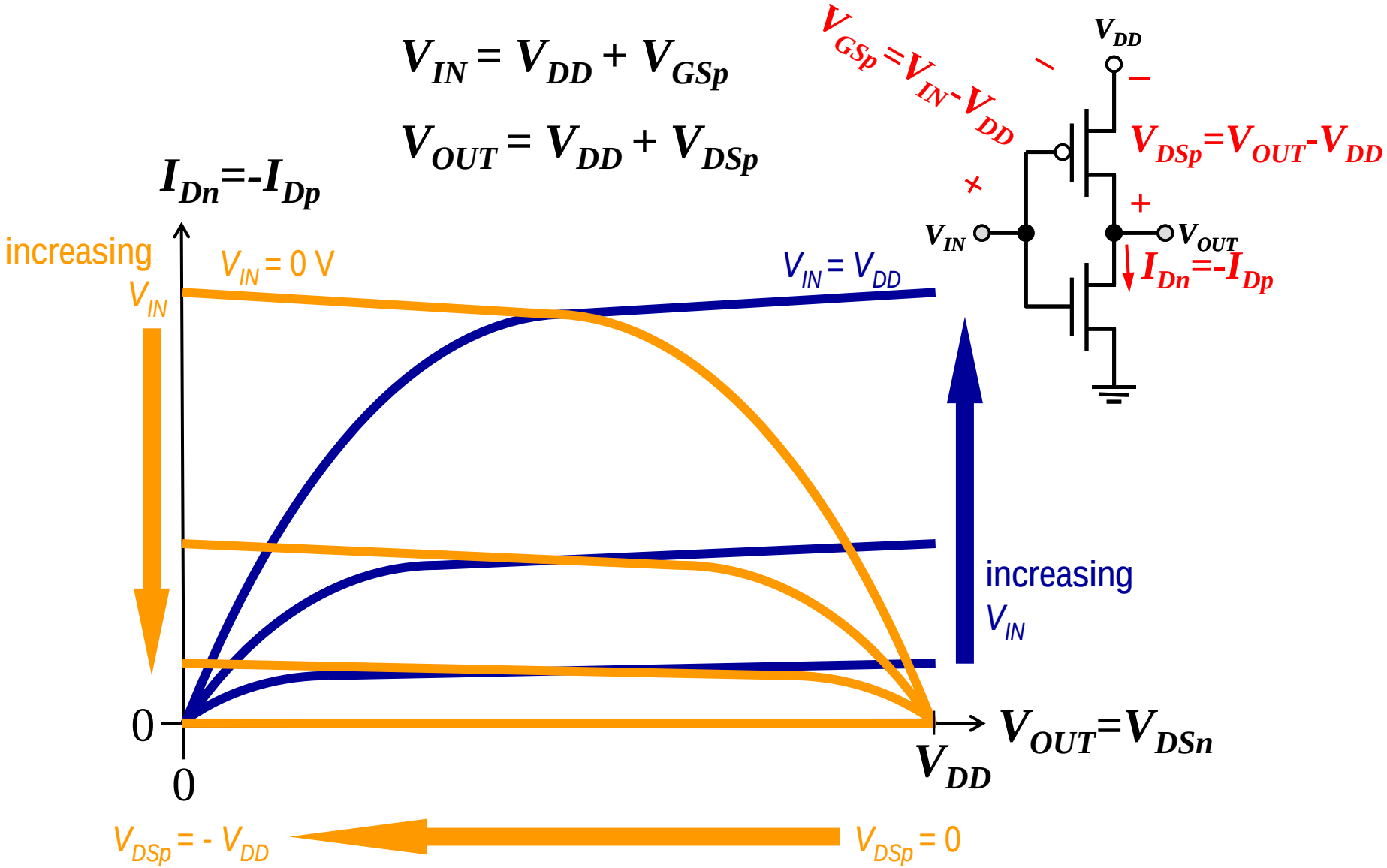
CMOS Inverter Voltage Transfer Characteristic



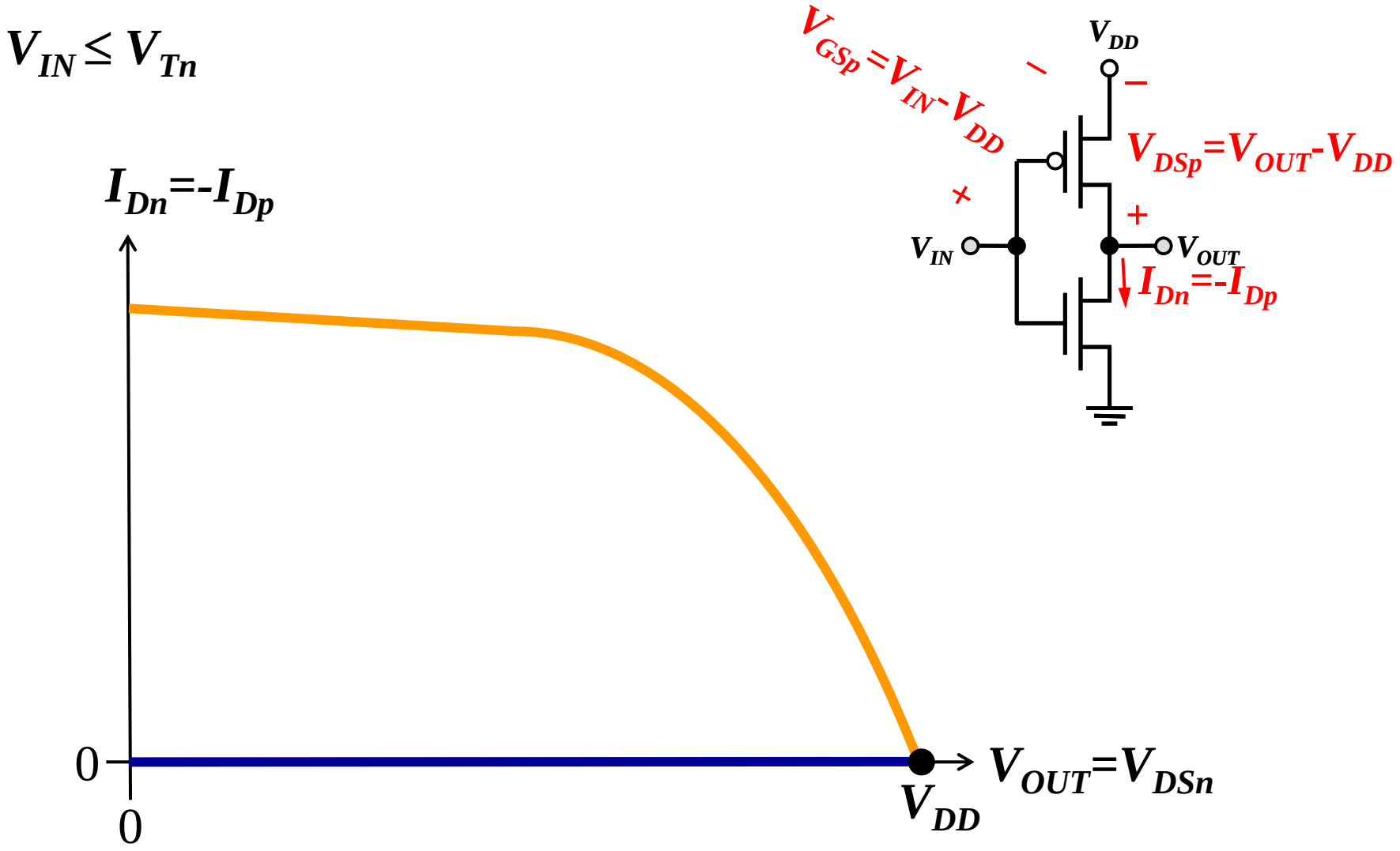
CMOS Inverter Load-Line Analysis

$$V_{IN} = V_{DD} + V_{GSp}$$

$$V_{OUT} = V_{DD} + V_{DSp}$$

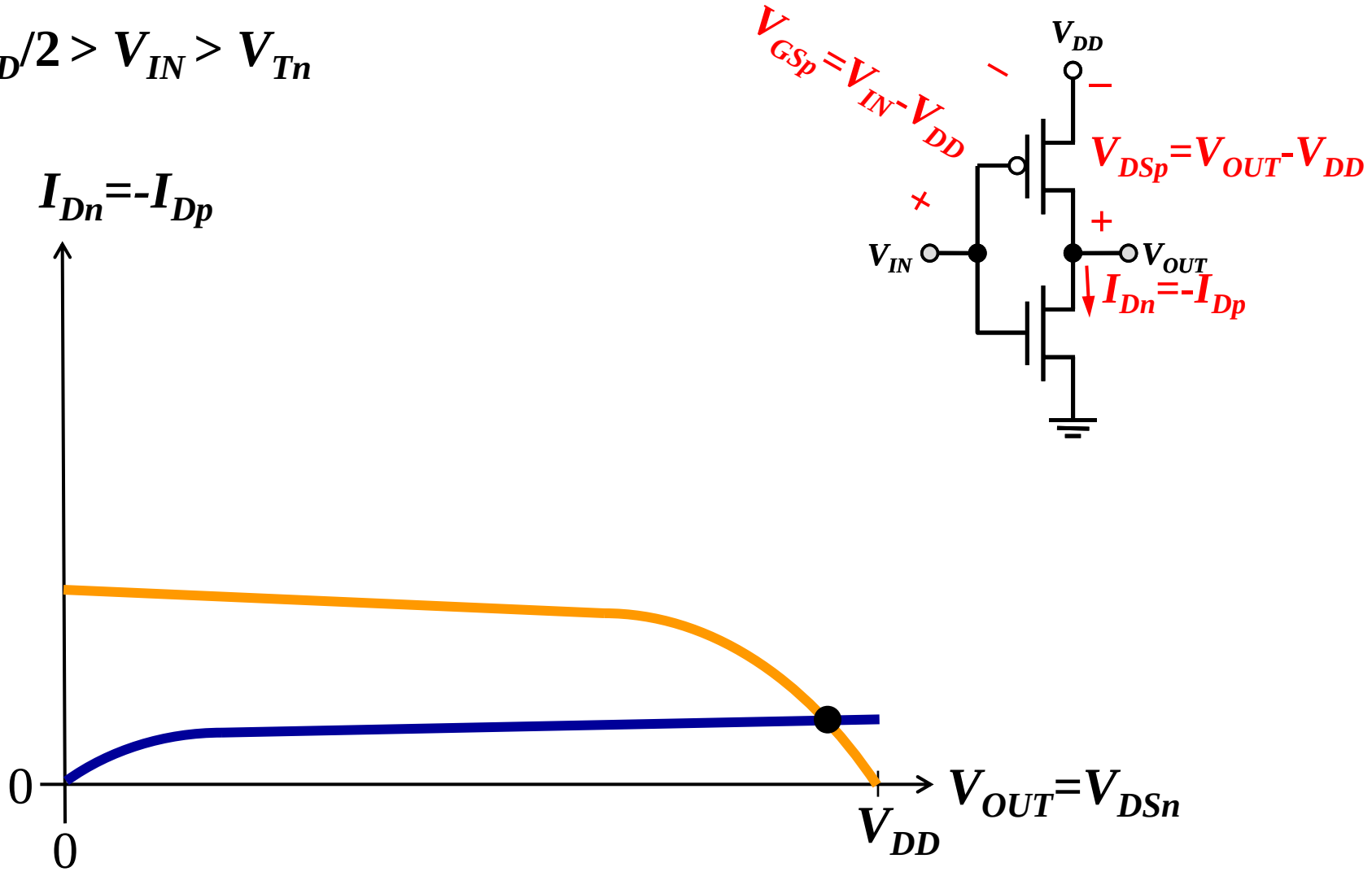


CMOS Inverter Load-Line Analysis: Region A



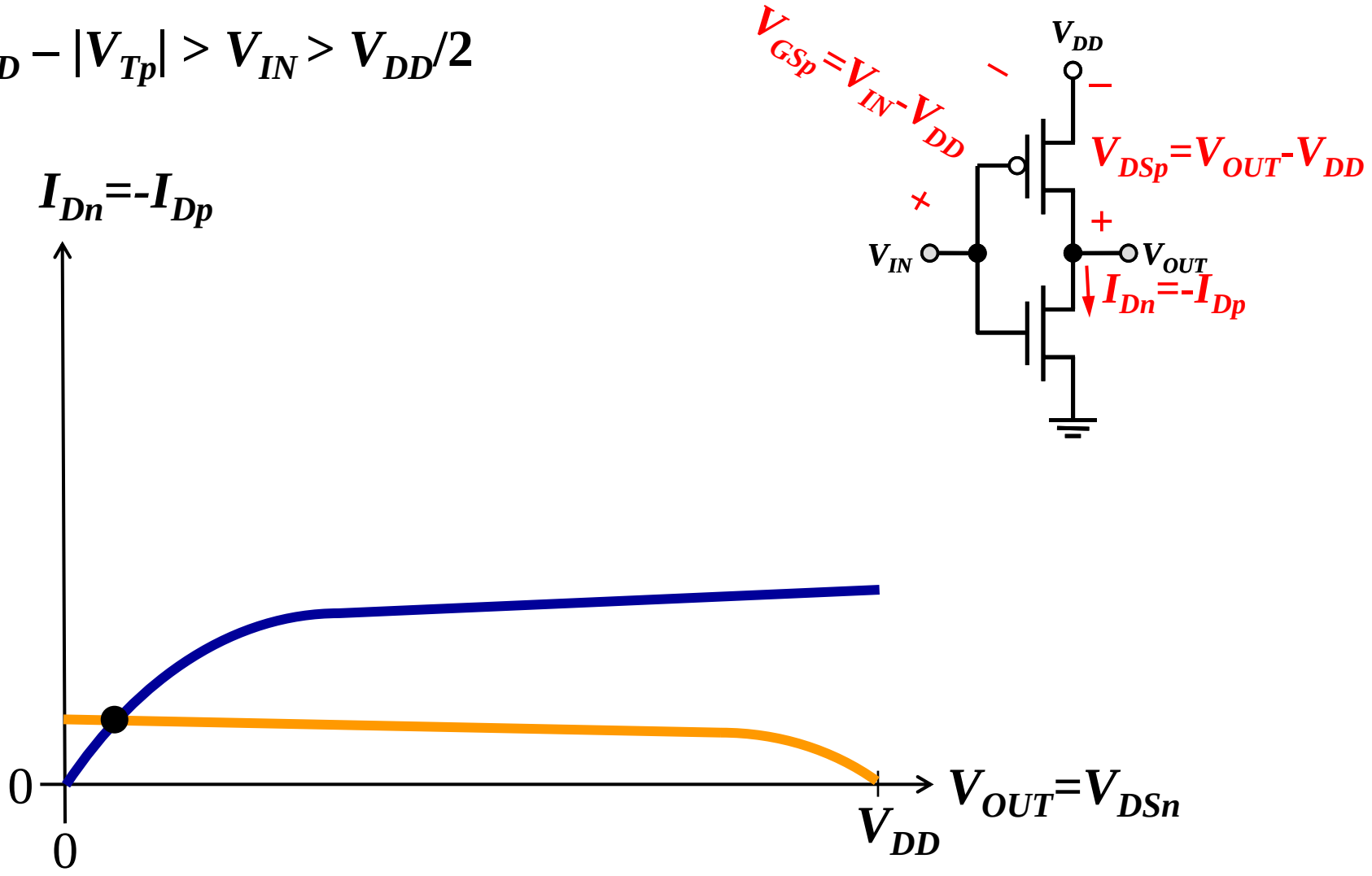
CMOS Inverter Load-Line Analysis: Region B

$V_{DD}/2 > V_{IN} > V_{Tn}$



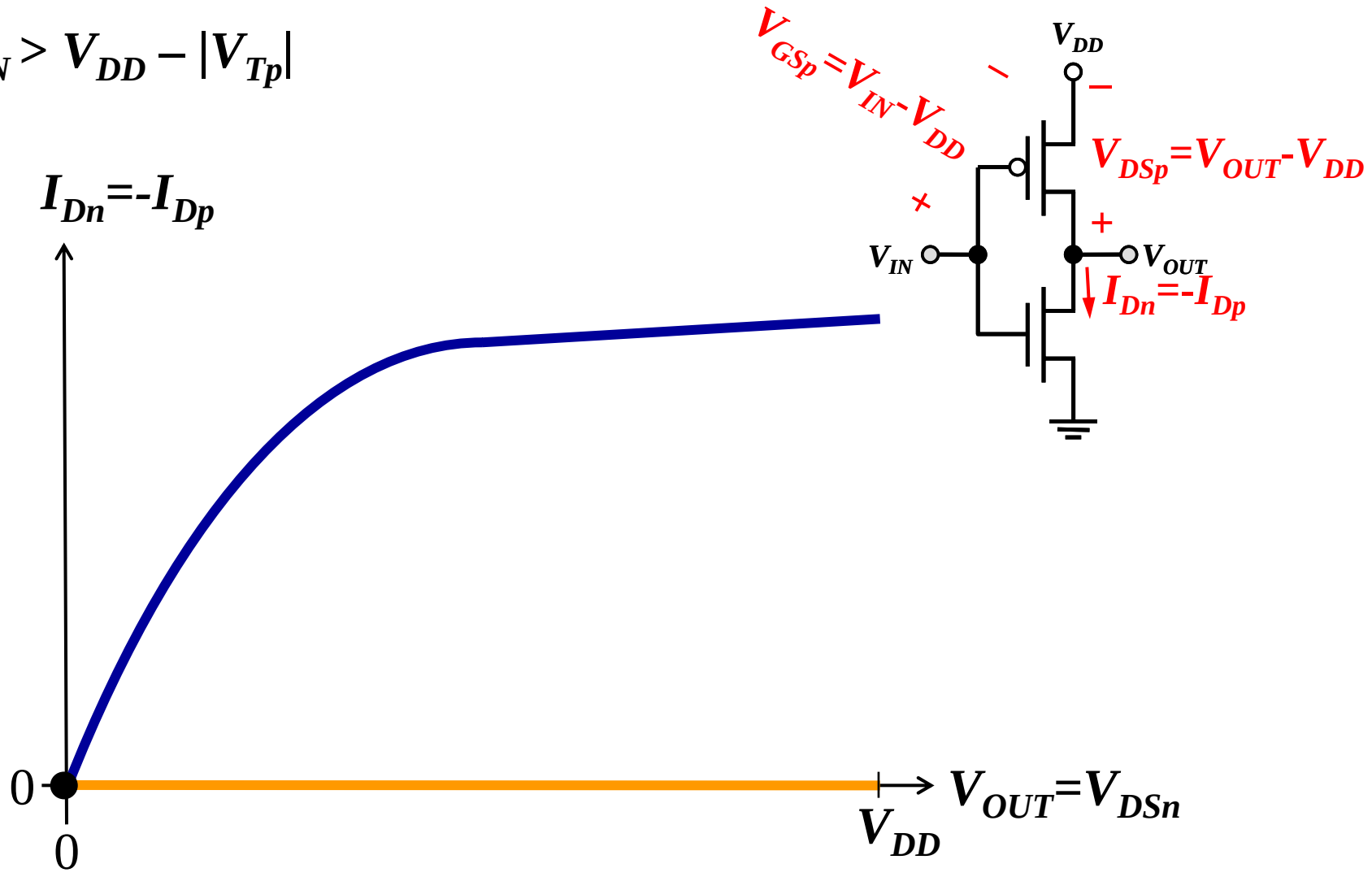
CMOS Inverter Load-Line Analysis: Region D

$V_{DD} - |V_{Tp}| > V_{IN} > V_{DD}/2$



CMOS Inverter Load-Line Analysis: Region E

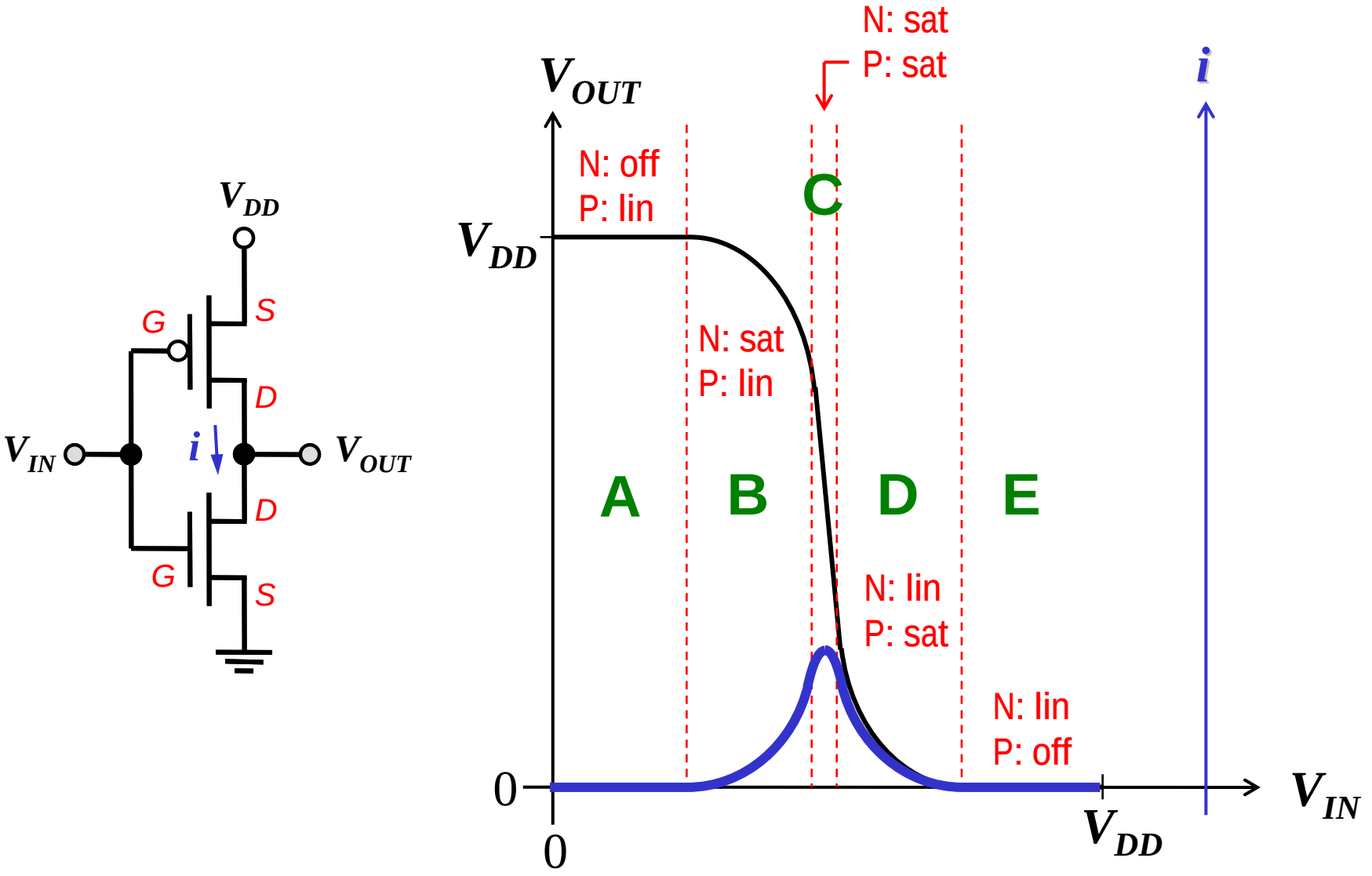
$V_{IN} > V_{DD} - |V_{Tp}|$



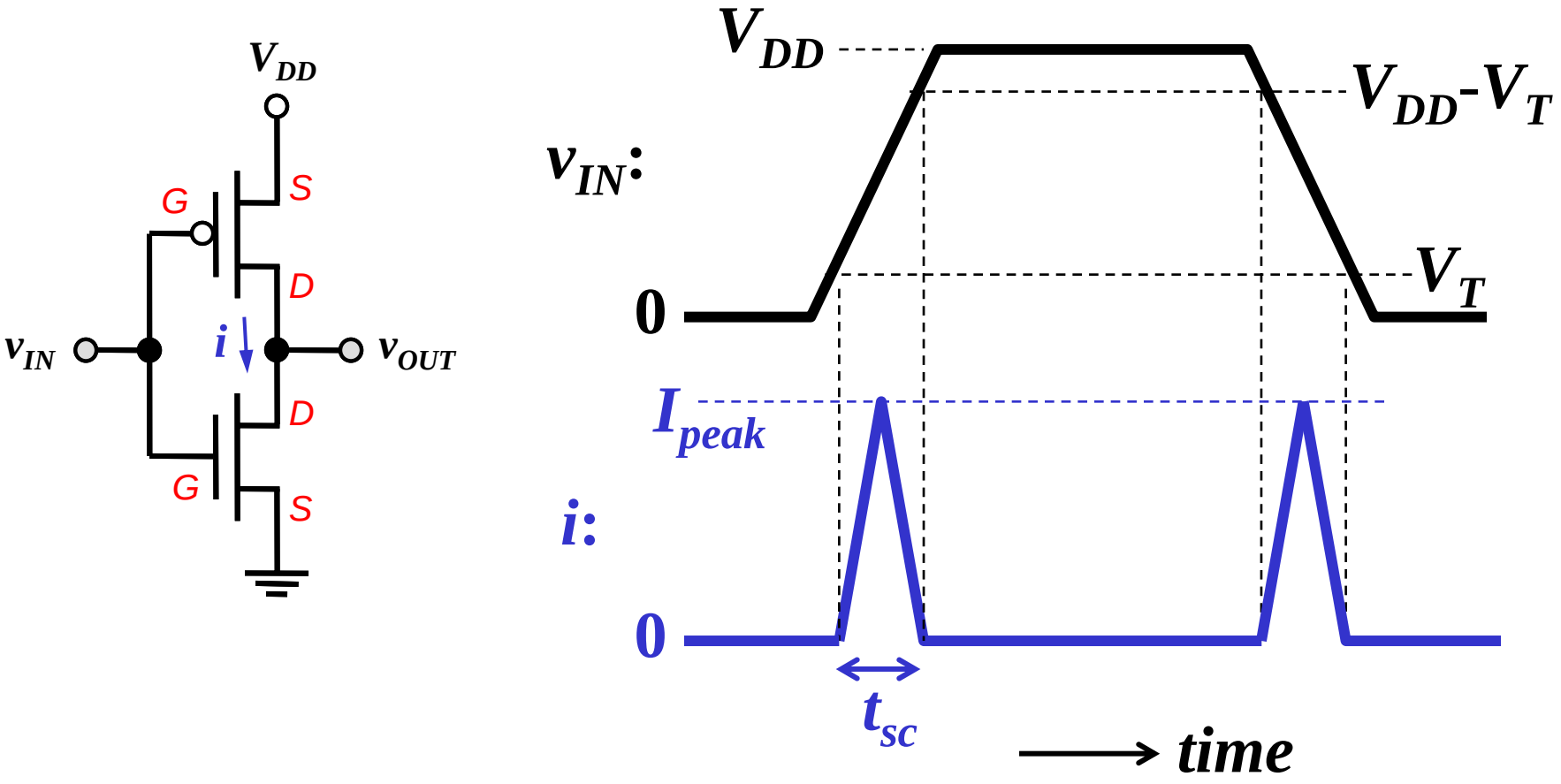
Features of CMOS Digital Circuits

- The output is always connected to V_{DD} or **GND** in steady state
  - → Full logic swing; large noise margins
  - → Logic levels are not dependent upon the relative sizes of the devices ("ratioless")
- There is no direct path between V_{DD} and **GND** in steady state
  - → no static power dissipation

The CMOS Inverter: Current Flow during Switching



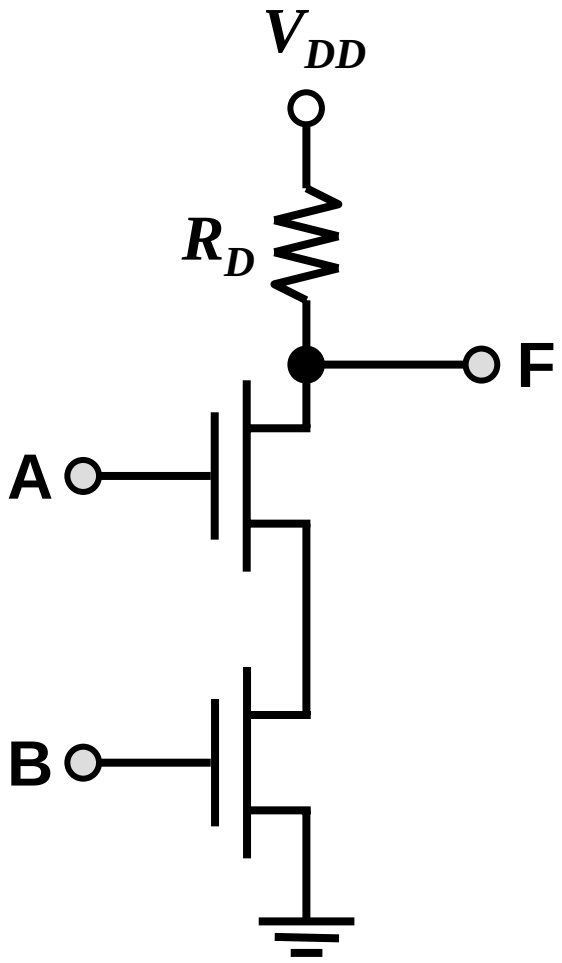
Power Dissipation due to Direct-Path Current



Energy consumed per switching period: $E_{dp} = t_{sc} V_{DD} I_{peak}$

NMOS NAND Gate

- Output is low only if both inputs are high

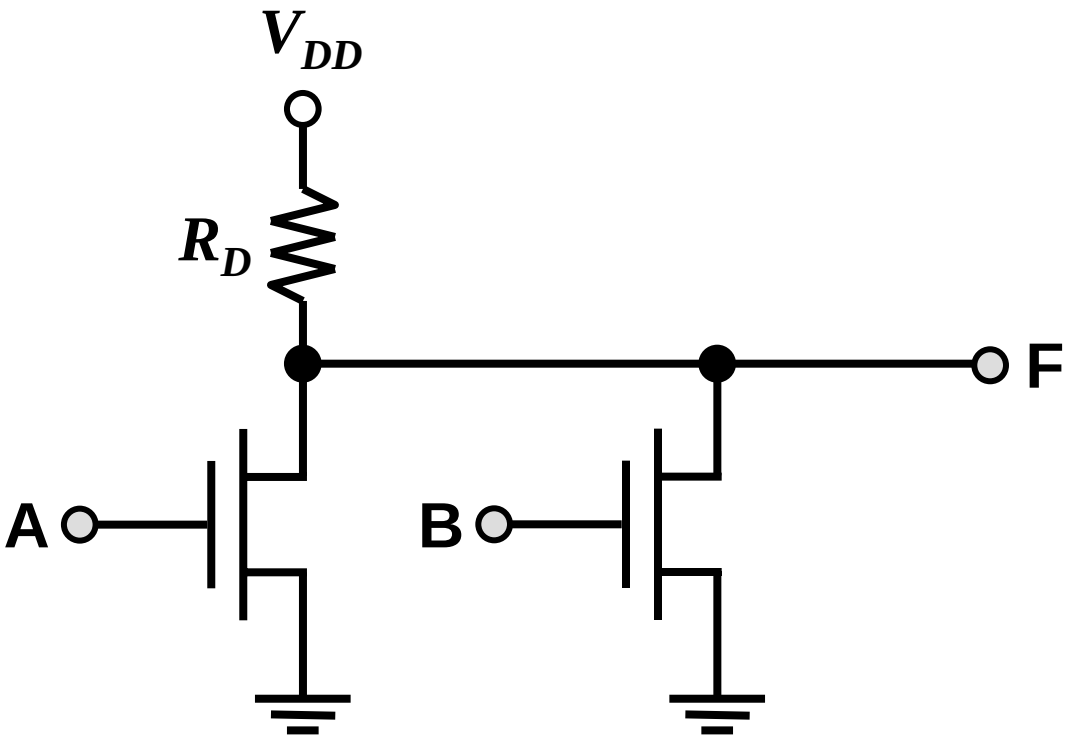


Truth Table

A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

NMOS NOR Gate

- Output is low if either input is high

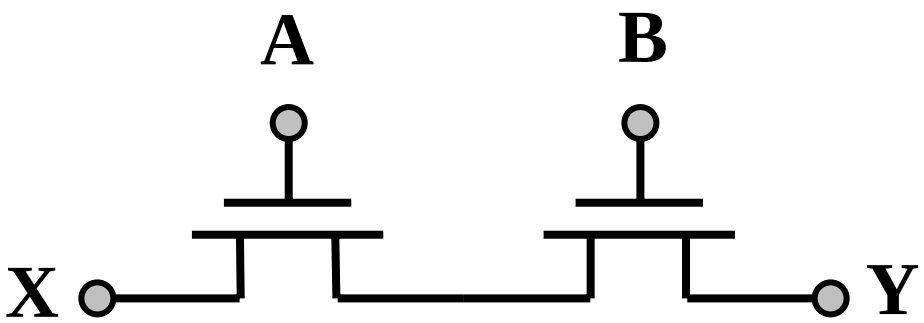


Truth Table

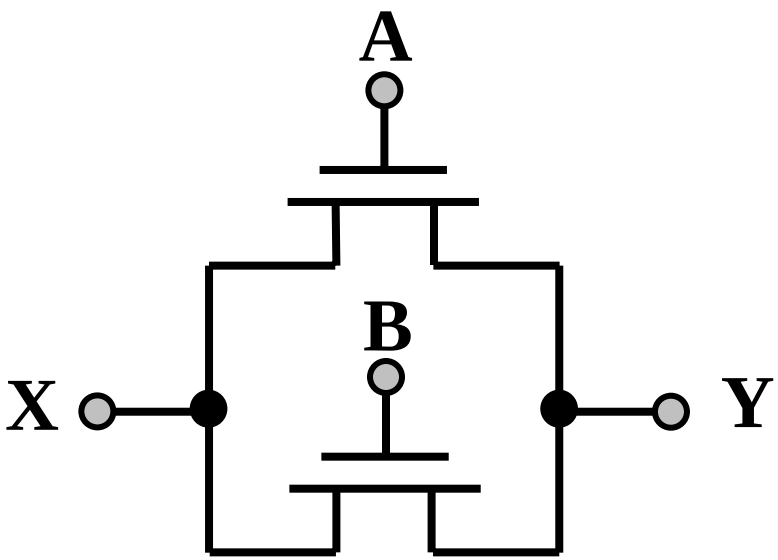
A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

N-Channel MOSFET Operation

An NMOSFET is a closed switch when the input is high



Y = X if **A** and **B**

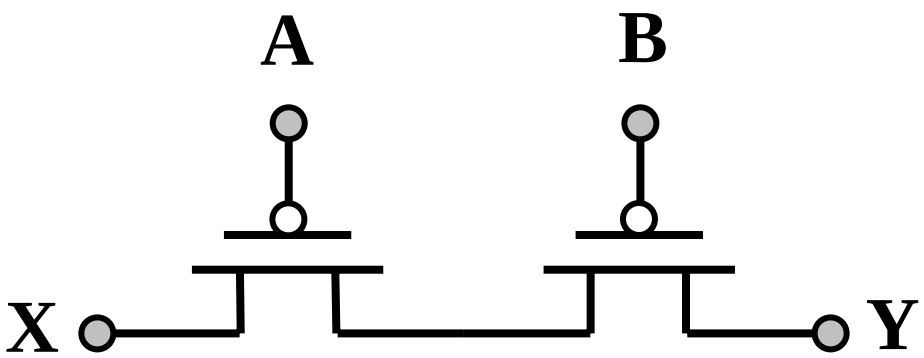


Y = X if **A** or **B**

NMOSFETs pass a “strong” **0** but a “weak” **1**

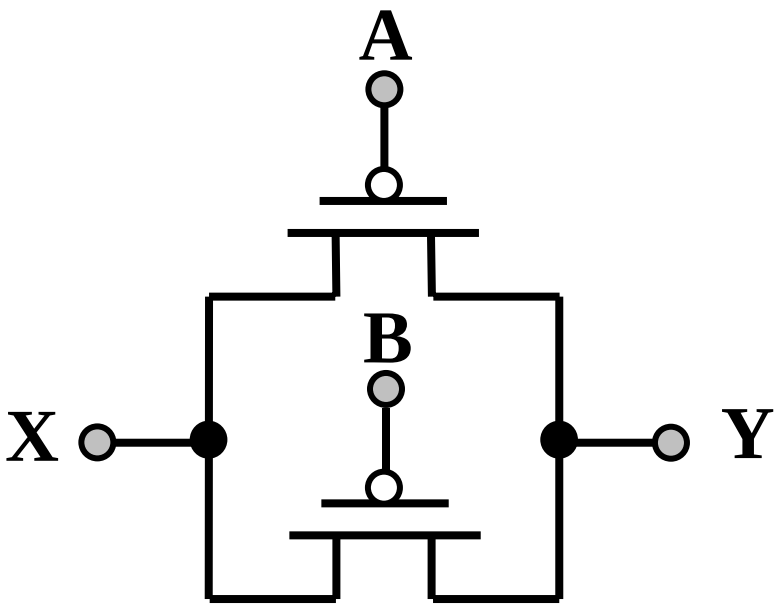
P-Channel MOSFET Operation

A PMOSFET is a closed switch when the input is low



$Y = X$ if $\overline{A}$ and $\overline{B}$

$= \overline{(A + B)}$



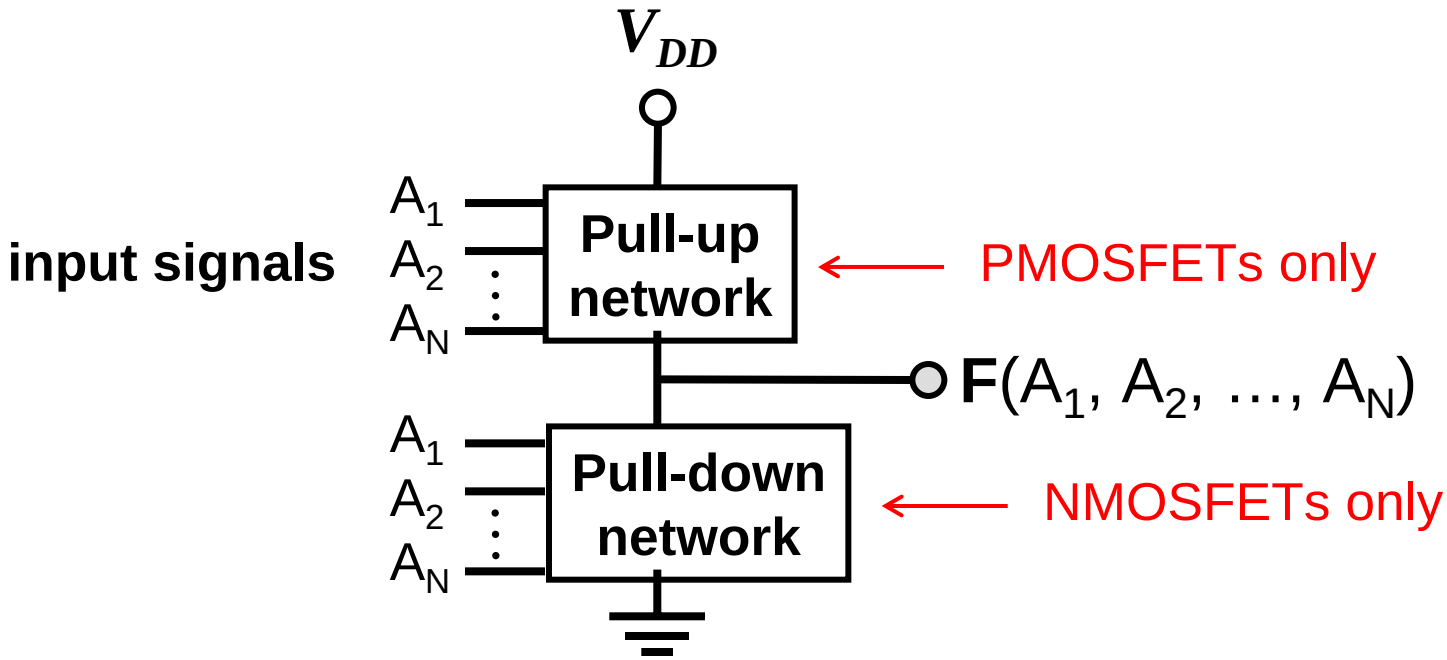
$Y = X$ if $\overline{A}$ or $\overline{B}$

$= \overline{(AB)}$

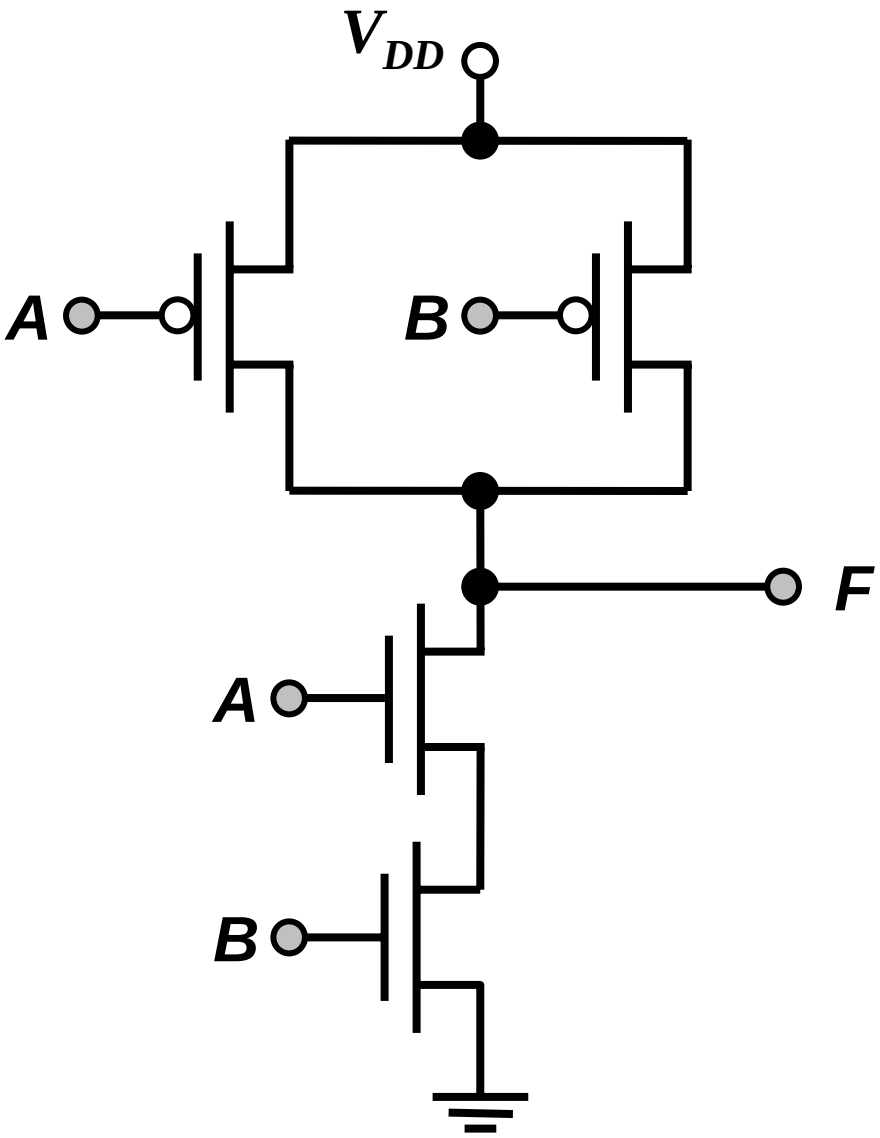
PMOSFETs pass a “strong” **1** but a “weak” **0**

Pull-Down and Pull-Up Devices

- In CMOS logic gates, NMOSFETs are used to connect the output to **GND**, whereas PMOSFETs are used to connect the output to V_{DD}.
  - An NMOSFET functions as a ***pull-down device*** when it is turned on (gate voltage = V_{DD})
  - A PMOSFET functions as a ***pull-up device*** when it is turned on (gate voltage = ***GND***)

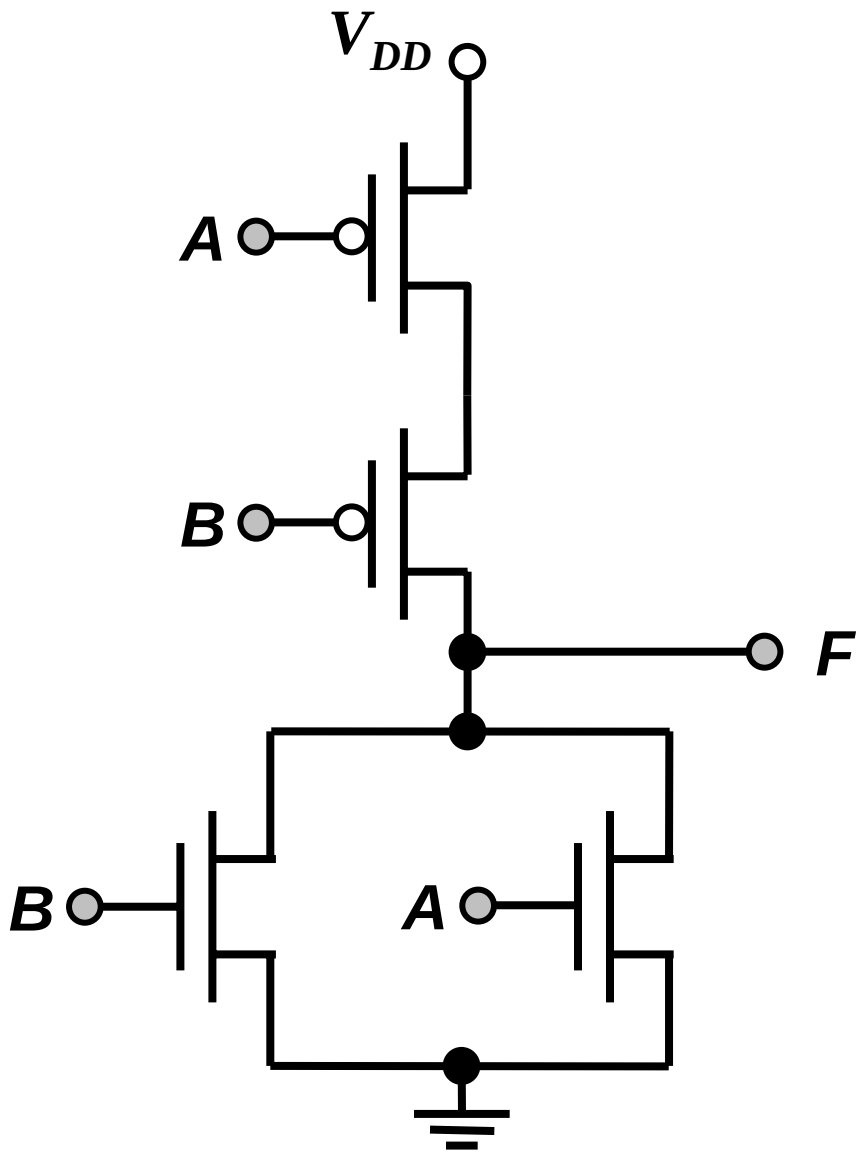


CMOS NAND Gate



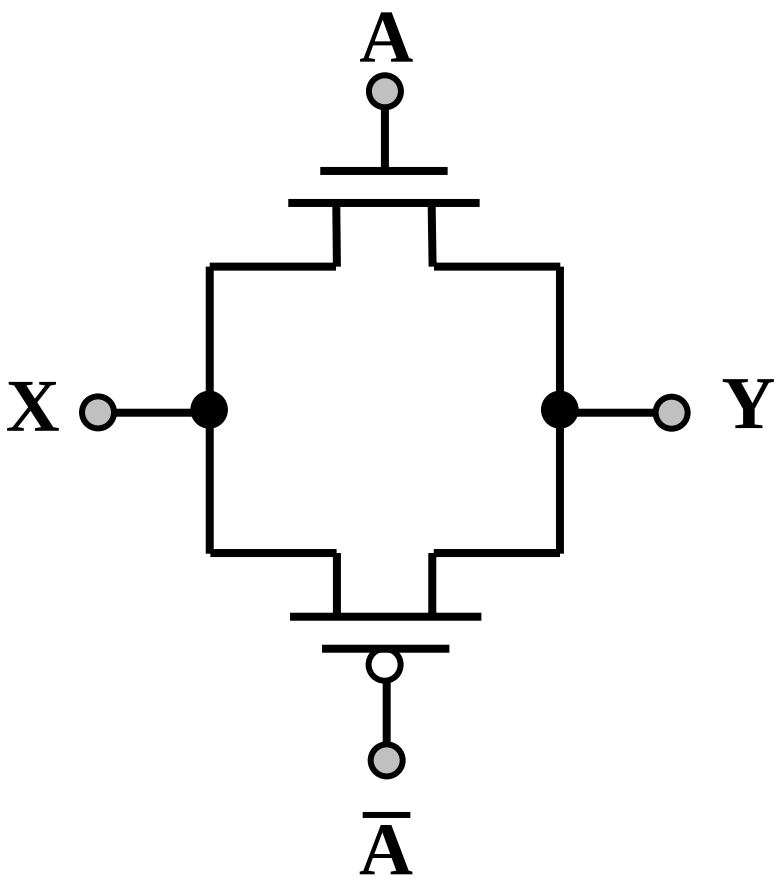
A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

CMOS NOR Gate



A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

CMOS Pass Gate



Y = X if A