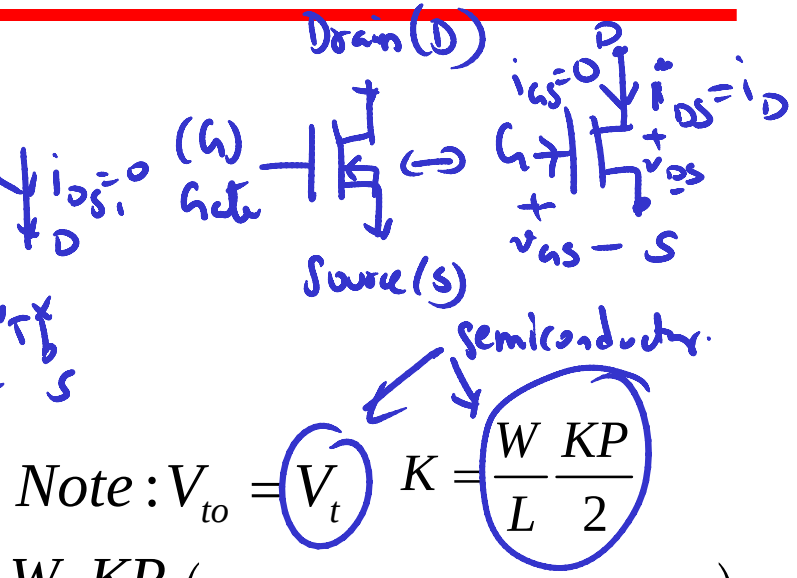
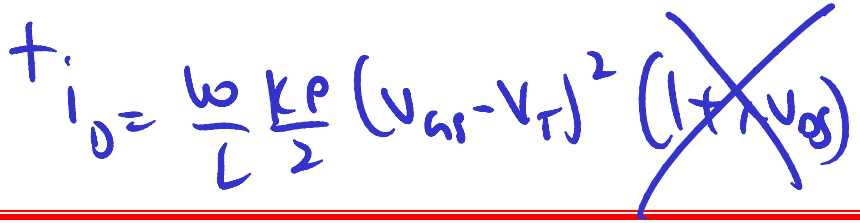
EE100Su08 Lecture #17 (August 4th 2008)

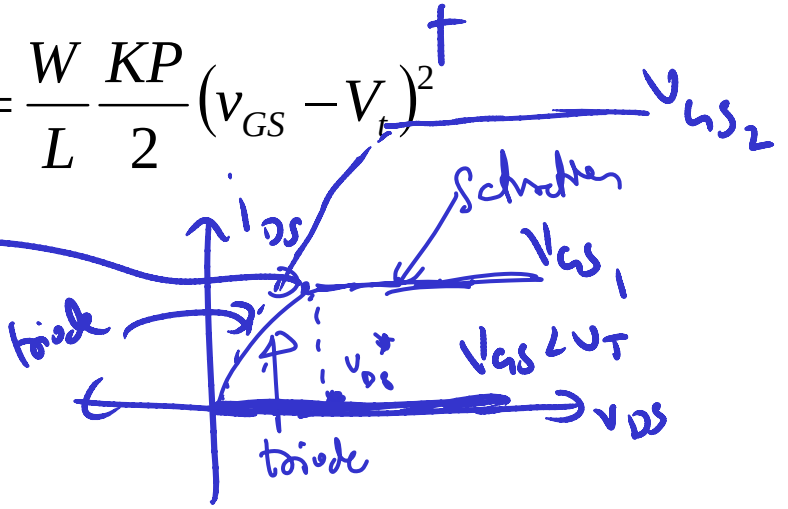
- OUTLINE
  - HW #3s-#6s: Pick up from lab, regrades: talk to Bart (HW #4s are in lab as well)
  - QUESTIONS?
  - Lecture schedule:
    - Today: wrap up transistors
    - Wednesday (08/06): Review
    - Friday (08/08), Monday (08/11): NO LECTURE
    - Wednesday (08/13): TA review
    - Friday (08/15): Final exam
  - Transistor introduction (MOSFETs)
  - Simple transistor circuit: resistive inverter
  - Transistor logic circuits
- Reading
  - Reader: Chapter 4 and 5 (concentrate on logic applications).

MOSFET

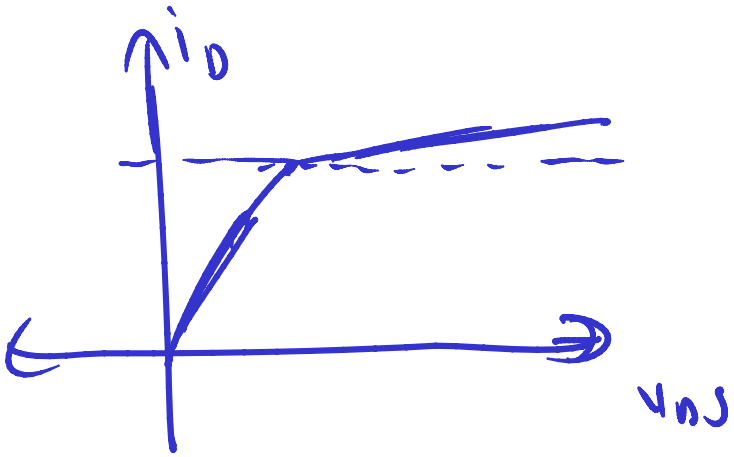
- NMOS: Three regions of operation
  - V_{DS} and V_{GS} normally positive valus
  - $V_{GS}<V_t$:cut off mode, $I_{DS}=0$ for any V_{DS}
  - $V_{GS}>V_t$:transistor is turned on
    - $V_{DS}< V_{GS}-V_t$: Triode Region $\longrightarrow$ $i_D = \frac{W}{L}\frac{KP}{2}\left(2\cdot(v_{GS}-V_t)v_{DS}-v_{DS}^{\ 2}\right)$
    - $V_{DS}> V_{GS}-V_t$: Saturation Region $\longrightarrow$ $i_D = \frac{W}{L}\frac{KP}{2}(v_{GS}-V_t)^2$
    - Boundary $v_{GS}-V_t = v_{DS}^*$

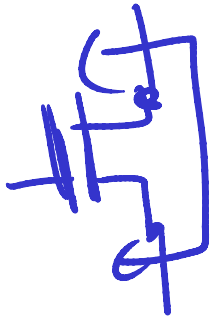






Transistor as an amplifier

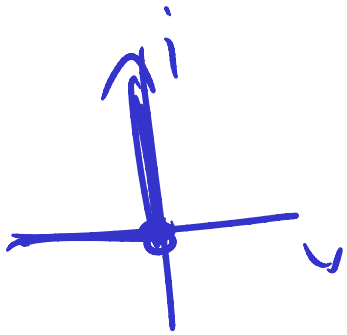




R_{out} ↓, saturation

Big!

(operated in triode)



Notice:

(1) $$i_D = \begin{cases} 0 & \text{if } V_{GS} < V_T \rightarrow \text{cutoff} \\ k\left(2(V_{GS}-V_T)\cdot V_{DS} - V_{DS}^2\right) & V_{GS} > V_T \ \& \ V_{DS} < V_{GS}-V_T \\ k(V_{GS}-V_T)^2 & V_{GS} > V_T \ \& \ V_{DS} > V_{GS}-V_T \end{cases}$$

triode

saturation

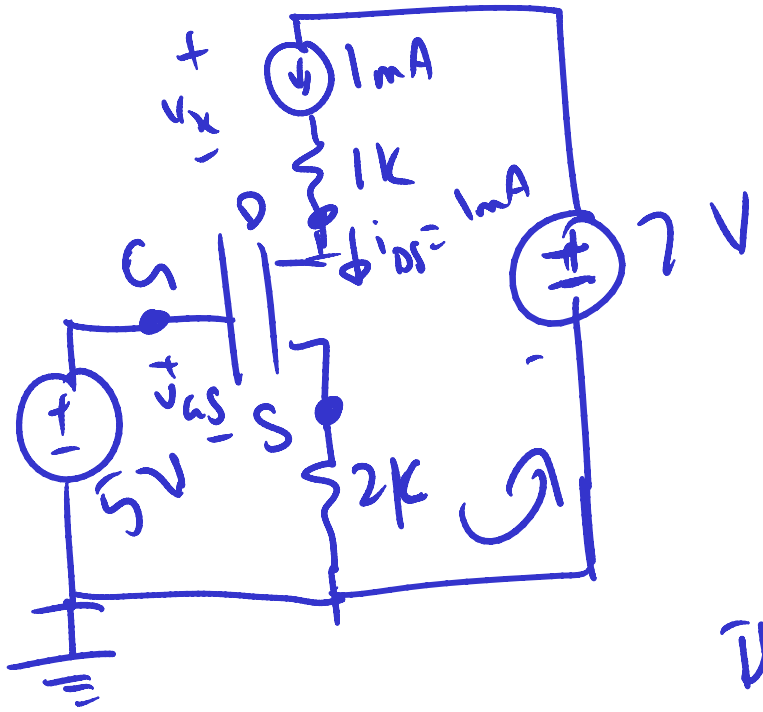
(2) As you switch from triode $\rightarrow$ saturation,

$$k\left(2(V_{GS}-V_T)V_{DS} - V_{DS}^2\right)\Big|_{V_{GS}-V_T = V_{DS}} = k\left(2(V_{GS}-V_T)^2 - (V_{GS}-V_T)^2\right)$$

$$= k(V_{GS}-V_T)^2 \triangleq \text{saturation} \quad \checkmark$$

[usually: $V_T = 1\ V$, $K = 500\ \frac{\mu A}{V^2}$]

Simple transistor circuits.



Qs: (1) what is V_{DS}?

(2) what mode is the transistor operating in?

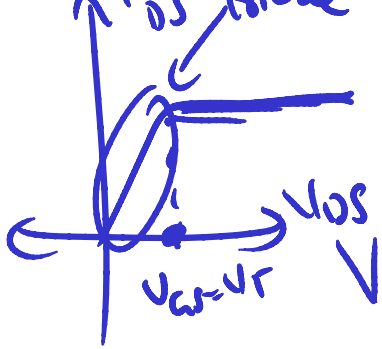
KVL: $7 - V_x - 1 - V_{DS} - 2 = 0$

If we can find V_{GS}, we know V_T

$\Rightarrow$ we can try & find the transistor mode of operation.

$V_T = 0.7$ V

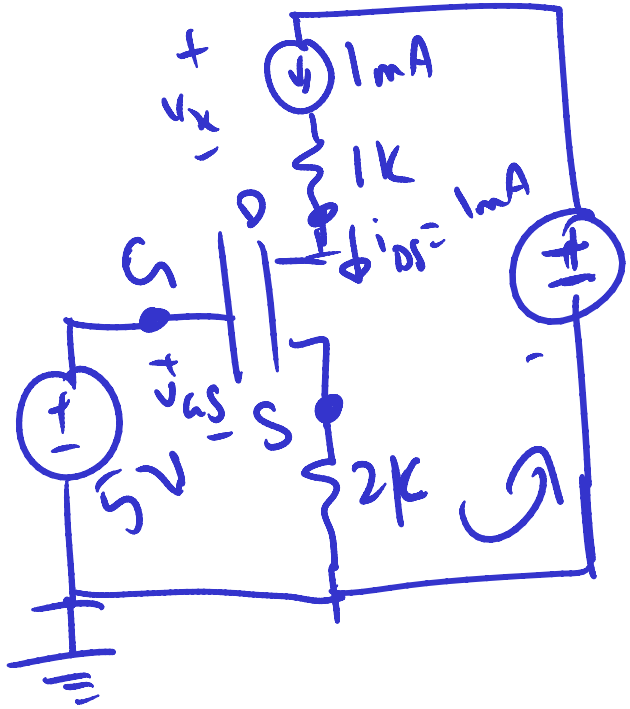
$k = 500 \frac{mA}{V^2}$



$V_{GS} = V_G - V_S = 5 - (2k)(1m A)$

$= 3$ V

Simple transistor circuits.



$V_T = 0.7$ V

$k = 500 \frac{mA}{V^2}$

Q: (1) what is V_{DS}?

(2) what mode is the transistor operating in?

KVL: $7 - V_x - 1 - V_{DS} - 2 = 0$

$I_D = 1$mA, fixed by current source

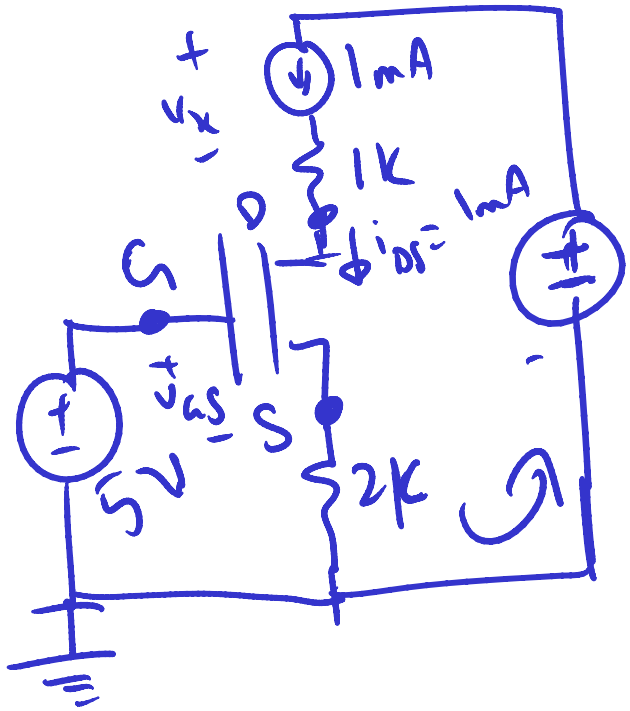
Assume transistor is saturated

$\Rightarrow I_D = k(V_{GS} - V_T)^2$

$= 500 \frac{mA}{V^2} (3 - 0.7)^2$

$= (2.3)^2 \cdot 500$ mA ≈ 2.6 mA

Simple transistor circuits.



Qs: (1) What is V_{DS}?

(2) What mode is the transistor operating in?

$\rightarrow$ $V_{DS} < V_{GS} - V_T$

$\Rightarrow$ (2) Transistor is in triode

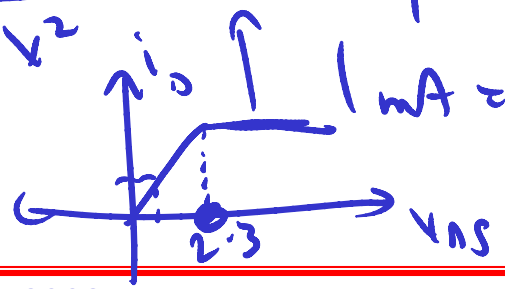
[Because $i_{D_{fet}} \neq i_{D_{current\ source}}$]

$V_T = 0.7$ V

$K = 500 \frac{mA}{V^2}$

$\therefore i_D = K\left((V_{GS} - V_T) \cdot V_{DS} - V_{DS}^2\right)$

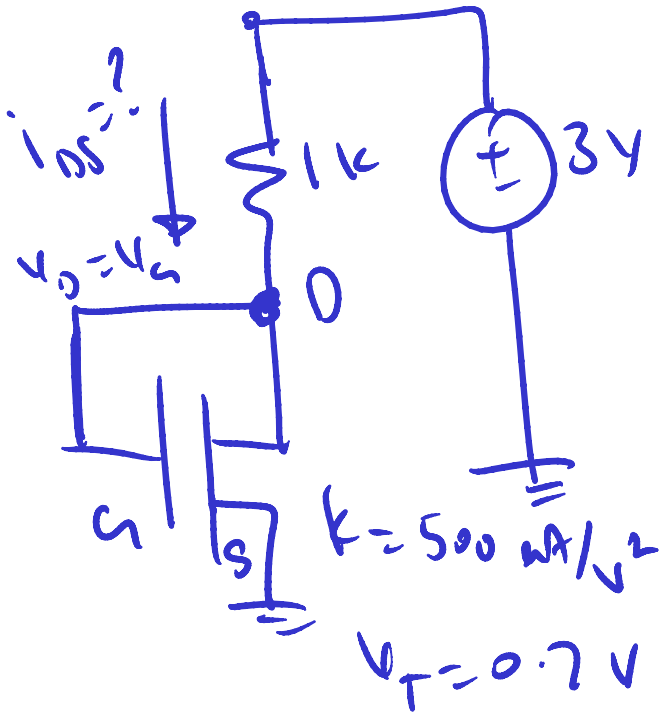
$V_{GS} = 3$ V



$1\text{mA} = 500\text{mA}\left(2.3 V_{DS} - V_{DS}^2\right)$

$\Rightarrow$ $V_{DS} = 0.49$ V, 4.11 V

Interesting Circuit : CURRENT SOURCES



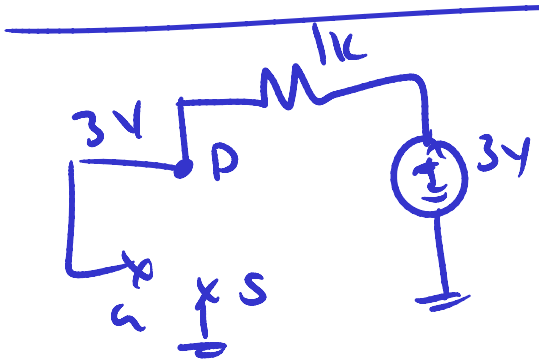
Mode of operation:

$V_{GS} < V_T \Rightarrow$ OFF!

$V_{DS} < V_{GS} - V_T \Rightarrow$ triode

$V_{DS} \geq V_{GS} - V_T \Rightarrow$ saturation

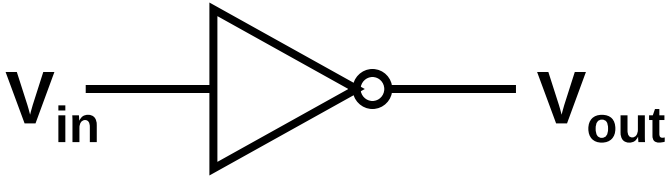
$V_{DS} = V_{GS} - V_T$ ⊃ D



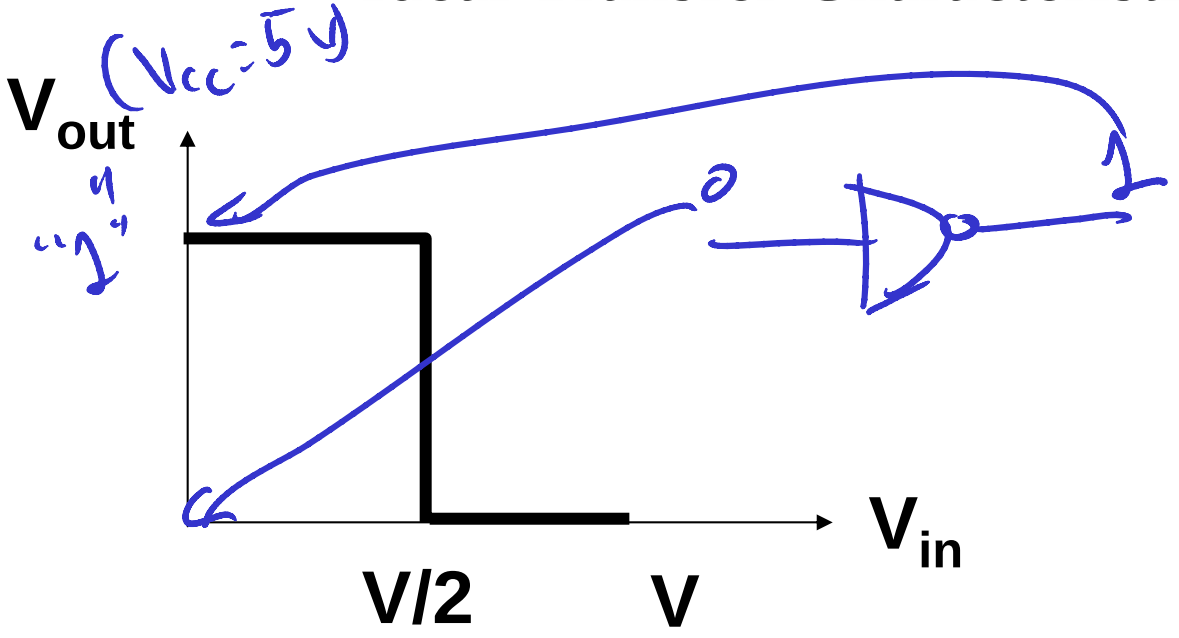
Solved $I_{DS} = k(V_{GS} - V_T)^2$

$\Rightarrow \boxed{\frac{3 - V_{DS}}{1k} = k(V_{DS} - V_T)^2}$

Inverter = NOT Gate

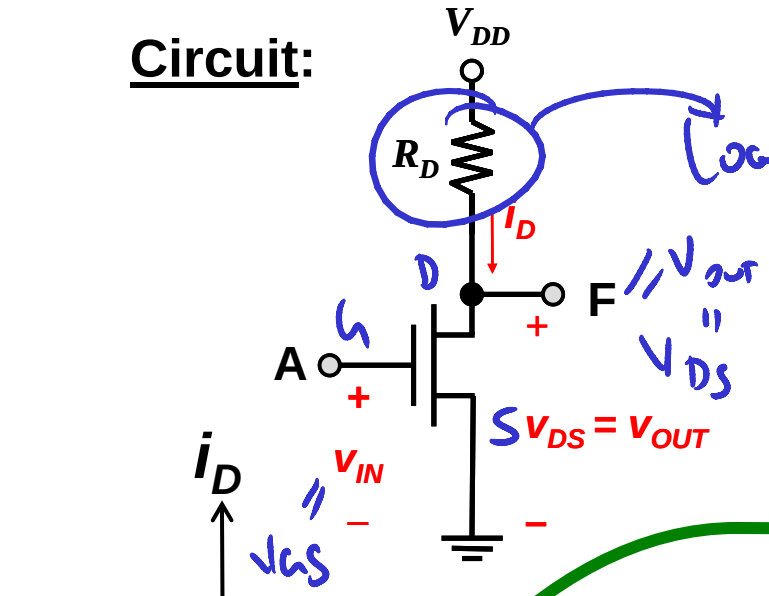


Ideal Transfer Characteristics

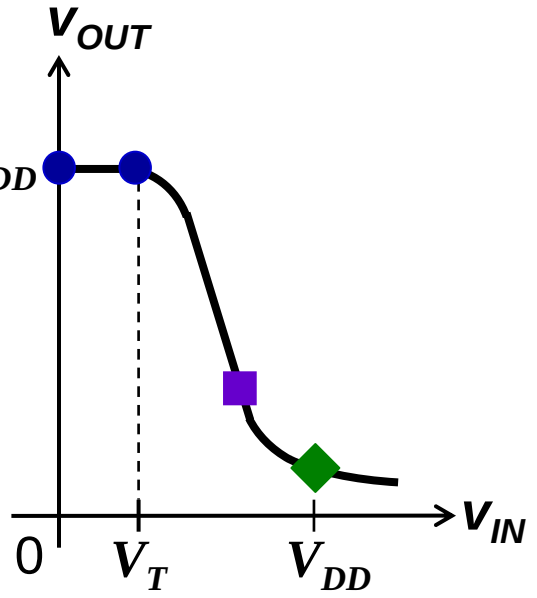


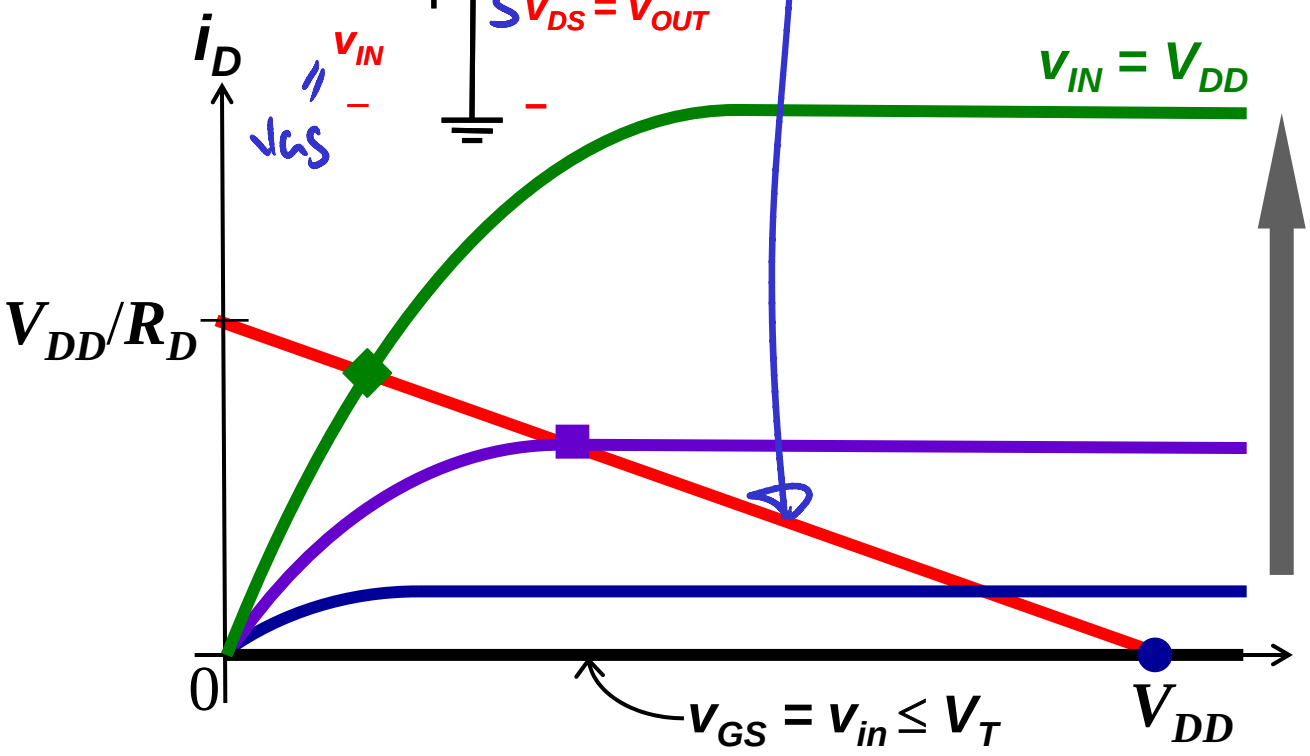
NMOS Resistor Pull-Up

Circuit:



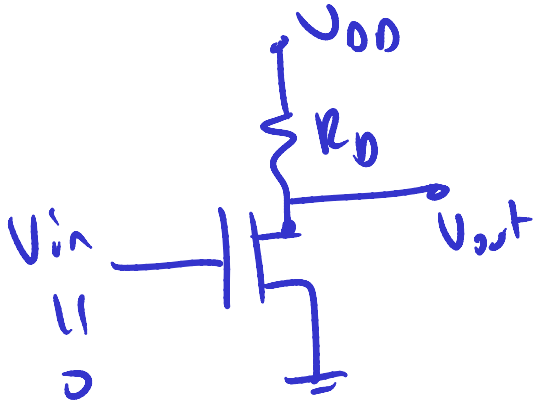
Voltage-Transfer Characteristic

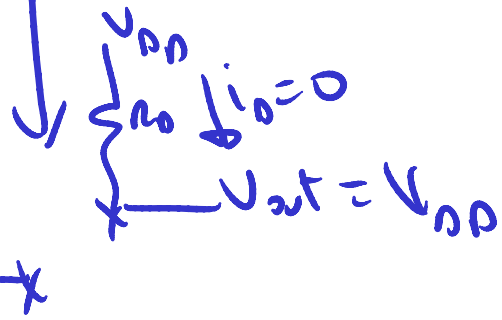




A	F
0	1
1	0

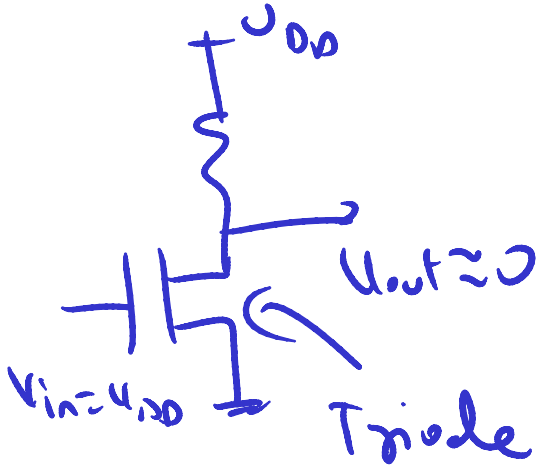
NMOS-resistively loaded inverter: Power problem!





$P_{D_{R_D}} = 0\,W$

$P_{D_{NMOS}} = 0\,W$ ✓



$\Rightarrow P_{dissipated} \neq 0\,V$

Disadvantages of NMOS Logic Gates

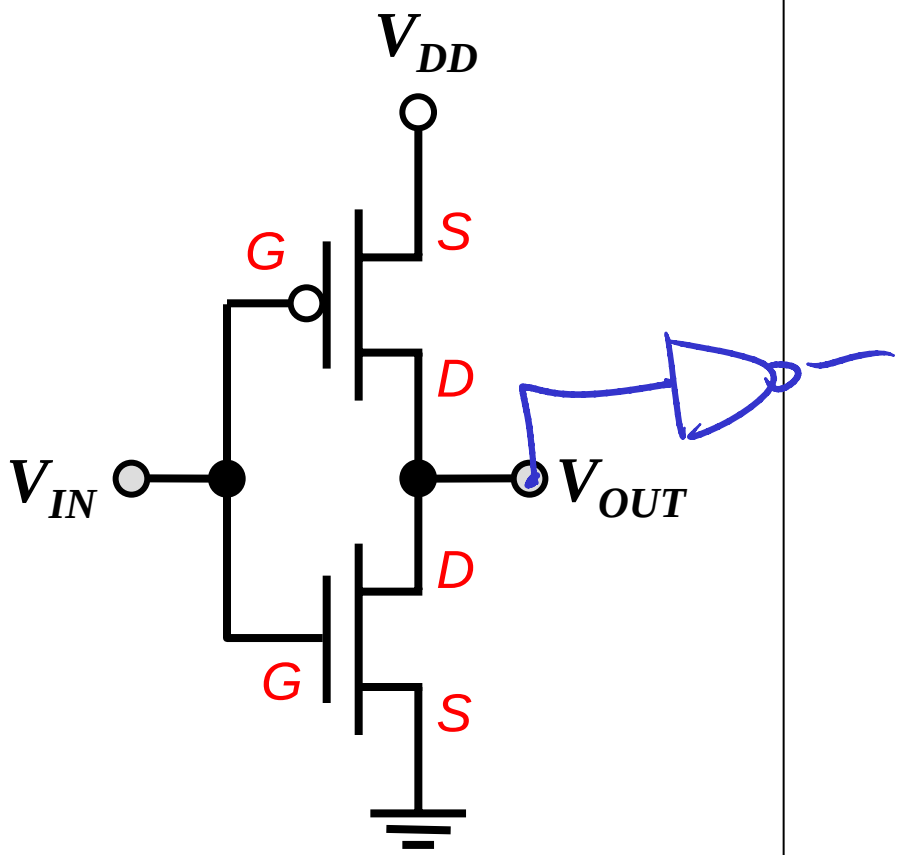
- Large values of $\boldsymbol{R_D}$ are required in order to
  - achieve a low value of V_{OL}
  - keep power consumption low

  → Large resistors are needed, but these take up a lot of space.

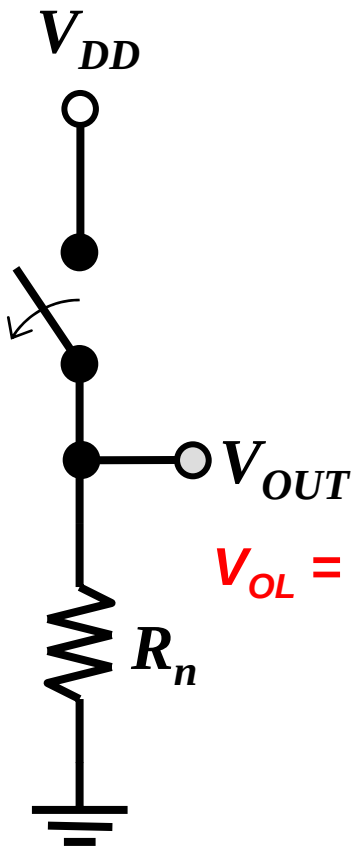
    - One solution is to replace the resistor with an NMOSFET that is always on.

The CMOS Inverter: Intuitive Perspective

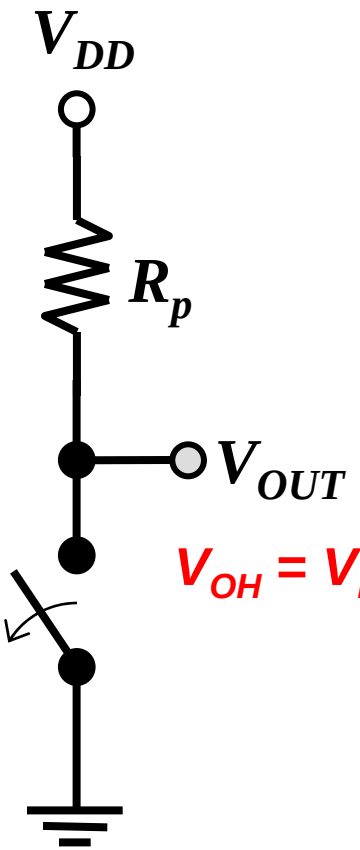
CIRCUIT



SWITCH MODELS



$V_{OL} = 0$ V



$V_{OH} = V_{DD}$

Low static power consumption, since one MOSFET is always off in steady state

$V_{IN} = V_{DD}$

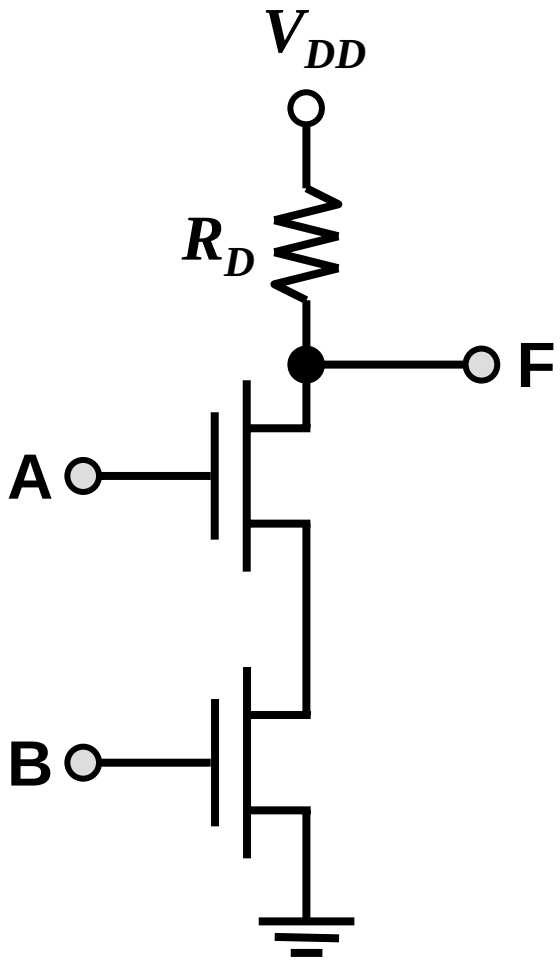
$V_{IN} = 0$ V

Features of CMOS Digital Circuits

- The output is always connected to V_{DD} or **GND** in steady state
  - → Full logic swing; large noise margins
  - → Logic levels are not dependent upon the relative sizes of the devices ("ratioless")
- There is no direct path between V_{DD} and **GND** in steady state
  - → no static power dissipation

NMOS NAND Gate

- Output is low only if both inputs are high



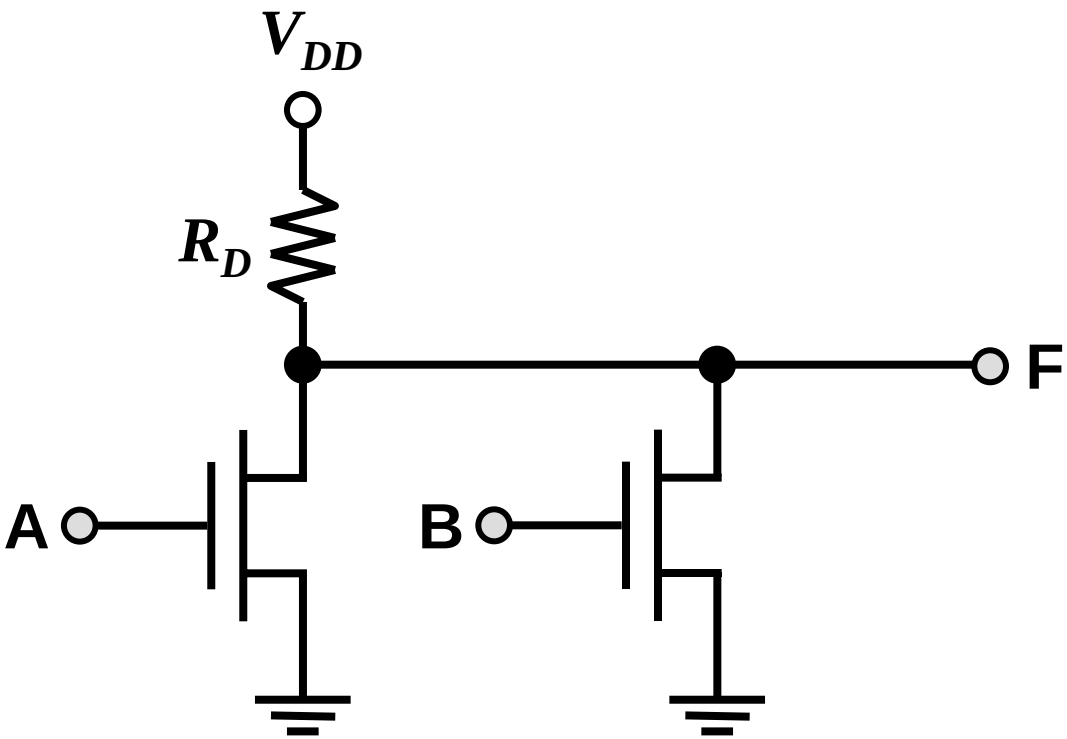
0 = ⏚ 1 = V_{DD}

A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

Truth Table

NMOS NOR Gate

- Output is low if either input is high

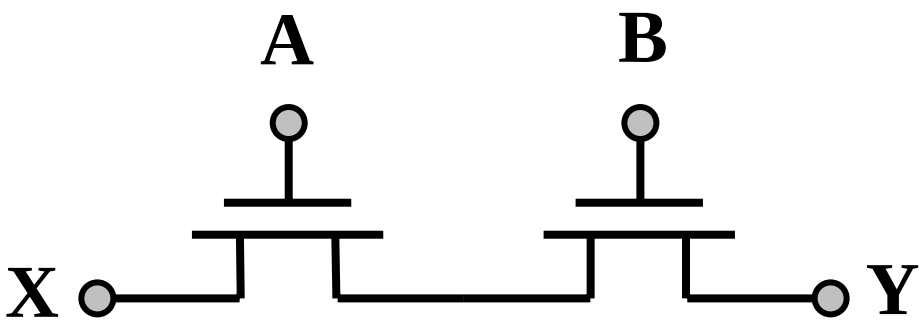


Truth Table

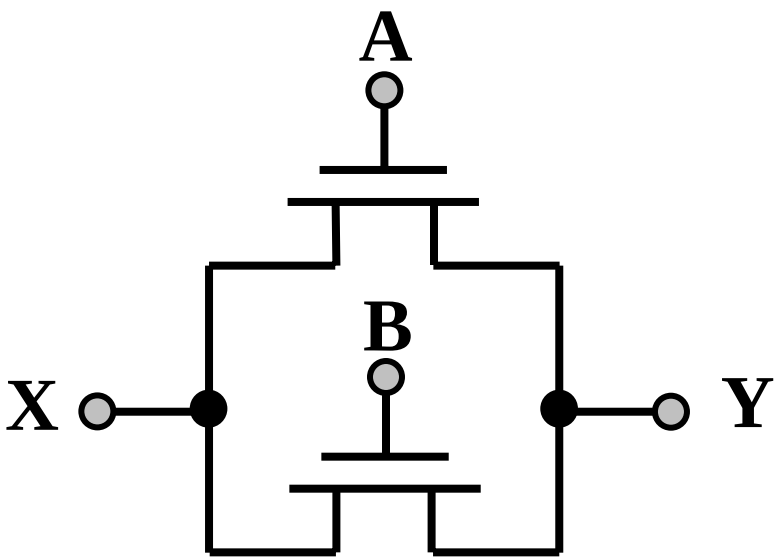
A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

N-Channel MOSFET Operation

An NMOSFET is a closed switch when the input is high



Y = **X** if **A** and **B**

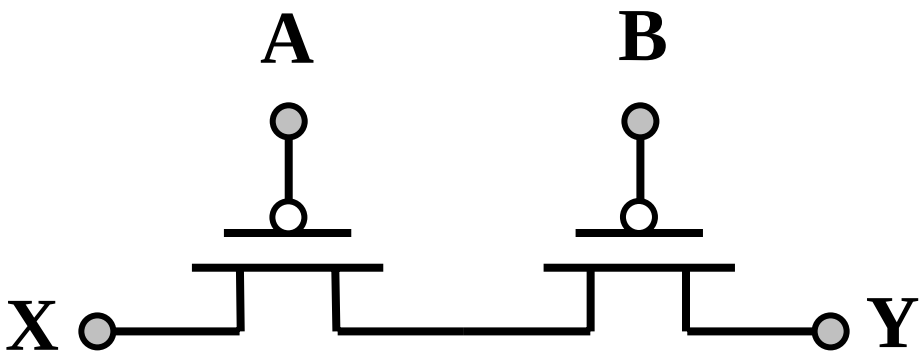


Y = **X** if **A** or **B**

NMOSFETs pass a “strong” **0** but a “weak” **1**

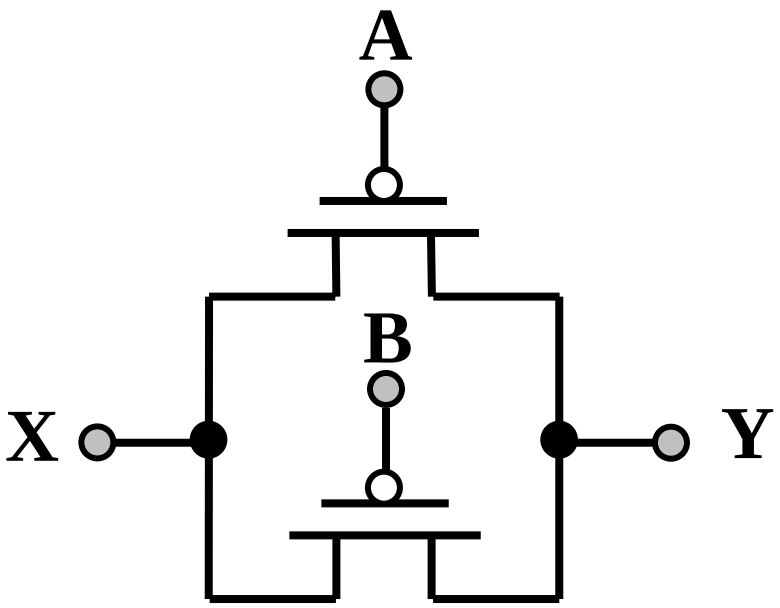
P-Channel MOSFET Operation

A PMOSFET is a closed switch when the input is low



$Y = X$ if $\overline{A}$ and $\overline{B}$

$= \overline{(A + B)}$



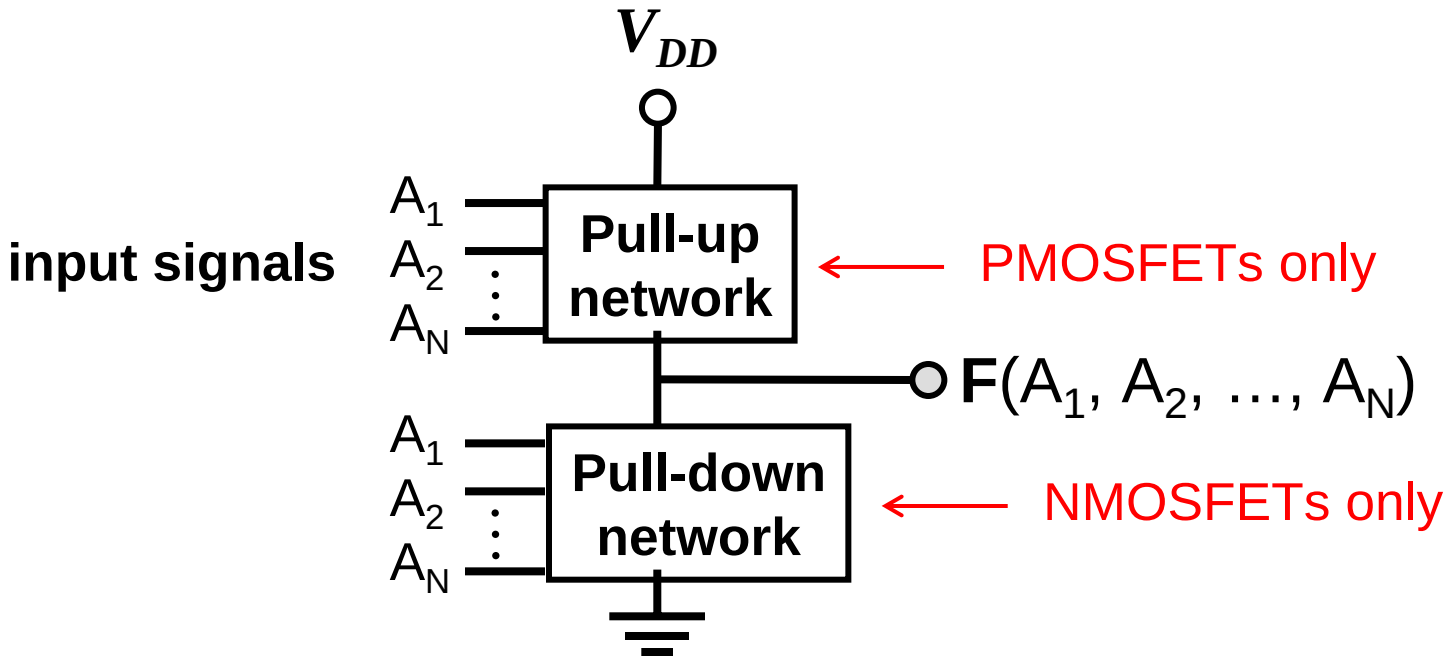
$Y = X$ if $\overline{A}$ or $\overline{B}$

$= \overline{(AB)}$

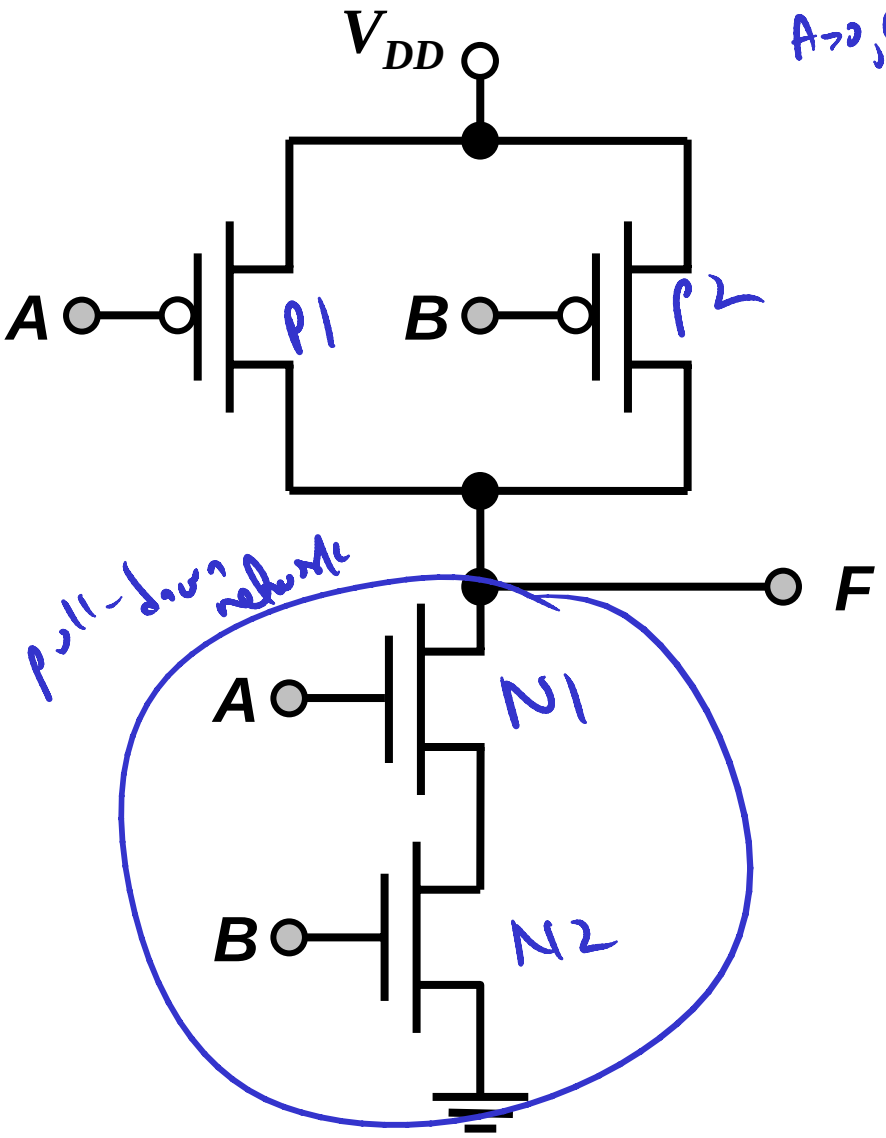
PMOSFETs pass a “strong” **1** but a “weak” **0**

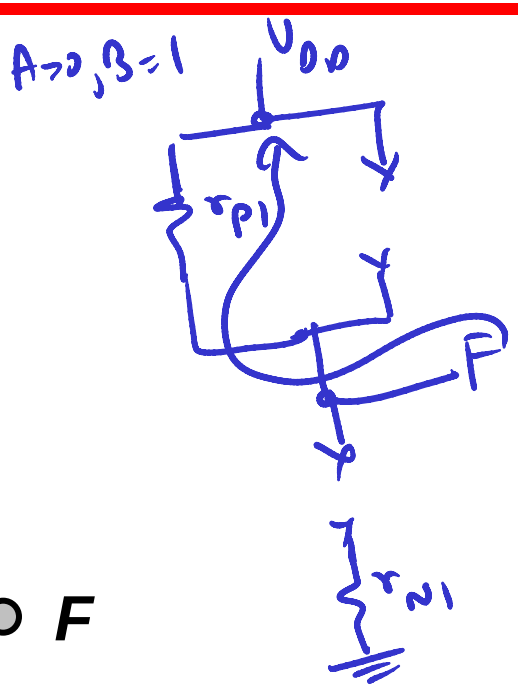
Pull-Down and Pull-Up Devices

- In CMOS logic gates, NMOSFETs are used to connect the output to **GND**, whereas PMOSFETs are used to connect the output to V_{DD}.
  - An NMOSFET functions as a ***pull-down device*** when it is turned on (gate voltage = V_{DD})
  - A PMOSFET functions as a ***pull-up device*** when it is turned on (gate voltage = ***GND***)



CMOS NAND Gate

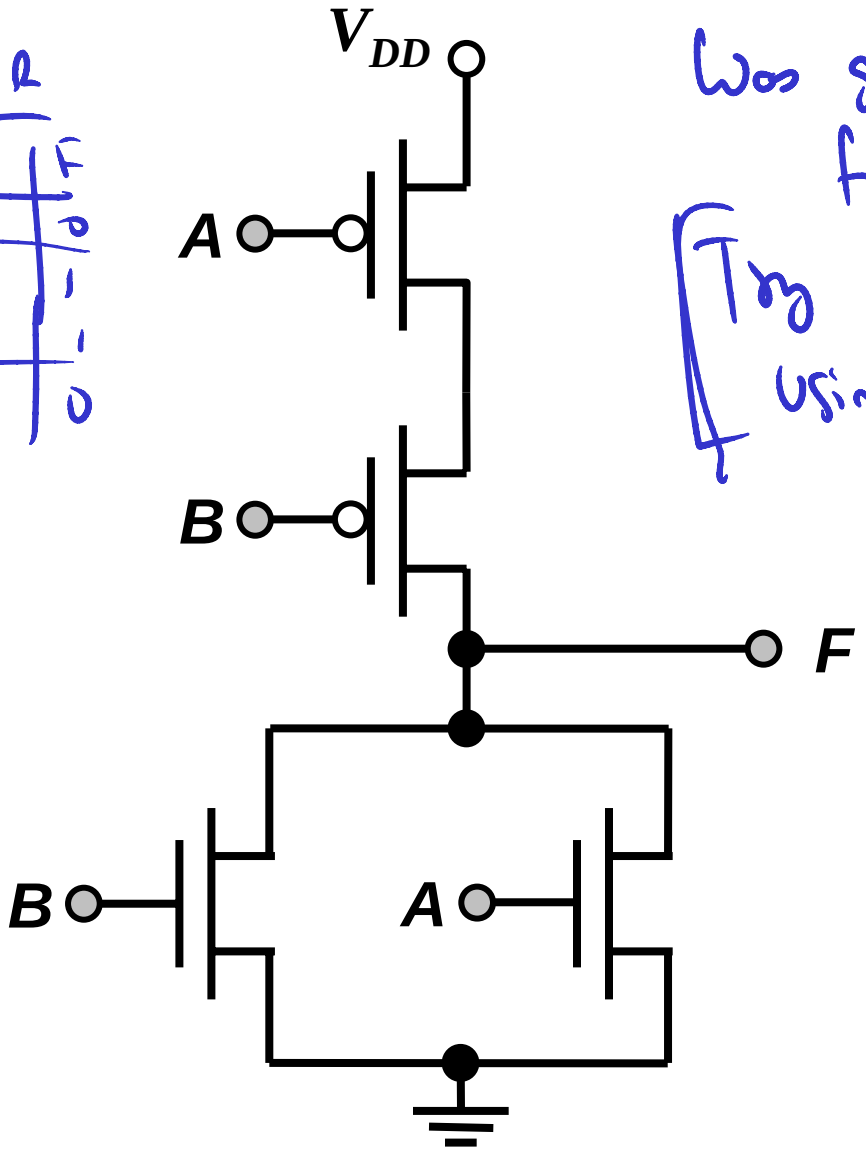




A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

A	B	F	P1	P2	N1	N2
0	0	1	on	on	off	off
0	1	1	on	off	off	on
1	0	1	off	on	on	off
1	1	0	off	off	on	on

CMOS NOR Gate



A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

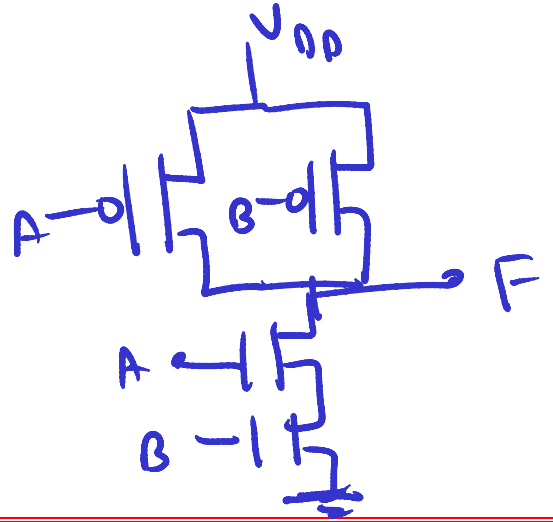
XOR

A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

Was going to be a final problem:

Try to design XOR using CMOS (without cascading NAND, NOR etc)

Notice: NAND formed



XOR: is not linearly separable

A	B	F
0	0	0
0	1	1
1	0	1
1	1	0