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EECS105

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Microelectronic Devices and Circuits- EECS105 Final Exam

Wednesday, December 8, 1999

Costas J. Spanos University of California at Berkeley College of Engineering Department of Electrical Engineering and Computer Sciences

Your Name:	Official	Solutions.
	(last)	(first)
Your Signature: _	-	
		s page before you start.
2. You are allowe	ed three, 8.5"x11'	' handwritten sheets. No books or note

3. Do everything on this exam, and make your methods as clear as possible.

Problem 1	/ 24	AVG = 69
Problem 2	/28	AV0 - 07
Problem 3	/24	J = 17.3
Problem 4	/24	
TOTAL	/ <i>100</i>	

MOS Device Data (you may not have to use all of these...)

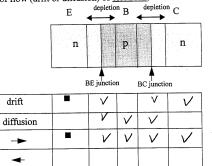
$$\begin{split} & \mu_n C_{ox} = 50 \mu A/V^2, \ \mu_p C_{ox} = 25 \mu A/V^2, \ V_{Tn} = -V_{Tp} = 1V, \ Lmin = 2 \mu m. \ V_{BS} = 0. \\ & \lambda_n = \lambda_p = 0.1 V^{-1} \ when \ L = 2 \mu m, \ and \ it is otherwise proportional to 1/L \\ & C_{ox} = 2.3 fF/\mu m^2, \ C_{jn} = 0.1 fF/\mu m^2, \ C_{jp} = 0.3 fF/\mu m^2, \ C_{jswn} = 0.5 fF/\mu m, \\ & C_{jswp} = 0.35 fF/\mu m, \ C_{ovp} = 0.5 fF/\mu m, \ C_{ovp} = 0.5 fF/\mu m \end{split}$$

$$\begin{array}{l} \underline{npn\ Data} \ I_S = 10^{-17}A, \, \beta = 100, \, V_A = 25V, \, \tau_F = 50ps, \, C_{je} = 15fF, \, C_\mu = 10fF \\ \underline{pnp\ Data} \ I_S = 10^{-17}A, \, \beta = 50, \quad V_A = 25V, \, \tau_F = 50ps, \, C_{je} = 15fF, \, C_\mu = 10fF \end{array}$$

Problem 1 of 4: Answer each question briefly and clearly. (4 points each, total 24)

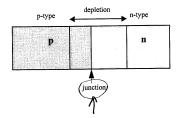
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Mark in the table below the npn Bipolar Transistor in forward action mode the direction of flow, and the type of flow (drift or diffusion) of electrons, in each of the bulk and depletion regions.

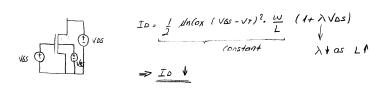


(place a mark at the appropriate box to indicate your answer. You can choose more than one box if appropriate.)

Where is the maximum |E| field in a forward-biased junction? Please place a mark on the graph



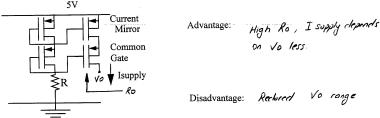
What happens to the drain current of an n-channel MOS transistor in saturation, when L and W increase proportionally? (i.e. L and W increase, but W/L stays constant. Assume that VGS, VBS and V_{DS} stay constant. Do take λ into account!)



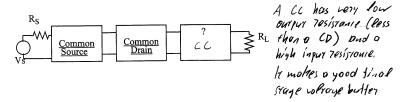
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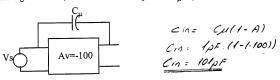
Name one advantage and one disadvantage of a MOS current source employing a CG buffer, versus one that does not employ one.



The following multistage amplifier is meant to deliver a voltage signal to a relatively small ohmic load of $1K\Omega$. Mark your choice of the last stage, and write a brief justification.



The following voltage amplifier has a voltage gain Av = -100. What is the capacitance "seen" by the signal source, due to the added capacitor $C_u = 1pF$ as shown?

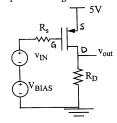


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Problem 2 of 4 (28 points)

The following p-channel common source amplifier uses a rather primitive current supply: it is a simple resistor $R_D=10k\Omega$ tied between drain and ground. $L=2\mu m, \, \lambda_p=0.1 V^{-1}$.



For each of the following questions, make sure that you show the expressions <u>before</u> you plug in the specific values. A correct expression is worth 70% of the credit, even if the numerical calculation is incorrect!

a) Find W/L so that when V_{BIAS} =3.5 and V_{in} = 0V, then Vout = 2.5V. Do take λ_p into account! Note that L=2 μ m. (4 points)

$$IO = \frac{2.5^{\vee}}{1040} = 250 \mu A \qquad IO = \frac{1}{2} \cdot \frac{\omega}{L} \quad \mu_{P}(ox. (Vas-Vip)^{2} (1+Vas. \lambda_{P}))$$

$$= \frac{2.5 Vas}{1040} = \frac{250 \mu A}{25 \mu A. (05)^{2} (1.25)} = \frac{\omega}{L} = 64$$

 $W/L = \frac{128}{2}$

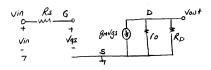
b) What is the minimum and the maximum output voltage for this amplifier? Make sure you mention the limiting reason for each case (i.e. transistor X falls out of saturation, or current source Y hits its minimum voltage drop, etc.). (4 points)

MIN Vout =
$$\Omega$$
 MIN Limited by: GNC

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c) Draw the small signal model <u>for this amplifier</u>, and calculate the values of g_m and r_o <u>for this transistor</u> (4 points).



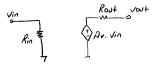
$$g_{m} = \frac{2 \text{ ID}}{(\sqrt{s} + \sqrt{t} p)} = \frac{\ell_{m} H}{V}$$

$$r_{0} = \frac{\ell}{\lambda_{1} T_{0}} = \frac{\ell_{1} \times 250 \mu H}{0.1 \times 250 \mu H} = 40 \text{ kg}$$

$$g_m = ImA/V$$

$$r_0 = 40 k\Omega$$

d) Draw the 2-port model for this circuit <u>as a voltage amplifier</u> and calculate the values of A_v , R_{in} and R_{out} . (4 points)

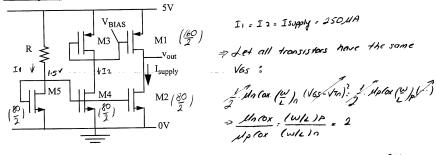


Parameter	Expression	Value
$A_{\mathbf{v}}$	- gm. (roll Ro)	- 8
R _{in}	∞	∞
R _{out}	(roll Ro)	8 k D

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e) In an attempt to increase the Av of this amp, we redesign it with a "real" biasing circuit as shown below. Calculate the value of the reference resistor and the $\underline{W/L}$ of the biasing transistors so that $I_{supply} = 250\mu A$ and $V_{BIAS} = 3.5V$. For this part do not take λ into account, and assume that the $\underline{W/L}$ of the amplifying transistor M1 is 160/2. (this is *not* the same value as the one you found in part a). Make it so that all three branches have the same current of $250\mu A$. (4 points)



=> make all NMOS transisters 80/2

Choose:

. $V_{655} = V_{651} = 1.5^{\circ} = 7 \quad I_{1} = \frac{5 - 1.5^{\circ}}{R} = 250 \mu A = 7 \quad \frac{3.5}{250 \mu A} = R$ $\mu_{42} = R$

Other choices for Vosz are possible, Monerer, it you choose Vosz > 1.5, you limit voltage suring. It you choose Vosz < 1.5, Mz become, roo large, so cap becomes a problem.

Transistor	W/L
M1	160/2
M2	80 12
M3	160 /2
M4	80 /2
M5	80 /2
Resistor	Value in Ω
R	14000

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f) What is the R_{in} , A_{v} and R_{out} of the new design? (4 points)

$$g_{m/2} = \frac{2 \times 250 \text{ MA}}{0.5} = 1 \frac{\text{mA}}{V}$$

$$10_1 : 10_2 = \frac{1}{\lambda_1} = 40 \text{ kg}$$

$$10_3 : 10_4 = \frac{1}{\lambda_4} = 40 \text{ kg}$$

Parameter	Expression	- Value -
A _v	- gm, (10,1102)	-20
R _{in}	∞	20
R _{out}	(ro,11/02)	2012

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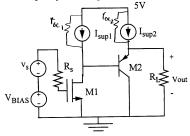
g) What is the minimum and the maximum output voltage of the new design? Make sure you mention the limiting reason for each case (i.e. transistor X falls out of saturation, or current source Y hits its minimum voltage drop, etc.). (4 points)

$$MIN V_{out} = 0.5$$
 $MIN Limited by: M2 falls out of saturation$

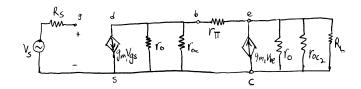
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Problem 3/4 (24 points)

The following is a two stage voltage amplifier employing a n-channel CS stage, and a pnp CC stage. Note that there are no numerical substitutions or calculations in parts a, b and c of this problem - just symbolic expressions!



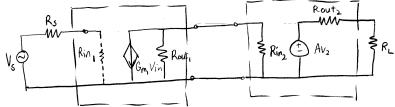
a) Draw the small signal model for this amplifier (Make sure to properly mark the g, s and d nodes for M1, and b, c, and e nodes for M2. Include r_{oc1} , r_{oc2} due to I_{sup1} and I_{sup2} , respectively). (6 points)



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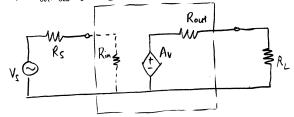
b) Draw the two stage amp 2-port model (i.e. draw one 2-port of each stage and connect them properly together. CS is a transconductance amp, CC is a voltage amp). Write the *expressions* for the quantities shown below, in terms of the device parameters, r_{ocl} , r_{oc2} and R_s and R_L as needed. (OK to use the simplified formulae). (6 points)



Parameter	Expression
Gm ₁	gm,
R _{in1}	∞
R _{out1}	ro, Ilroc,
Av ₂	
R _{in2}	r _π + β. (r. r.
R _{out2}	$\frac{1}{g_{m_2}} + \frac{R_{out_1}}{\rho_o}$

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c) Draw the <u>overall voltage amp</u> 2-port for the entire amp (i.e. draw one 2-port that represents the entire 2-stage amp), and derive *expressions* for the A_v , R_{in} , R_{out} , as well as v_{out}/v_s in terms of the device parameters, and r_{ocl} , r_{oc2} , R_s and R_L , as needed. (6 points)



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$$A_{V} = -G_{m_{1}}(R_{out}, IIR_{in_{2}})$$

$$\frac{V_{out}}{V_{S}} = A_{V} \cdot \frac{R_{L}}{R_{L} + R_{out}}$$

Parameter	Expression	
R _{in}	∞ '	
R _{out}	J + Rout, Po	
A _v	-9m1(ro1/1roc1)[[rπ+β.(ro2/1roc2/1RL)])	
v _{out} /v _s	-gm, (ro, 11 roc, 1) [rπ + βο (roz 11 roc 2 11 RL)] - RL+ fm2 + Ros	

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d) Assume that $V_{BIAS} = 1.5V$, and that the minimum voltage across the current sources is 0.5V. Find the maximum and minimum voltages at the drain of M1 and at the emitter of M2. Make sure you mention the limiting reason for each case (i.e. transistor X falls out of saturation, or current source Y hits its minimum voltage drop, etc.) (6 points)

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•
$$V_{dmax} \neq 4.5V$$
 because $V_{e} = 4.5V + 0.7V = 5.2V > V_{DD}$
 $V_{emax} = \boxed{4.5V}$.: $V_{dmax} = 4.5V - 0.7V = \boxed{3.8V}$

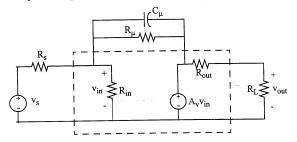
Node	Min Voltage	Reason for Min Voltage	Max Voltage	Reason for Max Voltage
drain of M1	O. 5V	Vpsat of MI	3.8V	Min voltage across Isupz & VEB of M2
emitter of M2	1,2V	VIsat of MI & VEB of M2	4.5V	Min voltage across 1sup2

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Problem 4/4 (24 points)

The following is the 2-port representation of a voltage amplifier, where the "Miller" elements C_{μ} and R_{ν} have been added as shown.

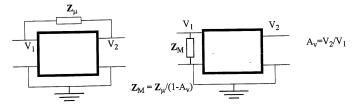
 $A_{v} = -100, R_{s} = 5k\Omega, R_{in} = 5k\Omega, R_{out} = 5k\Omega, R_{L} = 5k\Omega, C_{\mu} = 0.4pF, R_{\mu} = 100k\Omega.$



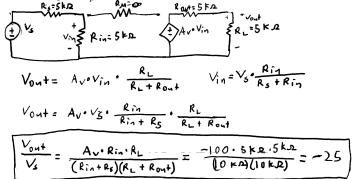
Miller Approximation Refresher:

Note that the Miller approximation applies to any kind of complex impedance connected between the nodes that exhibit voltage gain A_v . In general, $\mathbf{Z}_M = \mathbf{Z}_\mu/(1-A_v)$. (Here a **bold** symbol indicates a complex number). As you know, for capacitors, $\mathbf{Z}_\mu = 1/\mathrm{jo}\,C_\mu$, so it turns out that $C_M = C_\mu(1-A_v)$. Below you will be asked to apply the Miller approximation for capacitors, as well as for resistors

Miller approximation refresher: these two circuits are almost equivalent.



a) For the voltage amplifier shown in the previous page, find the overall \underline{DC} gain (v_{out}/v_s) with no Miller resistor in place ($R_u = infinity$). (5 points)



b) Find the overall
$$\underline{DC}$$
 gain expression and evaluate it when $R_{\mu} = 100 \text{ k}\Omega$. (5 points)
$$R_{M} = 100 \text{ k}\Omega \qquad R_{M} = \frac{100 \text{ k}\Omega}{(1+100)} \approx |\text{k}\Omega|$$

$$R_{in} = \frac{5 \text{ k}\Omega \cdot 1 \text{ k}\Omega}{6 \text{ k}\Omega} = 0.83 \text{ k}\Omega$$

$$\frac{V_{out}}{V_{s}} = \frac{A_{s}(R_{in}||R_{M})}{(R_{in}||R_{M}+R_{s})} \frac{R_{L}}{(R_{in}||R_{M}+R_{s})} = \frac{-100 \cdot (0.83 \text{ k}\Omega)(5 \text{ k}\Omega)}{5.83 \text{ k}\Omega \cdot 10 \text{ k}\Omega} = -7.143$$

	Expression		Value for $R_{\mu} = 100 k\Omega$
v _{out} /v _s	Av·(Rinll Pm)·RL	Pm = PH/(1-AV)	-7,143
	(RinllRm+Rs)(RL+Rout)	-	

c) Find the ω_{3db} of $|v_{out}/v_s|$ when R_μ is infinity and when R_μ is $100k\Omega$. Hint: apply the Miller approximation to the resistor and the capacitor separately. It is not necessary to solve this considerable. ering the complex impedance of the resistor and capacitor taken together. (5 points)

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$$C_{M} = 0.4 \text{ pF} \qquad C_{m} = 101 \cdot C_{M} \approx 40 \text{ pF}$$

$$for \quad R_{M} = \infty$$

$$R = R_{S} || R_{1n} = 2.5 \text{ k/2}$$

$$R \cdot C_{m} = 10^{-7} \text{ sec} \implies W_{3db} = \frac{1 \cdot R_{ad}}{10^{-7} \text{ sec}} = 10 \text{ M cad/sec}$$

$$for \quad R_{M} = 100 \text{ k/2} \qquad R_{m} = 1 \text{ k/2}$$

$$R = R_{S} || R_{1n} || R_{M} = \frac{-2.5 \text{ k/2} \cdot 1 \text{ k/2}}{3.5 \text{ k/2}} = 0.714$$

$$R \cdot C_{m} = 2.86 \times 10^{-8} \text{ sec} \implies W_{3db} = \frac{1 \cdot R_{ad}}{2.86 \times 10^{-8} \text{ sec}} = 35 \frac{\text{m rad}}{\text{sec}}$$

	Expression	Value in Mrad/sec
ω_{3db} for R_{μ} infinity	(R s 11 Rin) Cm (p(1-Av) Rm = Rp(1-Av)	- 40 -
ω3db for $Rμ = 100kΩ$	(Rsll Rin Rm) Cm	35

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d) Draw Bode plots on the same graph for $|v_{out}/v_s|$ when R_μ infinity and R_μ =100k Ω . (5 points)

For RM=100 FR

Gain $|v_{out}/v_s|$ (db) $R_{\bullet} = \sigma$ this port is common for both curves, since the have the same KW=100 FD Gain X Bandwidth: +20-25 × 10 ~ 7.143 × 35 350 35 10 ___100 (Mrad/sec)

-340+ e) Derive an expression for the Gain X Bandwidth product of this amplifier. Do not substitute any values. Simplify this expression assuming that $|A_v| >> 1$, $R_\mu / |A_v| << R_s$ and $R_\mu / |A_v| << R_{in}$. (4 points)

Gain =
$$\frac{Rin ||(R\mu/(1-A\nu))}{|Rs+Rin||(R\mu/(1-A\nu))}.$$

 $Can = \frac{Rin || (R\mu/(1-A\nu))}{|R_s + Rin|| (R\mu/(1-A\nu))} \cdot \frac{A\nu \cdot RL}{|R_{out} + RL|} \quad BW = \frac{C_M \cdot (\frac{R\mu}{-A\nu}||R_s||R_{in})}{|C_{\mu}(1-A\nu)(\frac{R\mu}{A\nu})||R_s||R_{in})}$ $Row = \frac{c_{\mu}(1-A\nu)(\frac{R\mu}{A\nu})||R_s||R_{in}|}{|C_{\mu}(1-A\nu)(\frac{R\mu}{A\nu})||R_s||R_{in}|}$ $|-A\nu| \approx -4\nu$