Common-Source Amplifier

- “Common” means “grounded” or more generally, “connected to a DC supply”

DC Bias Point of the Common-Source Amplifier

For biasing, we
1. ignore the small-signal source vs and its small-signal resistance: $R_s \to 0 \, \Omega$
2. ignore the load resistor (since it’s a small-signal resistance, too): $R_L \to \infty \, \Omega$

What is going on with the load resistor $R_L$?
DC level of the output voltage is NOT zero ... but
A “typical load” does not draw much if any DC current ... because it is non-linear and the load resistor is the load’s small-signal model!
What is a “typical load”?

Where to set $V_{OUT}$?
Graphical “Load-Line” Analysis

The current through $R_D$ must equal the drain current.

$$I_D = \frac{V_{DD} - V_{OUT}}{R_D} = I_R$$

What does this equation mean?

Small-Signal Model of CS Amplifier

- Substitute parameters at operating point selected so that $V_{OUT} = V_{DD}/2$

- Find two-port parameters of this amplifier:
  “natural” to use the transconductance form

$$R_{in} =$$

$$R_{out} =$$

$$G_m =$$
Two-Port Model of Common-Source Amplifier

- Attach the source and load to find output current as a function of the source voltage

Infinite input resistance is ideal for a voltage input

Output resistance increases with \( R_D \) increasing, but DC drain current \( I_D \) will decrease and \( r_m \) will decrease with \( I_D^{1/2} \)

Current-Source Supplies

- A current source to supply current, rather than a resistor, allows a high DC current for the device with a large incremental (small-signal) resistance

The plot of \( i_{SUP} \) vs. \( v_{SUP} \) is: (note that \( v_{SUP} \) must be positive)
Common-Source with Current Source Supply

- $R_D$ is replaced with idealized current source with internal resistance

For DC bias analysis, the small-signal source (with $R_S$) and the load resistor $R_L$ are eliminated, along with the internal resistance $r_{oc}$ of the current source.

Graphical Analysis of CS Amplifier with Current-Source Supply

The region of input bias voltage $V_{BIAS}$ for which the current source and the MOSFET are in their constant-current regions is extremely small.
Common-Source/Current-Source Supply Models

- The small-signal model is identical to the resistor supply, except that the current source's internal resistance $r_{oc}$ replaces $R_D$.

Tradeoffs are different from case of resistor load since $I_D$ is now decoupled from the small-signal current supply resistance $r_{oc}$.

p-Channel Common-Source Amplifier

- Source of p-channel is tied to positive supply; current supply sinks $I_{SUP}$ to ground or to lower supply.

- DC bias:
  Eliminate small-signal sources; control voltage is $V_{SG} = V_{DD} - V_{BIAS}$. 

![p-Channel Common-Source Amplifier Diagram]
p-Channel CS Small-Signal Model

- p-channel MOSFET small-signal model has the source at the top

Transform this into a circuit with $v_{gs}$ as the control voltage

Common Gate Amplifiers

- Input signal is applied to the source, output is taken from the drain
- Summary:
  current gain is about unity, input resistance is low, output resistance is high
  a CG stage is a current “buffer” ... it takes a current at the input that may have a relatively small Norton equivalent resistance and replicates it at the output port, which is a good current source due to the high output resistance.

Biasing is very easy ... $I_{BIAS} = -I_{SUP}$
Note that the source can be tied to the bulk if the device is in a well.
Common-Gate Current Gain $A_i$

- Small-signal circuit, with output shorted (according to the two-port procedure to find $A_i$)

Analysis: $i_{out} = i_d$ and $i_d = -i_g - i_s = -i_s = -i_i$

Solving for the short-circuit current gain:

$$A_i = \frac{i_{out}}{i_i} = -1$$

Common-Gate Input Resistance $R_{in}$

- Apply test current, with load resistor $R_L$ present at the output

Add the currents at the input node and set equal to the test current:

$$i_t = -g_m v_{gs} + g_m v_t + \left(\frac{v_t - v_{out}}{r_o}\right)$$

The output voltage $= -i_{out} (r_o \parallel R_L) = -(-i_t) (r_o \parallel R_L)$ (why?)

$$i_t = g_m v_{gs} + g_m v_t + \left(\frac{v_t - v_{out}}{r_o}\right)$$
Input Resistance (Cont.)

- Solve for the ratio of the test voltage to the test current

\[ R_{in} = \frac{\frac{v_t}{i_t}}{\frac{1}{g_m + g_{mb}} + \frac{1}{r_o}} \]

the input resistance is a function of the load resistance \( R_L \) ...

- Evaluate the relative sizes of the terms:

  - \( g_m \) is around 500 \( \mu \text{S} \)
  - \( g_{mb} \) is around 50 \( \mu \text{S} \)
  - \( 1/r_o \) is around 5 \( \mu \text{S} \) or less, so neglect versus \( g_m + g_{mb} \)

  current supply is usually good enough that \( r_{oc} \parallel R_L \approx R_L \)

- What about ratio of \( R_L \) and \( r_o \)? It depends ...

  \( R_{in} = \frac{v_t}{i_t} = \frac{1 + R_L}{g_m + g_{mb}} \)

  \( R_{in} \approx \frac{1}{g_m + g_{mb}} \) \( \frac{1}{g_m} \) \( \text{for } r_{oc}, r_o >> R_L \)

Common-Gate Output Resistance \( R_{out} \)

- Test circuit: leave source resistance \( R_S \) of small-signal source current in place; remove \( r_{oc} \) for analysis and put it back in at the end ...

\[ \begin{align*}
  &v_s \\
  &\downarrow
\\
  &R_S
\\
  &\downarrow
\\
  &g_{mb}
\\
  &\downarrow
\\
  &v_{gs}
\\
  &\downarrow
\\
  &v_t
\\
  &\downarrow
\\
  &\downarrow
\\
  &r_o
\\
  &\downarrow
\\
  &i_t
\\
  &\downarrow
\\
  &v_o
\\
\end{align*} \]

- Circuit analysis exercise:

  \( \text{it helps to note that } v_s = i_t R_S \)

- Kirchhoff’s current law at the source resistor node: sum currents leaving node

\[ \frac{v_s}{R_S} + \frac{v_t}{g_m} - \frac{g_{mb}v_t}{r_o} + \frac{v_s - v_t}{r_o} = 0 \]

\[ v_s \left( \frac{1}{R_S} + \frac{g_m + g_{mb} + 1}{r_o} \right) = \frac{v_s}{r_o} \]

- Substituting \( v_s = i_t R_S \) and solving for the output resistance \( = (v_t / i_t) \parallel r_{oc} \)

\[ R_{out} = r_{oc} \parallel \left[ \left( R_S R_o / R_S + (g_m r_o + g_{mb} r_o + 1) \right) \right] \]

... quite a mess
The output resistance is a function of the source resistance $R_S$.

Evaluate the relative sizes of the terms:
- $g_m$ is around 500 $\mu$S
- $g_{mb}$ is around 50 $\mu$S
- $r_o$ is around 200 k$\Omega$

$g_m r_o = (0.5)(200) = 100 >> 1$

Simplifying

$$R_{out} = r_o \left[ (r_o + (g_m r_o + g_{mb} r_o) R_S) \right] = r_o \left[ (1 + (g_m + g_{mb}) R_S) \right]$$

If we neglect the backgate generator ($g_{mb} \ll g_m$)

$$R_{out} = r_o \left[ r_o (1 + (g_m R_S)) \right]$$

The output resistance of the common-gate can be very large ... on the order of 100 times $r_o$ ... if the current supply’s resistance is large enough not to limit it.

Design tradeoffs:
- Ideal current buffer has $R_{in} = 0$ $\Omega$: need to increase $g_m$ to approach this goal.
- Also, an ideal current buffer has $R_{out} = \infty$ $\Omega$: increase $g_m r_o$ ... and use a good current supply with a large $r_{oc}$.
P-Channel Common Gate Amplifier

Small-signal model is identical to n-channel version

Common-Drain Amplifier

- Also called a “source follower” for reasons that will become clear shortly

For DC bias, neglect small signal source (and its resistance) and the small-signal load resistance; $i_{SUP} = I_{SUP}$

Note that

$$V_{OUT} = V_{BIAS} - V_{GS}$$

The DC gate-source voltage is:
DC Transfer Curve

p-well CMOS process means that the source and bulk can be shorted ... not true for an n-well process.

The threshold voltage $V_{Th}$ is not a constant, since the source-bulk voltage $V_{SB}$ increases as $V_{OUT}$ increases:

$$V_{Th} = V_{ToN} + \gamma_n \left( (V_{OUT} - V) - \frac{2v_p}{\sqrt{2v_p}} \right)$$

DC Transfer Curve for Common-Drain Amps

Simple idea: slope of transfer curve is the voltage gain ... about 1

The common-drain is a voltage buffer

$$A_v = \frac{dV_{OUT}}{dV_{BIAS}} = 1$$
Common-Drain Open-Circuit Voltage Gain

For finding $A_v$ exactly, remove the source and its resistance and the load resistance and apply a test voltage and find the output voltage

$$A_v = \frac{v_{out}}{v_i} = \frac{g_m}{g_m + g_{mb} + \left(\frac{1}{r_{oc}}\right)_{ro}} \approx \frac{g_m}{g_m + g_{mb}}$$

KCL at source node:

$$\frac{v_{out}}{r_{oc}} - g_m(v_i - v_{out}) - (-g_{mb}v_{out}) = 0$$

$$v_{out}\left(\frac{1}{r_{oc}}\right) + g_m = g_m v_i$$

Output Resistance of Common-Drain Amplifier

- Leave the source resistance attached while exercising the output with a test voltage

KCL at the source node ... remove $r_s || r_{oc}$ and put it back in

$$i_t + g_m(0 - v_i) + (-g_{mb}v_i) = 0$$

$$R_{out} = \frac{(r_o || r_{oc})}{v_i} = \frac{(r_o || r_{oc})}{\left(g_m + g_{mb}\right)} = \frac{1}{1/(r_o || r_{oc}) + g_m + g_{mb}}$$

Typically, $r_o || r_{oc} >> g_m + g_{mb}$

$$R_{out} \approx \frac{1}{g_m + g_{mb}}$$
**Common-Drain Small-Signal Model**

Input resistance is infinite: open-circuit from gate-source

\[ V_{gs} \]

\[ V_{ds} \]

\[ g_m \left( g_m + g_{mb} \right) \]

\[ V_{ds} \]

\[ V_{gs} \]

If source and bulk can be shorted (possible for a MOSFET in a well), then the gate is essentially 1 (since backgate generator has zero \( v_{sb} \) controlling it.)

Output resistance is ideally zero for a voltage-output amplifier: typical values

\[ g_m = 500 \mu S \]
\[ g_{mb} = 50 \mu S \]

\[ R_{\text{out}} = \frac{1}{g_m + g_{mb}} = 2 \text{k}\Omega \]

The output resistance can be reduced by increasing the transconductance ... 
\((W/L)\) can be made huge in order to drive \( R_{\text{out}} \) toward zero.

**Summary of MOSFET Two-Port Models**

<table>
<thead>
<tr>
<th>Transistor Type</th>
<th>MOSFET</th>
<th>PMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Common Source/ Common Emitter (CS/CE)</td>
<td>( V_{gs} )</td>
<td>( V_{ds} )</td>
</tr>
<tr>
<td>Common Gate/ Common Base (CG/CC)</td>
<td>( i_{gs} )</td>
<td>( i_{ds} )</td>
</tr>
<tr>
<td>Common Drain/ Common Cathode (GD/CC)</td>
<td>( V_{ds} )</td>
<td>( V_{gs} )</td>
</tr>
</tbody>
</table>

\[ \left( g_m + g_{mb} \right) \cdot V_{gs} \]

\[ \left( g_m + g_{mb} \right) \cdot V_{ds} \]
Assessment of MOS Amplifiers

Common-source is the only stage that provides gain

Common-gate can buffer a poor current source into a nearly ideal one

Common-drain can buffer a poor voltage source into a nearly ideal one

We need more than one stage to approach an ideal amplifier (of any of the 4 types)