Lecture 11: MOS Transistor

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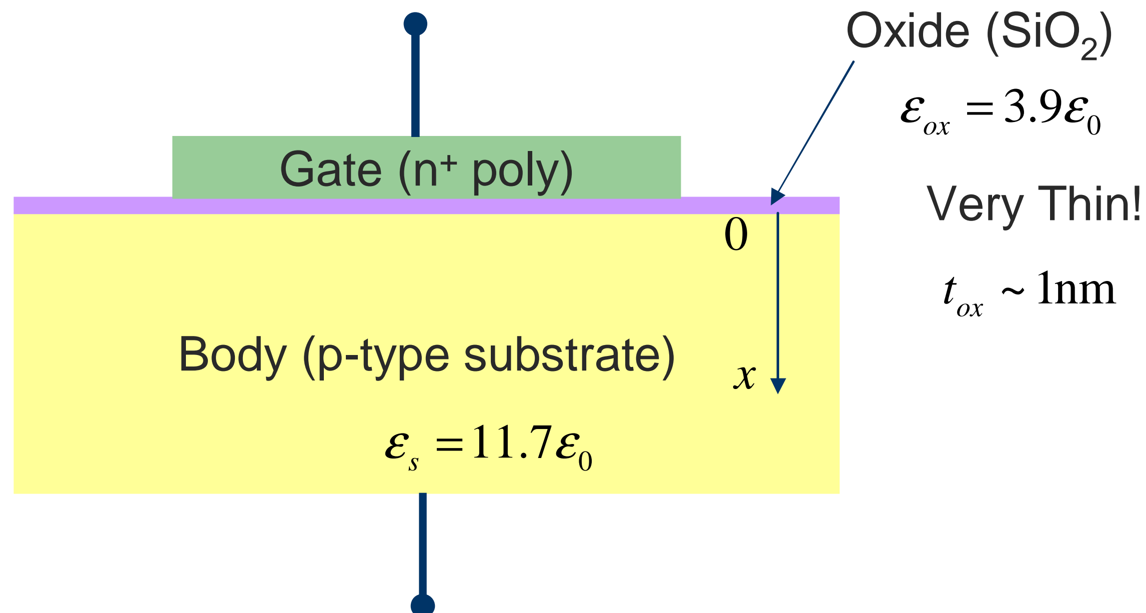
Lecture Outline

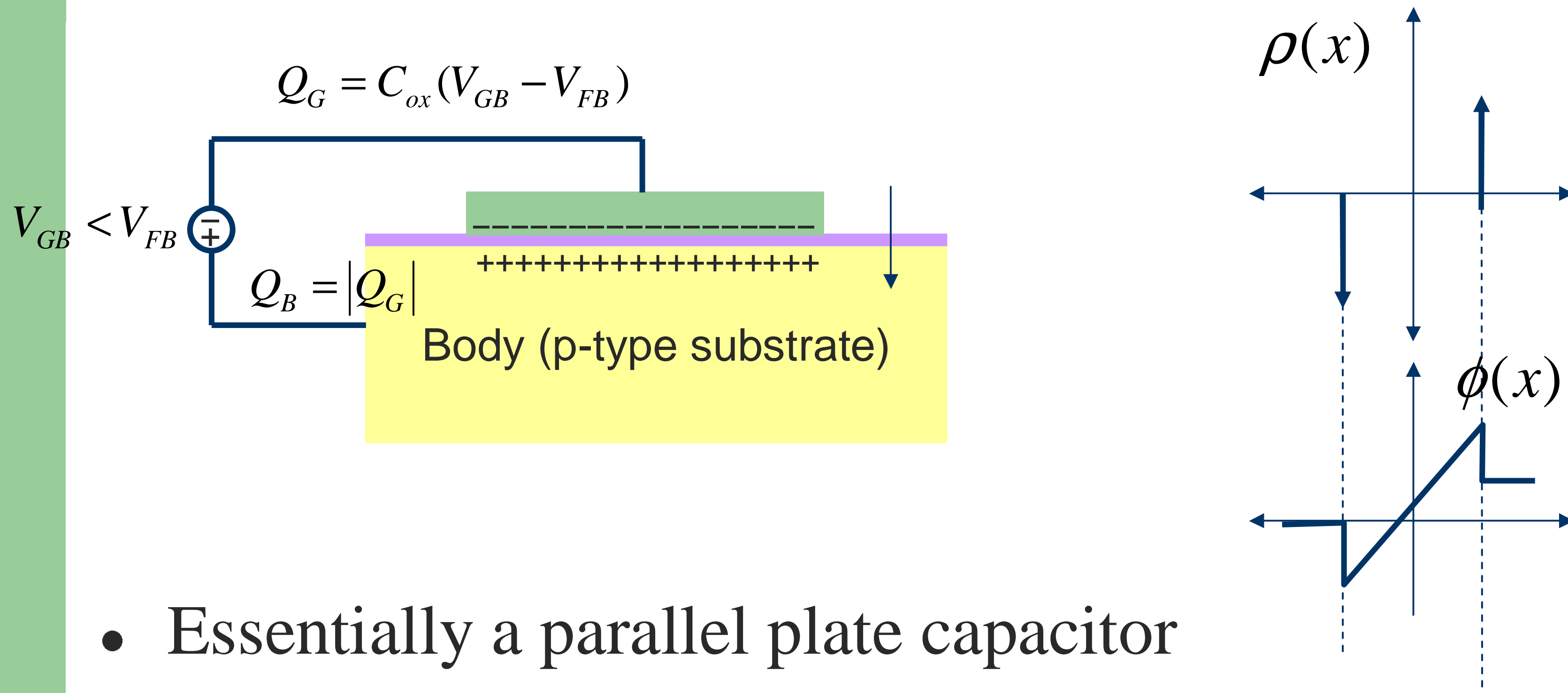
- Review: MOS Capacitors Regions
- MOS Capacitors (3.8 – 3.9)
  - CV Curve
  - Threshold Voltage
- MOS Transistors (4.1 – 4.3):
  - Overview
  - Cross-section and layout
  - I-V Curve

MOS Capacitor



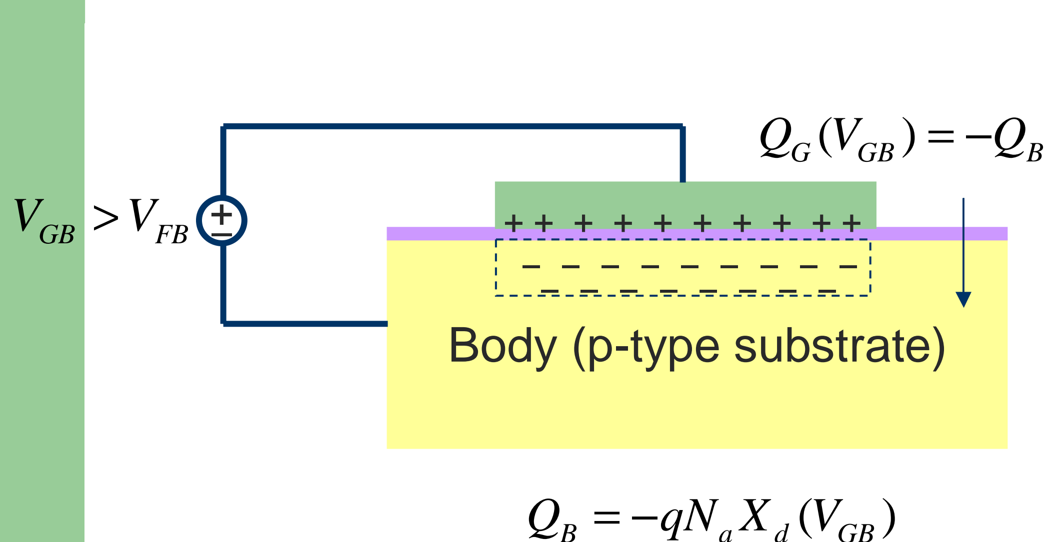
- MOS = Metal Oxide Silicon
- Sandwich of conductors separated by an insulator
- "Metal" is more commonly a heavily doped polysilicon layer n^+ or p^+ layer
- NMOS → p-type substrate, PMOS → n-type substrate

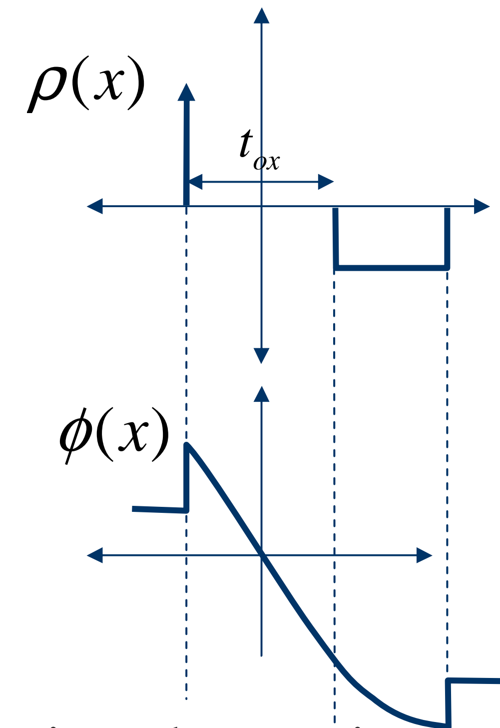
Accumulation: $V_{GB} < V_{FB}$



- Essentially a parallel plate capacitor
- Capacitance is determined by oxide thickness:

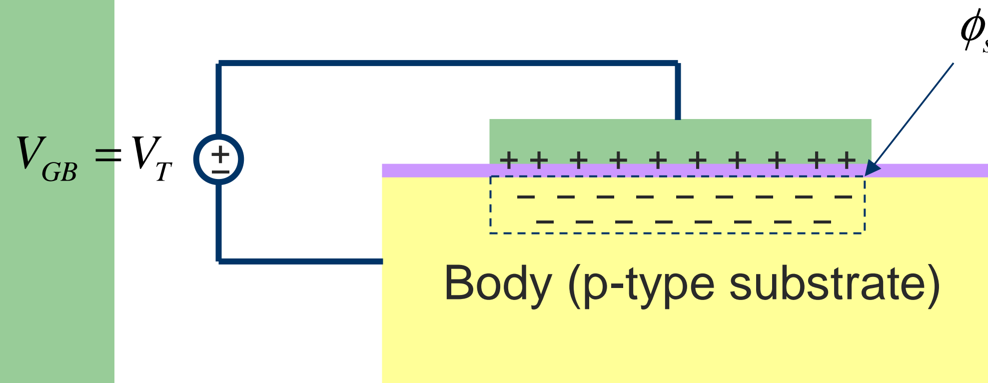
Depletion: $V_{FB} < V_{GB} < V_T$

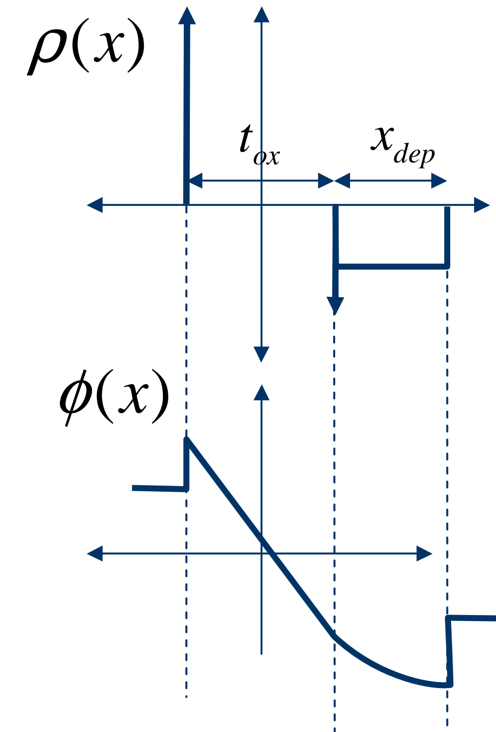




- Positive charge on gate terminates on negative charges in depletion region
- Potential drop across the oxide and depletion region
- Charge has a square-root dependence on applied bias

Inversion



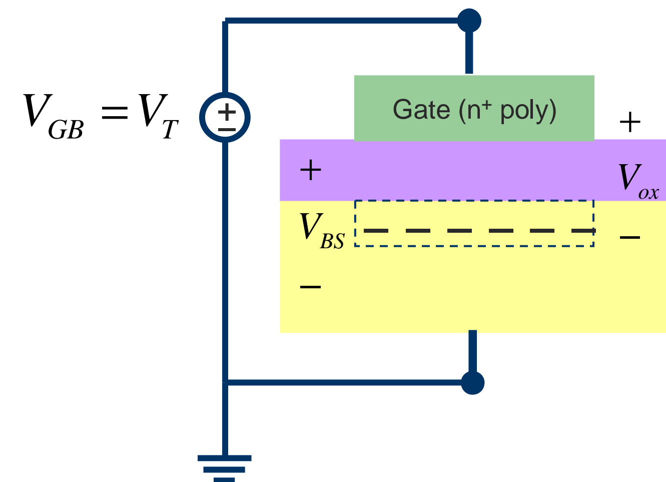


$$n_s = n_i e^{\frac{q\phi_s}{kT}} = N_a$$

- The surface potential increases to a point where the electron density at the surface equals the background ion density
- At this point, the depletion region stops growing and the extra charge is provided by the inversion charge at surface

Threshold Voltage

- The threshold voltage is defined as the gate-body voltage that causes the surface to change from p-type to n-type
- For this condition, the surface potential has to equal the negative of the p-type potential
- Apply KCL around loop:



$$V_{GS} = V_{FB} + V_{ox} + V_{BS}$$

$$\phi_s = V_{BS} = -2\phi_p$$

$$V_{ox} = E_{ox} t_{ox} = \frac{\varepsilon_s}{\varepsilon_{ox}} t_{ox} E_s$$

$$E_s = \frac{qN_a x_{dep}}{\varepsilon_s} = \frac{qN_a}{\varepsilon_s}\sqrt{\frac{2\varepsilon_s}{qN_a}\phi_s} = \sqrt{\frac{2qN_a(-2\phi_p)}{\varepsilon_s}}$$

$$V_{Tn} = V_{FB} - 2\phi_p + \frac{1}{C_{ox}}\sqrt{2q\varepsilon_s N_a(-2\phi_p)}$$

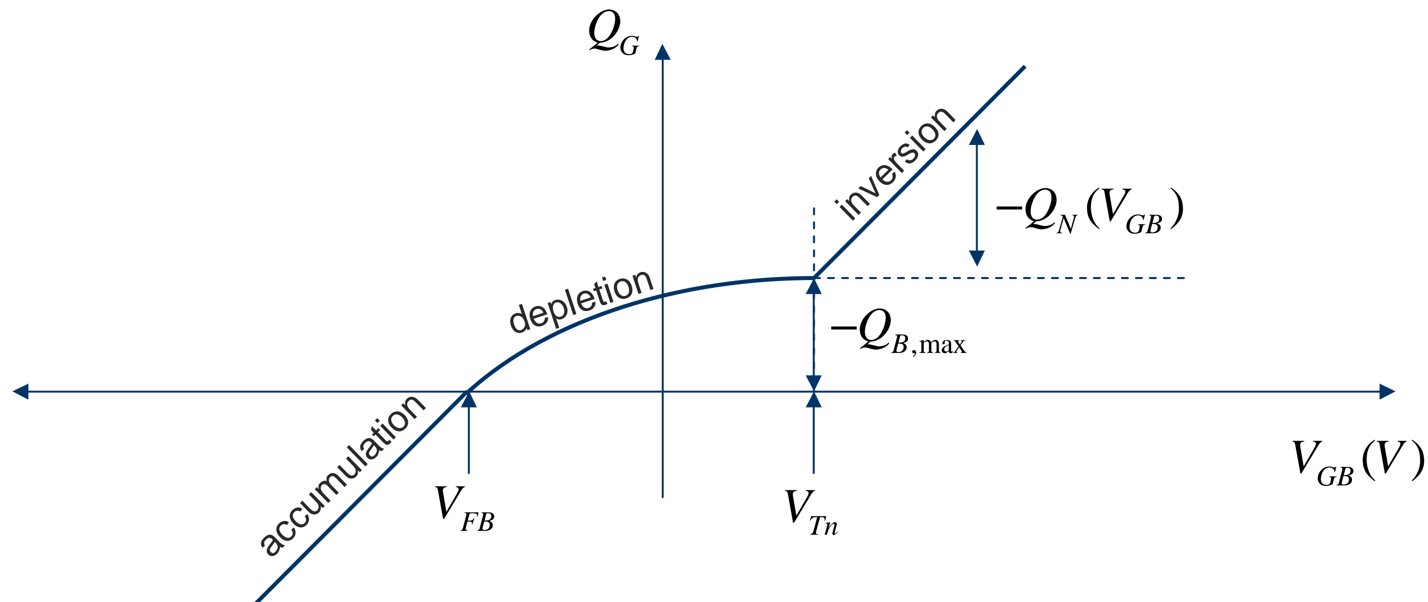
Inversion Stops Depletion

- A simple approximation is to assume that once inversion happens, the depletion region stops growing
- This is a good assumption since the inversion charge is an exponential function of the surface potential
- Under this condition:

$$Q_G(V_{Tn}) \approx -Q_{B,\max}$$

$$Q_G(V_{GB}) = C_{ox}(V_{GB} - V_{Tn}) - Q_{B,\max}$$

Q-V Curve for MOS Capacitor



- In accumulation, the charge is simply proportional to the applies gate-body bias
- In inversion, the same is true
- In depletion, the charge grows slower since the voltage is applied over a depletion region

Numerical Example

- MOS Capacitor with p-type substrate:

$$t_{ox} = 20\text{nm} \qquad N_a = 5\times10^{16}\,\text{cm}^{-3}$$

- Calculate flat-band:

$$V_{FB} = -(\phi_{n^+} - \phi_p) = -(550 - (-402)) = -0.95\text{V}$$

- Calculate threshold voltage:

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.45\times10^{-13}\,\text{F/cm}}{2\times10^{-6}\text{cm}}$$

$$V_{Tn} = V_{FB} - 2\phi_p + \frac{1}{C_{ox}}\sqrt{2q\varepsilon_s N_a(-2\phi_p)}$$

$$V_{Tn} = -.95 - 2(-0.4) + \frac{\sqrt{2\times1.6\times10^{-19}\times1.04\times10^{-12}\times5\times10^{16}\times2\times0.4}}{C_{ox}} = 0.52\text{V}$$

Num Example: Electric Field in Oxide

- Apply a gate-to-body voltage:

$$V_{GB} = -2.5 < V_{FB}$$

- Device is in accumulation
- The entire voltage drop is across the oxide:

$$E_{ox} = \frac{V_{ox}}{t_{ox}} = \frac{V_{GB} + \phi_{n^+} - \phi_p}{t_{ox}} = \frac{-2.5 + 0.55 - (-0.4)}{2 \times 10^{-6}} = -8 \times 10^5 \frac{\text{V}}{\text{cm}}$$

- The charge in the substrate (body) consist of holes:

$$Q_B = -C_{ox}(V_{GB} - V_{FB}) = 2.67 \times 10^{-7}\ \text{C/cm}^2$$

Numerical Example: Depletion Region

- In inversion, what's the depletion region width and charge?

$$V_{B,\max} = \phi_s - \phi_p = -\phi_p - \phi_p = -2\phi_p = 0.8\text{V}$$

$$V_{B,\max} = \frac{1}{2}\left(\frac{qN_a}{\varepsilon_s}\right) X_{d,\max}^2$$

$$X_{d,\max} = \sqrt{\frac{2\varepsilon_s V_{B,\max}}{qN_a}} = 144\text{nm}$$

$$Q_{B,\max} = -qN_a X_{d,\max} = -1.15\times 10^{-7}\,\text{C/cm}^2$$

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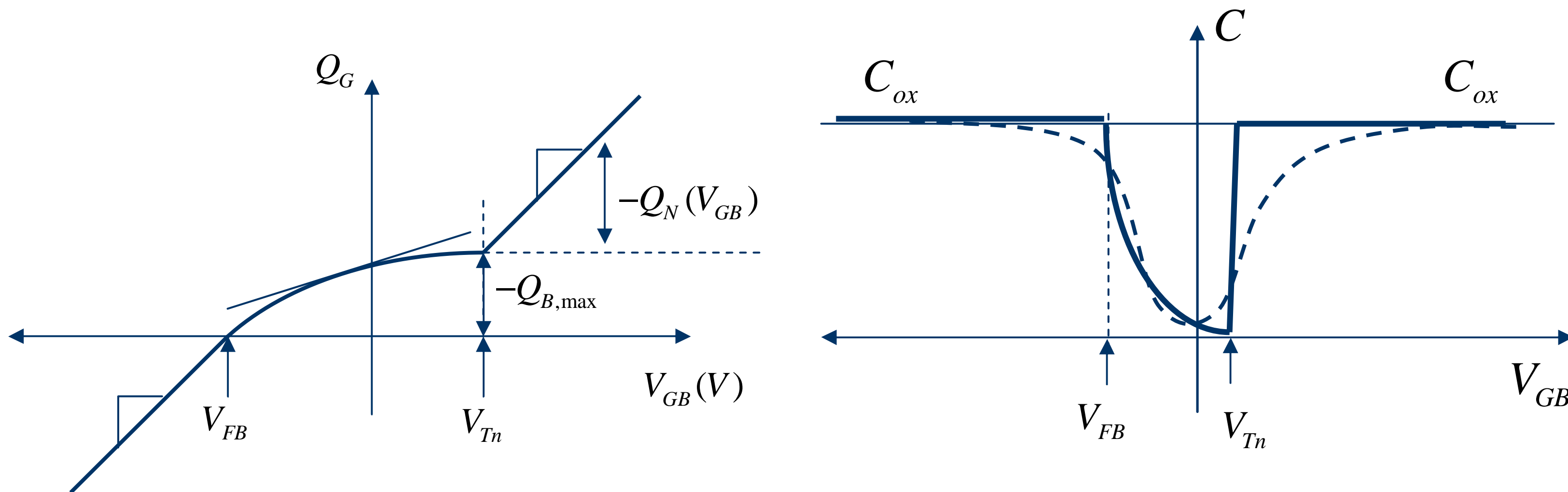
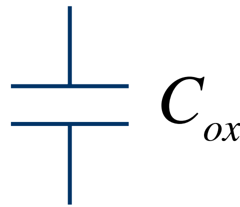
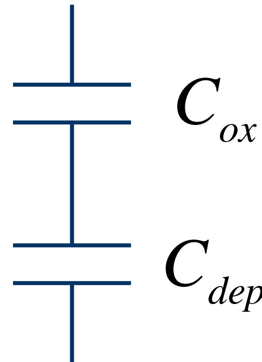
MOS CV Curve

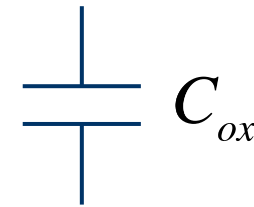


- Small-signal capacitance is slope of Q-V curve
- Capacitance is linear in accumulation and inversion
- Capacitance is depletion region is smallest
- Capacitance is non-linear in depletion

C-V Curve Equivalent Circuits



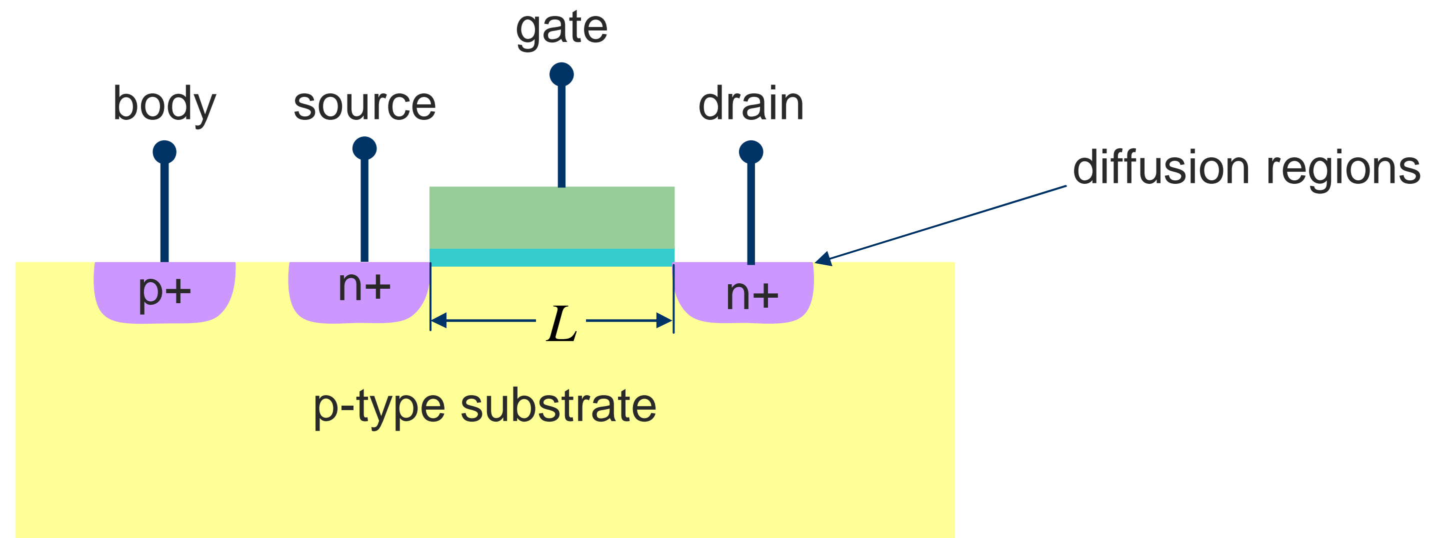




$$C_{dep} = \frac{\varepsilon_s}{x_{dep}} \qquad C_{tot} = \frac{C_{dep} C_{ox}}{C_{dep} + C_{ox}} = \frac{C_{ox}}{1 + \frac{C_{dep}}{C_{ox}}} = \frac{C_{ox}}{1 + \frac{\varepsilon_s}{\varepsilon_{ox}} \frac{t_{ox}}{x_{dep}}}$$

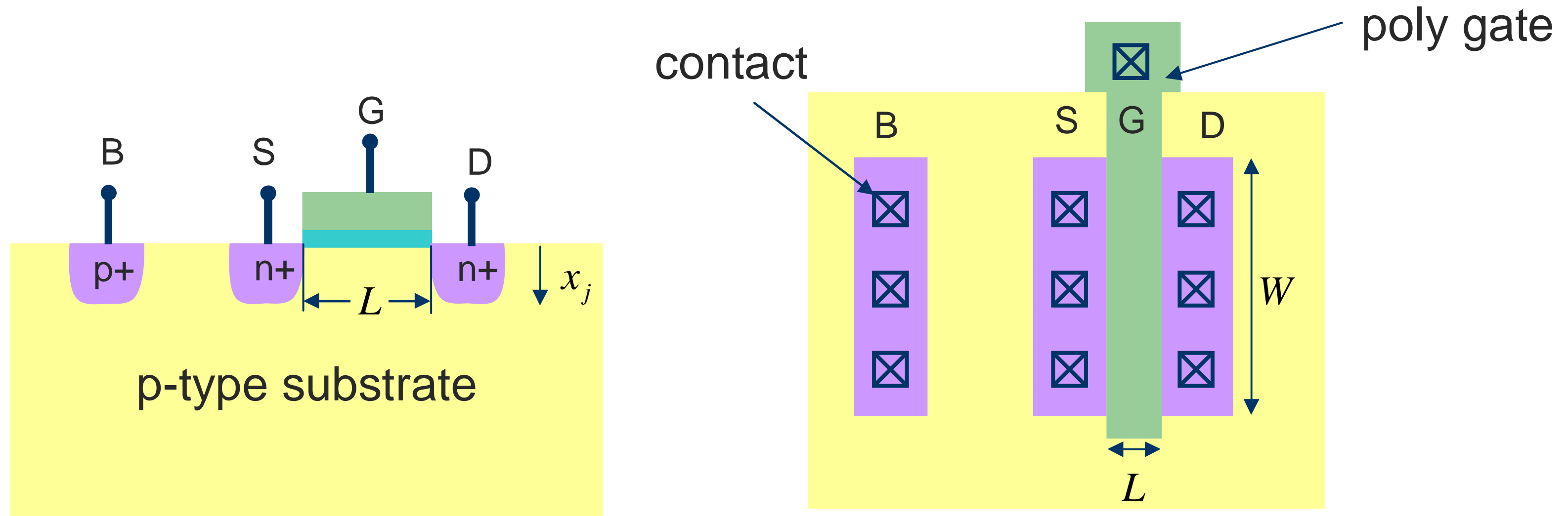
- In accumulation mode the capacitance is just due to the voltage drop across t_{ox}
- In inversion the incremental charge comes from the inversion layer (depletion region stops growing).
- In depletion region, the voltage drop is across the oxide and the depletion region

MOSFET Cross Section



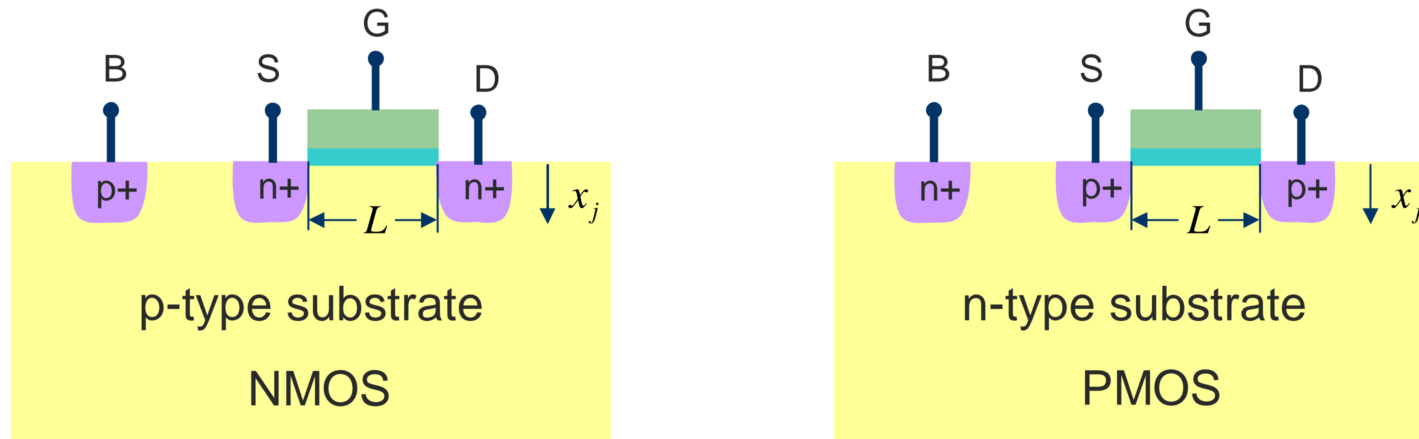
- Add two junctions around MOS capacitor
- The regions forms PN junctions with substrate
- MOSFET is a four terminal device
- The body is usually grounded (or at a DC potential)
- For ICs, the body contact is at surface

MOSFET Layout



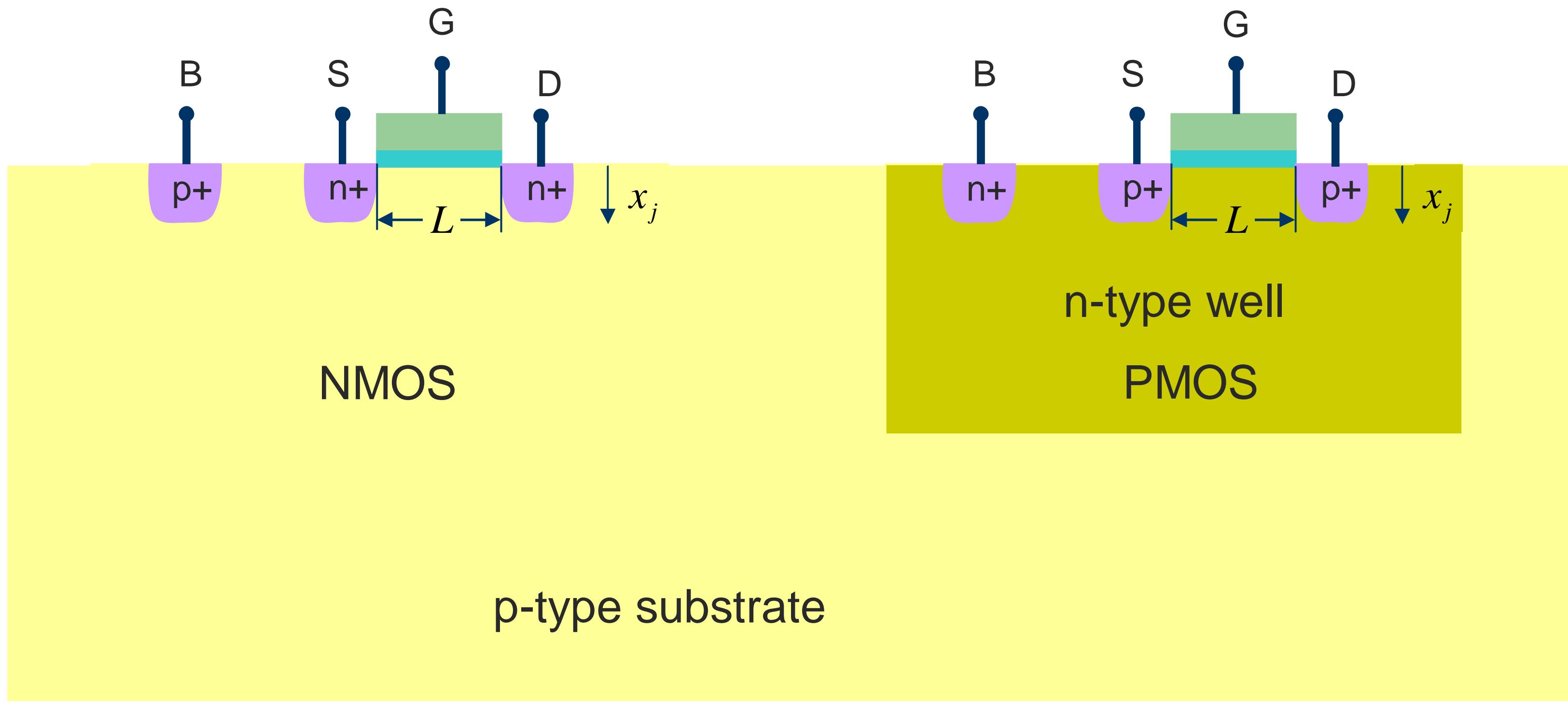
- Planar process: complete structure can be specified by a 2D layout
- Design engineer can control the transistor width W and L
- Process engineer controls t_{ox}, N_a, x_j, etc.

PMOS & NMOS



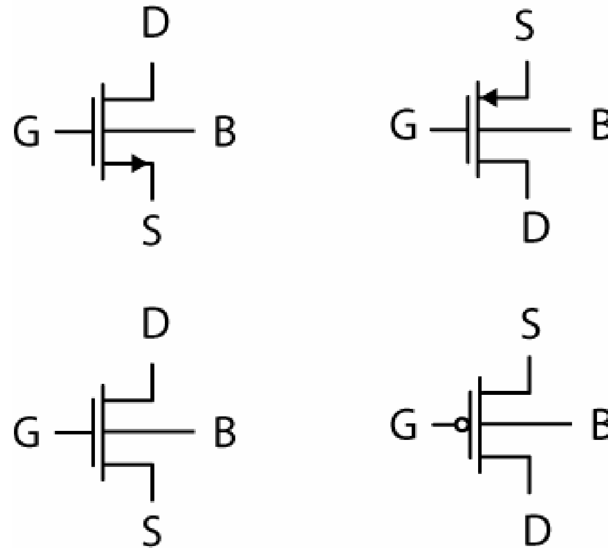
- A MOSFET by any other name is still a MOSFET:
  - NMOS, PMOS, nMOS, pMOS
  - NFET, PFET
  - IGFET
  - Other flavors: JFET, MESFET
- CMOS technology: The ability to fabricated NMOS and PMOS devices simultaneously

CMOS



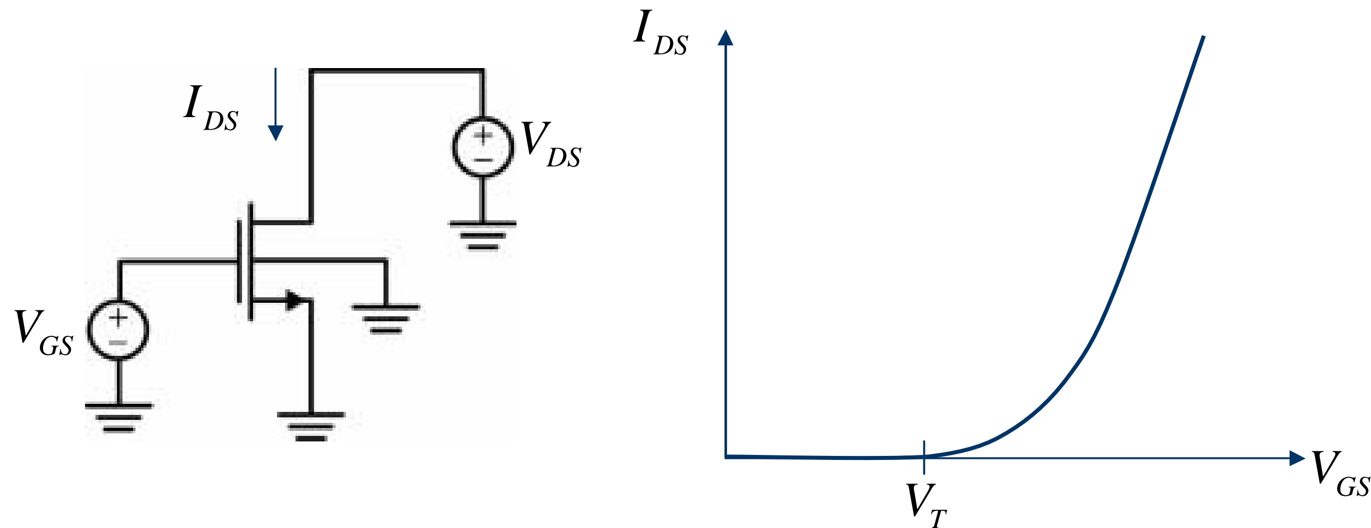
- Complementary MOS: Both P and N type devices
- Create a n-type body in a p-type substrate through compensation. This new region is called a "well".
- To isolate the PMOS from the NMOS, the well must be reverse biased (pn junction)

Circuit Symbols



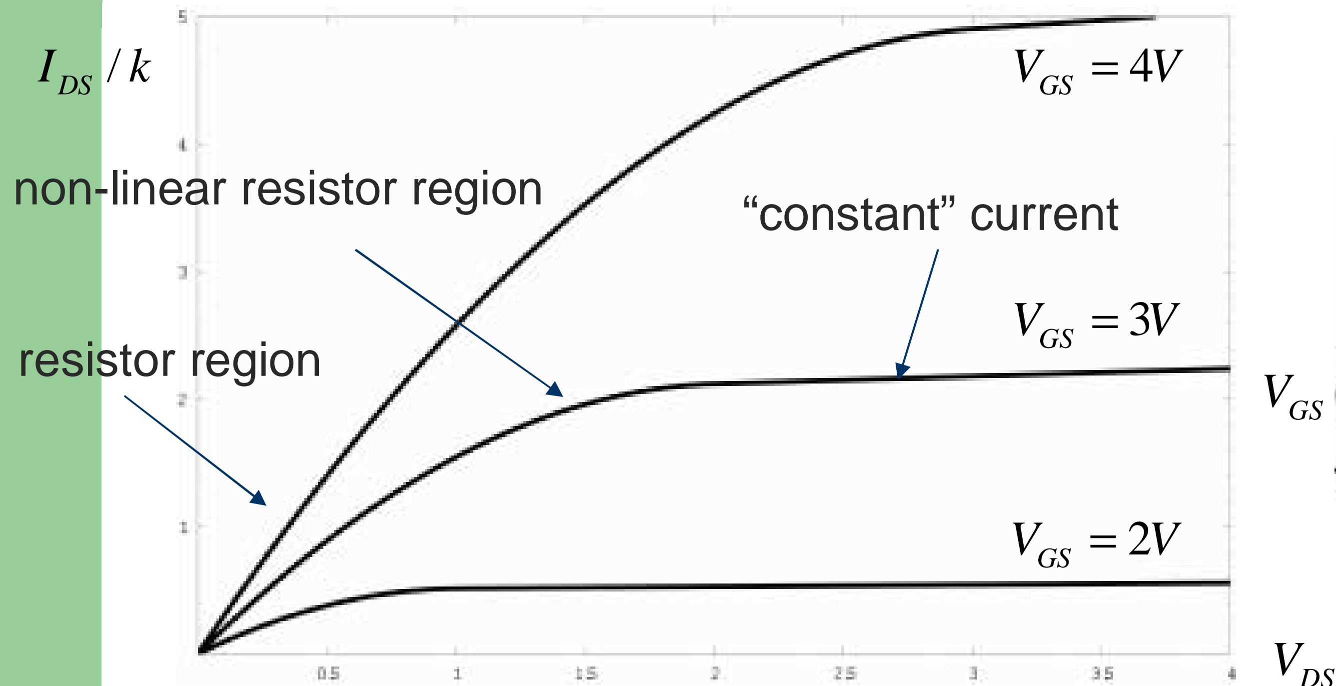
- The symbols with the arrows are typically used in analog applications
- The body contact is often not shown
- The source/drain can switch depending on how the device is biased (the device has inherent symmetry)

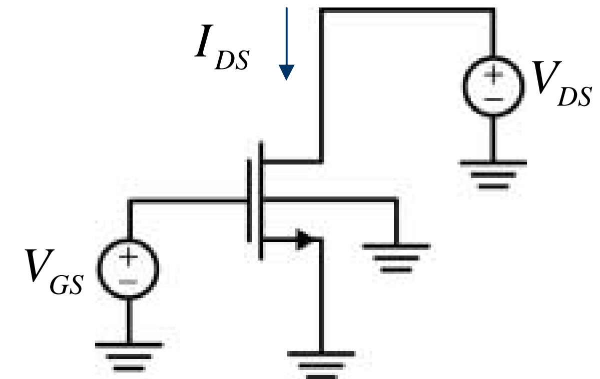
Observed Behavior: I_D-V_{GS}



- Current zero for negative gate voltage
- Current in transistor is very low until the gate voltage crosses the threshold voltage of device (same threshold voltage as MOS capacitor)
- Current increases rapidly at first and then it finally reaches a point where it simply increases linearly

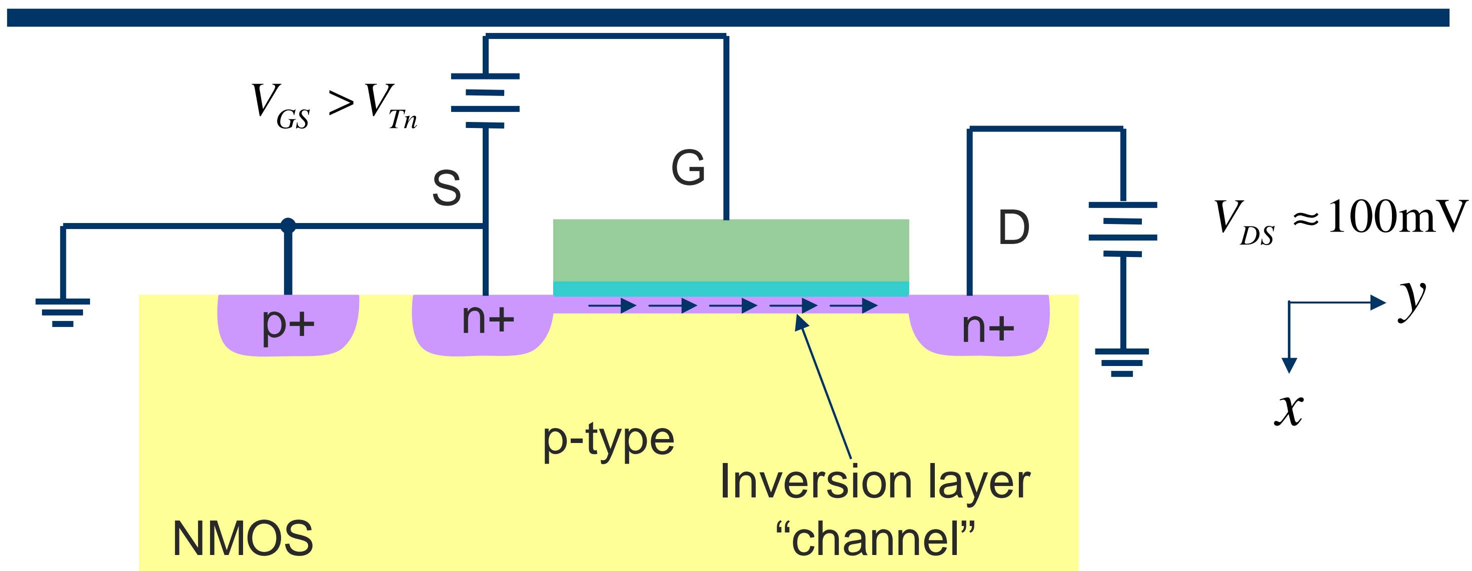
Observed Behavior: I_D-V_{DS}





- For low values of drain voltage, the device is like a resistor
- As the voltage is increases, the resistance behaves non-linearly and the rate of increase of current slows
- Eventually the current stops growing and remains essentially constant (current source)

"Linear" Region Current



- If the gate is biased above threshold, the surface is inverted
- This inverted region forms a channel that connects the drain and gate
- If a drain voltage is applied positive, electrons will flow from source to drain

MOSFET "Linear" Region

- The current in this channel is given by

$$I_{DS} = -Wv_y Q_N$$

- The charge proportional to the voltage applied across the oxide over threshold

$$Q_N = C_{ox}(V_{GS} - V_{Tn})$$

$$I_{DS} = -Wv_y C_{ox}(V_{GS} - V_{Tn})$$

- If the channel is uniform density, only drift current flows

$$v_y = -\mu_n E_y \qquad E_y = -\frac{V_{DS}}{L}$$

$$I_{DS} = \frac{W}{L}\mu_n C_{ox}(V_{GS} - V_{Tn})V_{DS} \qquad V_{GS} > V_{Tn} \quad V_{DS} \approx 100\text{mV}$$

MOSFET: Variable Resistor

- Notice that in the linear region, the current is proportional to the voltage

$$I_{DS} = \frac{W}{L}\mu_n C_{ox}(V_{GS} - V_{Tn})V_{DS}$$

- Can define a voltage-dependent resistor

$$R_{eq} = \frac{V_{DS}}{I_{DS}} = \frac{1}{\mu_n C_{ox}(V_{GS} - V_{Tn})}\left(\frac{L}{W}\right) = R_{\square}(V_{GS})\frac{L}{W}$$

- This is a nice variable resistor, electronically tunable!