

# EE105 – Fall 2014

## Microelectronic Devices and Circuits

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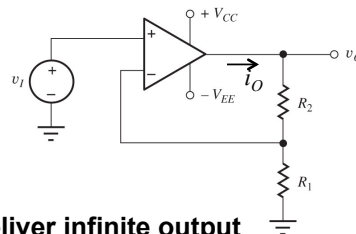


## Operational Amplifier Error Sources: dc Current and Output Range Limitations

- dc error sources result from the need to bias the internal circuits that form an operational amplifier and from mismatches between pairs of solid state devices in these circuits.

- These dc error sources include:

- Input offset voltage  $V_{OS}$
- Input bias current  $I_B$
- Input offset current  $I_{OS}$



- A real op amp obviously cannot deliver infinite output voltage or output current. Both are bounded:

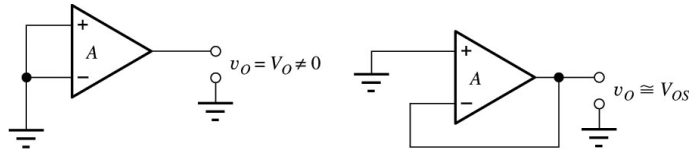
- $-V_{EE} \leq v_O \leq +V_{CC}$
- $|i_O| \leq I_{max}$



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## Input-Offset Voltage



With inputs being zero, the amplifier output rests at some non zero dc voltage level

The equivalent dc input offset voltage is

$$V_{OS} = \frac{V_O}{A}$$

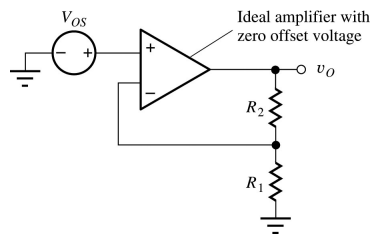
The amplifier is connected as a voltage-follower to give output voltage that is approximately equal to the offset voltage.

To model the effects of offset voltage,

$$v_O = A(v_{ID} + V_{OS})$$



## Input-Offset Voltage (Example)



**Problem:** Find quiescent dc voltage at output.

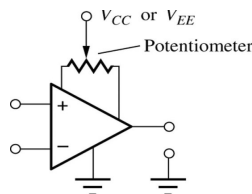
**Given data:**  $R_1 = 1.2 \text{ k}\Omega$ ,  $R_2 = 99 \text{ k}\Omega$ ,  $|V_{OS}| \leq 3 \text{ mV}$

**Assumptions:** The op amp is ideal except for nonzero offset voltage.

- Output voltage is given by

$$|V_{OS}| \leq \left(1 + \frac{99 \text{ k}\Omega}{1.2 \text{ k}\Omega}\right)(0.003) = 0.251 \text{ V}$$

- The actual sign of  $V_{OS}$  is unknown as only an upper bound is given.
- Note: The offset voltage of most IC op amps can be manually adjusted by adding a potentiometer as shown.



## Power Supply Rejection Ratio (PSRR)

- Power supply voltages change due to long-term drift or noise on supplies.
- Equivalent input offset voltage changes in response to power supply voltage changes.
- PSRR measures the ability of amplifier to reject power supply variations.
- PSRR indicates how offset voltage changes in response to change in power supply voltages.

$$PSRR_+ = \frac{\Delta V_{OS}}{\Delta V_{CC}}$$

$$PSRR_- = \frac{\Delta V_{OS}}{\Delta V_{EE}}$$

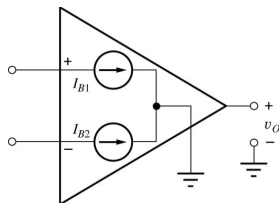
- Generally The “+” and “-” values of PSRR are generally different.
- Both CMRR and PSRR fall rapidly with frequency increase.



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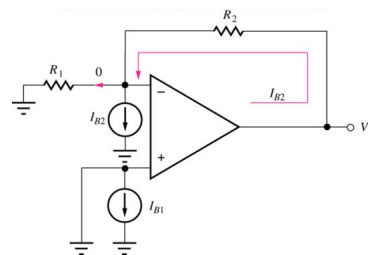
## Input-Bias and Offset Currents



Bias currents  $I_{B1}$  and  $I_{B2}$  (base currents in BJTs or gate currents in MOSFETs or JFETs) are similar in value with directions depending on the internal amplifier circuitry.

$$I_{OS} = I_{B1} - I_{B2}$$

Sign of the offset current is unknown as only upper bound is given.



In the inverting amplifier shown,  $I_{B1}$  is shorted out by the ground connection. Since, the inverting input is at virtual ground, the amplifier output is forced to supply  $I_{B2}$  through  $R_2$ .

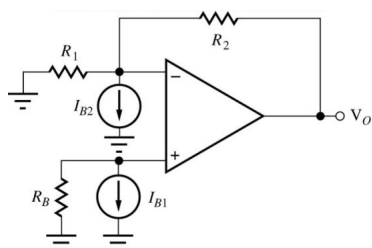
$$V_O = I_{B2} R_2$$



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## Bias Current Compensation



Bias current compensation resistor  $R_B$  is placed in series with the non-inverting input. Output due to  $I_{B1}$  alone is

$$V_O = -I_{B1}R_B \left(1 + \frac{R_2}{R_1}\right)$$

Using superposition:

$$V_O^T = I_{B2}R_2 - I_{B1}R_B \left(1 + \frac{R_2}{R_1}\right)$$

$$V_O^T = (I_{B2} - I_{B1})R_2 = -I_{OS}R_2$$

$$\text{for } R_B = \frac{R_1R_2}{R_1 + R_2}$$

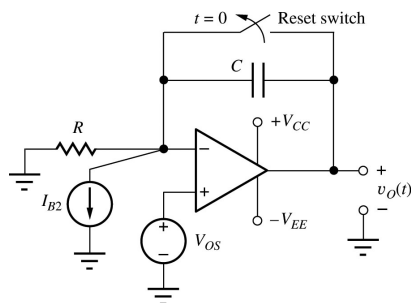
Since, the offset current is typically 5-10 times smaller than individual bias currents, the dc output voltage error can be reduced by using bias compensation.



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## Bias Currents Errors in Integrator



At  $t < 0$ , the reset switch is closed, circuit becomes a voltage-follower with

$$V_O = V_{OS}$$

At  $t = 0$ , the reset switch is opened, and the circuit starts integrating its own offset voltage and bias current. Using analysis by superposition:

$$v(t) = V_{OS} + \frac{V}{RC}t + \frac{I_{B2}}{C}t$$

The output becomes a ramp with slope determined by  $V_{OS}$  and  $I_{B2}$ , and eventually saturates at one of the power supplies.



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## Output Voltage and Current Limits

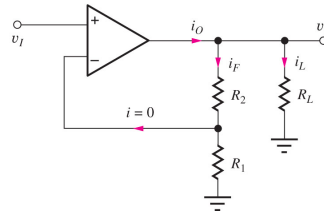
Practical op amps have limited output voltage and current ranges.

**Voltage:** Typically limited to several volts less than power supply span.

**Current:** Limited by additional circuits (to limit power dissipation or protect against accidental short circuits).

Current limit is often specified as minimum load resistance that the amplifier can drive with a given voltage swing. For example,

$$|i_o| \leq \frac{10V}{5k\Omega} = 2 \text{ mA}$$



$$i_o = i_L + i_F = \frac{v_o}{R_L} + \frac{v_o}{R_2 + R_1} = \frac{v_o}{R_{EQ}}$$

$$R_{EQ} = R_L \parallel (R_2 + R_1)$$

For the inverting amplifier,

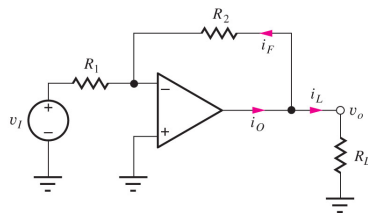
$$R_{EQ} = R_L \parallel R_2$$



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## Output Voltage and Current Limits Example



- **Problem:** Design an inverting amp with given specifications.
- **Given Data:**  $A_v = 20 \text{ dB}$ ,  $R_L \geq 5 \text{ k}\Omega$ ,  $v_o \leq 10 \text{ V}$ . Magnitude of output current less than 2.5 mA.

- **Assumptions:** Ideal op amp except for limited output current.

- **Analysis:**

$$R_{EQ} = R_L \parallel R_2 \geq \frac{10V}{2.5mA} = 4 \text{ k}\Omega$$

$$\text{Since } R_L \geq 5 \text{ k}\Omega, R_2 \geq 20 \text{ k}\Omega$$

$$A_v = 20 \text{ dB} \rightarrow \frac{R_2}{R_1} = 10$$

- Choose  $R_1 = 10 \text{ k}\Omega$  and  $R_2 = 100 \text{ k}\Omega$  to provide an input resistance of 10 kΩ.

- The maximum output current will be:

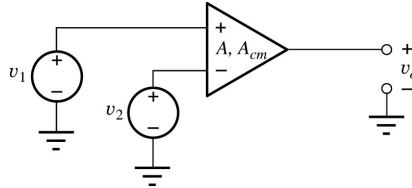
$$i_o \leq \frac{10V}{100k\Omega} + \frac{10V}{5k\Omega} = 2.1 \text{ mA} < 2.5 \text{ mA}$$



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## Finite Common-Mode Rejection Ratio (CMRR)



A real amplifier responds to signal common to both inputs, called common-mode input voltage. In general,

$$v_O = A(v_1 - v_2) + A_{cm} \left( \frac{v_1 + v_2}{2} \right)$$

Differential-mode Input:  $v_{id} = v_1 - v_2$

$$v_O = A(v_{id}) + A_{cm}(v_{ic})$$

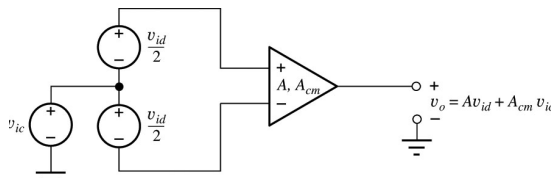
Common-mode Input:  $v_{ic} = \frac{v_1 + v_2}{2}$



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## Finite Common-Mode Rejection Ratio CMRR



$$v_1 = v_{ic} + \frac{v_{id}}{2} \quad v_2 = v_{ic} - \frac{v_{id}}{2}$$

$A$  (or  $A_{dm}$ ) = differential-mode gain

$A_{cm}$  = common-mode gain

$v_{id}$  = differential-mode input voltage

$v_{ic}$  = common-mode input voltage

An ideal amplifier has  $A_{cm} = 0$ , but for a real amplifier,

$$v_O = A \left( v_{id} + \frac{A_{cm} v_{ic}}{A} \right) = A \left( v_{id} + \frac{v_{ic}}{CMRR} \right)$$

$$CMRR = \frac{A}{A_{cm}}$$

The actual sign of CMRR is not known before hand as only a lower bound is typically provided.



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## Finite CMRR Example

- **Problem:** Find the error introduced by finite CMRR.
- **Given Data:**  $A = 2500$ ,  $CMRR = 80 \text{ dB}$ ,  $v_1 = 5.001 \text{ V}$ ,  $v_2 = 4.999 \text{ V}$
- **Assumptions:** Op amp is ideal except for finite gain and CMRR. The CMRR of 80 dB corresponds to CMRR of  $\pm 10^4$ . Assume  $CMRR = +10^4$

• **Analysis:**

$$v_{id} = 5.001\text{V} - 4.999\text{V} = 0.002 \text{ V}$$

$$v_{ic} = \frac{5.001 + 4.999}{2} \text{ V} = 5.00 \text{ V}$$

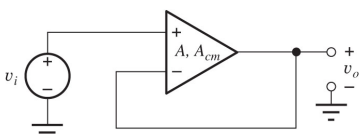
$$v_o = A \left( v_{id} + \frac{v_{ic}}{CMRR} \right) = 2500 \left( 0.002 + \frac{5.000}{10000} \right) = 6.25 \text{ V}$$

$$A_{cm} = \frac{A}{CMRR} = \frac{2500}{10000} = 0.25 \quad \text{or} \quad -12 \text{ dB}$$

- **The error introduced by the common-mode input is 25% of the differential input voltage.**



## Finite CMRR Voltage Follower Gain Error



**Ideal gain for voltage follower is unity, gain error**

$$GE = 1 - A_v = \frac{1 - \frac{A}{CMRR}}{1 + A \left( 1 - \frac{1}{2CMRR} \right)}$$

$$\approx \frac{1}{A} - \frac{1}{CMRR}$$

$$v_{id} = v_i - v_o \quad v_{ic} = \frac{v_i + v_o}{2}$$

$$v_o = A \left[ (v_i - v_o) + \frac{v_i + v_o}{2CMRR} \right]$$

$$A_v = \frac{v_o}{v_i} = \frac{A \left( 1 + \frac{1}{2CMRR} \right)}{1 + A \left( 1 - \frac{1}{2CMRR} \right)}$$

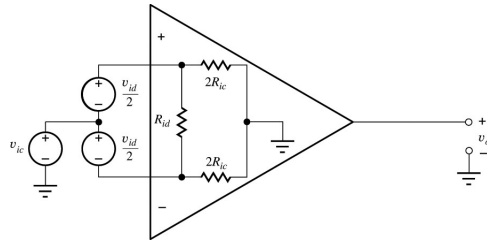
since both  $A$  and  $CMRR \gg 1$

**The first term is due to finite amplifier gain; the second term shows that CMRR may introduce an even larger error.**



## Common-mode Input Resistance

### Op Amp Input Equivalent Circuit



- When a purely common-mode signal  $v_{ic}$  is applied to the amplifier input ( $v_{id} = 0$ ), total resistance presented to source is  $2R_{ic} || 2R_{ic} = R_{ic}$  where  $R_{ic}$  is the common-mode input resistance.
- Normally,  $R_{ic} \gg R_{id}$ .
- For a purely differential-mode input signal, input resistance is  $R_{in} = R_{id} || 4R_{ic}$